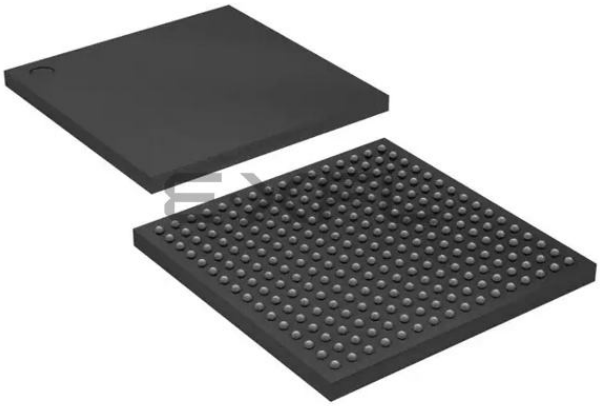

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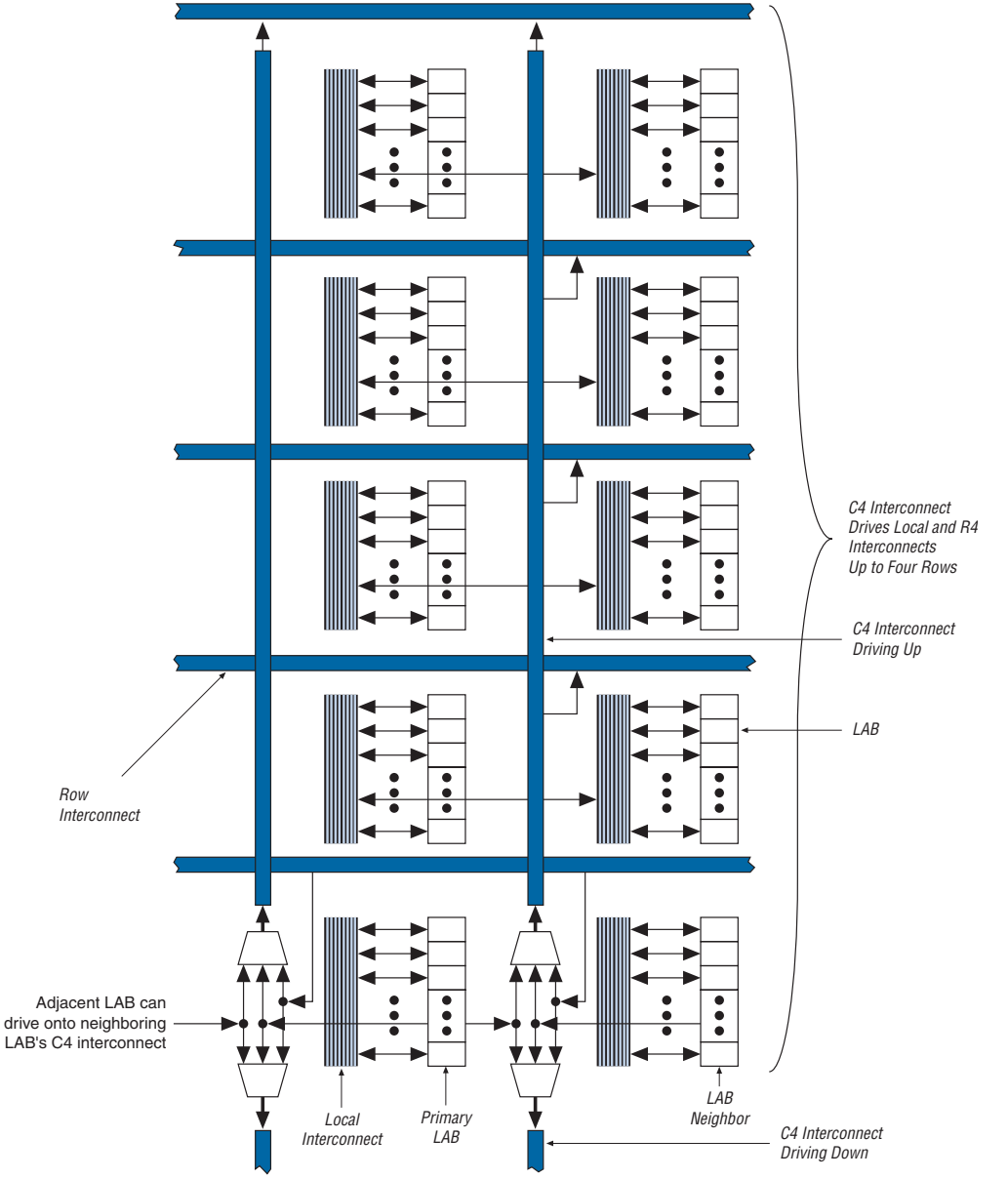
Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	182
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8f256c6n

Figure 2–10. C4 Interconnect Connections *Note (1)*



Note to Figure 2–10:
(1) Each C4 interconnect can drive either up or down four rows.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C50	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C70	672-pin FineLine BGA	20 *(4)*	8	8	8
	896-pin FineLine BGA	20 *(4)*	8	8	8

Notes to Table 2–15:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRI implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 2–15.

You can use any of the DQ pins for the parity pins in Cyclone II devices. The Cyclone II device family supports parity in the ×8/×9, and ×16/×18 mode. There is one parity bit available per eight bits of data pins.

The data mask, DM, pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are assigned and are the preferred pins. Each group of DQS and DQ signals requires a DM pin.

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two clock outputs is needed to generate the system and write clock. The system clock is used to clock the DQS write signals, commands, and addresses. The write clock is shifted by –90° from the system clock and is used to clock the DQ signals during writes.

Figure 2–27 illustrates DDR SDRAM interfacing from the I/O through the dedicated circuitry to the logic array.

I/O Banks

The I/O pins on Cyclone II devices are grouped together into I/O banks and each bank has a separate power bus. EP2C5 and EP2C8 devices have four I/O banks (see Figure 2–28), while EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices have eight I/O banks (see Figure 2–29). Each device I/O pin is associated with one I/O bank. To accommodate voltage-referenced I/O standards, each Cyclone II I/O bank has a VREF bus. Each bank in EP2C5, EP2C8, EP2C15, EP2C20, EP2C35, and EP2C50 devices supports two VREF pins and each bank of EP2C70 supports four VREF pins. When using the VREF pins, each VREF pin must be properly connected to the appropriate voltage level. In the event these pins are not used as VREF pins, they may be used as regular I/O pins.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support all I/O standards listed in Table 2–17, except the PCI/PCI-X I/O standards. The left and right side I/O banks (banks 1 and 3 in EP2C5 and EP2C8 devices and banks 1, 2, 5, and 6 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support I/O standards listed in Table 2–17, except SSTL-18 class II, HSTL-18 class II, and HSTL-15 class II I/O standards. See Table 2–17 for a complete list of supported I/O standards.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support DDR2 memory up to 167 MHz/333 Mbps and QDR memory up to 167 MHz/668 Mbps. The left and right side I/O banks (1 and 3 of EP2C5 and EP2C8 devices and 1, 2, 5, and 6 of EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) only support SDR and DDR SDRAM interfaces. All the I/O banks of the Cyclone II devices support SDR memory up to 167 MHz/167 Mbps and DDR memory up to 167 MHz/333 Mbps.

DDR2 and QDRII interfaces may be implemented in Cyclone II side banks if the use of class I I/O standard is acceptable.

Table 5–17. IOE Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TCOMBIN2PIN_C	1418	2622	1352	2831	1352	3041	ps
	—	—	1418	—	1418	—	ps
TCLR	137	—	165	—	165	—	ps
	—	—	151	—	165	—	ps
TPRE	192	—	233	—	233	—	ps
	—	—	212	—	233	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps

Notes to Table 5–17:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–18. DSP Block Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	47	—	62	—	62	—	ps
	—	—	54	—	62	—	ps
TH	110	—	113	—	113	—	ps
	—	—	111	—	113	—	ps
TCO	0	0	0	0	0	0	ps
	—	—	0	—	0	—	ps
TINREG2PIPE9	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps
TINREG2PIPE18	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–25:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–26. EP2C15A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–26:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C20/A Clock Timing Parameters

Tables 5–27 and 5–28 show the clock timing parameters for EP2C20/A devices.

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

EP2C70 Clock Timing Parameters

Tables 5–33 and 5–34 show the clock timing parameters for EP2C70 devices.

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 2 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
LVPECL	—	—	—	—	—	—	402	402	402
LVDS	402	402	402	402	402	402	402	402	402
1.2V_HSTL	110	90	80	—	—	—	110	90	80
1.2V_DIFFERENTIAL_HSTL	110	90	80	—	—	—	110	90	80

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
	12 mA	280	230	190	280	230	190	280	230	190
	16 mA	290	240	200	290	240	200	290	240	200
	20 mA	330	280	230	330	280	230	330	280	230
	24 mA	360	300	250	360	300	250	360	300	250

Table 5–50. LVDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
t_{FALL}	80–20%	150	200	250		150	200	250		150	200	250 (11)		ps
t_{LOCK}	—	—	—	100		—	—	100		—	—	100 (12)		µs

Notes to Table 5–50:

(1) The maximum data rate that complies with duty cycle distortion of 45–55%.

(2) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1562.5 ps) and a t_{DUTY} of 250 ps, the duty cycle distortion is ± t_{DUTY} / (UI*2) *100% = ± 250 ps / (1562.5 *2) * 100% = ± 8%, which gives you a duty cycle distortion of 42–58%.

(3) The TCCS specification applies to the entire bank of LVDS, as long as the SERDES logic is placed within the LAB adjacent to the output pins.

(4) For extended temperature devices, the maximum input clock frequency for ×10 through ×2 modes is 137.5 MHz.

(5) For extended temperature devices, the maximum data rate for ×10 through ×2 modes is 275 Mbps.

(6) For extended temperature devices, the maximum input clock frequency for ×10 through ×2 modes is 200 MHz.

(7) For extended temperature devices, the maximum data rate for ×10 through ×2 modes is 400 Mbps.

(8) For extended temperature devices, the maximum input clock frequency for ×1 mode is 340 MHz.

(9) For extended temperature devices, the maximum data rate for ×1 mode is 340 Mbps.

(10) For extended temperature devices, the maximum output jitter (peak to peak) is 600 ps.

(11) For extended temperature devices, the maximum t_{RISE} and t_{FALL} are 300 ps.

(12) For extended temperature devices, the maximum lock time is 500 us.

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

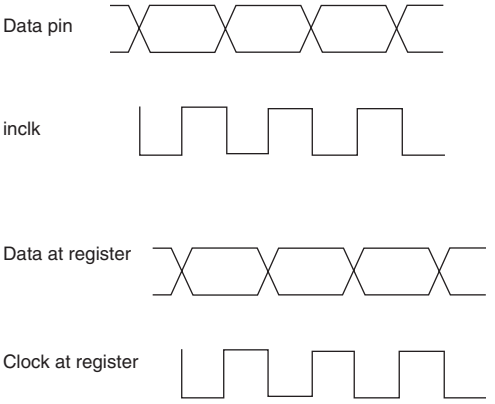
Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by `CLK[3..0]` when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as `LVDSCLK[2..1]p` and `LVDSCLK[2..1]n` pins. When using differential clocks, the `CLK0` pin's secondary function is `LVDSCLK1p`, the `CLK1` pin's secondary function is `LVDSCLK1n`, etc.

Figure 7–7. Phase Relationship between Cyclone II PLL Clocks in Source-Synchronous Compensation Mode



Set the input pin to the register delay chain within the IOE to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL.

Hardware Features

Cyclone II device PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementation and PLL lock circuits.

Clock Multiplication & Division

Cyclone II device PLLs provide clock synthesis for PLL output ports using $m/(n \times \text{post-scale})$ scaling factors. Every PLL has one pre-scale divider, n, with a range of 1 to 4 and one multiply counter, m, with a range of 1 to 32. The input clock, f_{IN}, is divided by a pre-scale counter, n, to produce the input reference clock, f_{REF}, to the PFD. This input reference clock, f_{REF}, is then multiplied by the m feedback factor. The control loop drives the VCO frequency to match $f_{IN} \times (m/n)$. The equations for these frequencies are:

$$f_{REF} = \frac{f_{IN}}{n}$$

$$f_{VCO} = f_{REF} \times m = f_{IN} \frac{m}{n}$$

Each output port has a unique post-scale counter to divide down the high-frequency VCO. There are three post-scale counters (c0, c1, and c2), which range from 1 to 32. The following equations show the frequencies for the three post-scale counters:

$$f_{C0} = \frac{f_{VCO}}{C0} = f_{IN} \frac{m}{n \times C0}$$

$$f_{C1} = \frac{f_{VCO}}{C1} = f_{IN} \frac{m}{n \times C1}$$

$$f_{C2} = \frac{f_{VCO}}{C2} = f_{IN} \frac{m}{n \times C2}$$

All three output counters can drive the global clock network. The c2 output counter can also drive a dedicated external I/O pin (single ended or differential). This counter output can drive a dedicated external clock output pin (`PLL<#>_OUT`) and the global clock network at the same time.

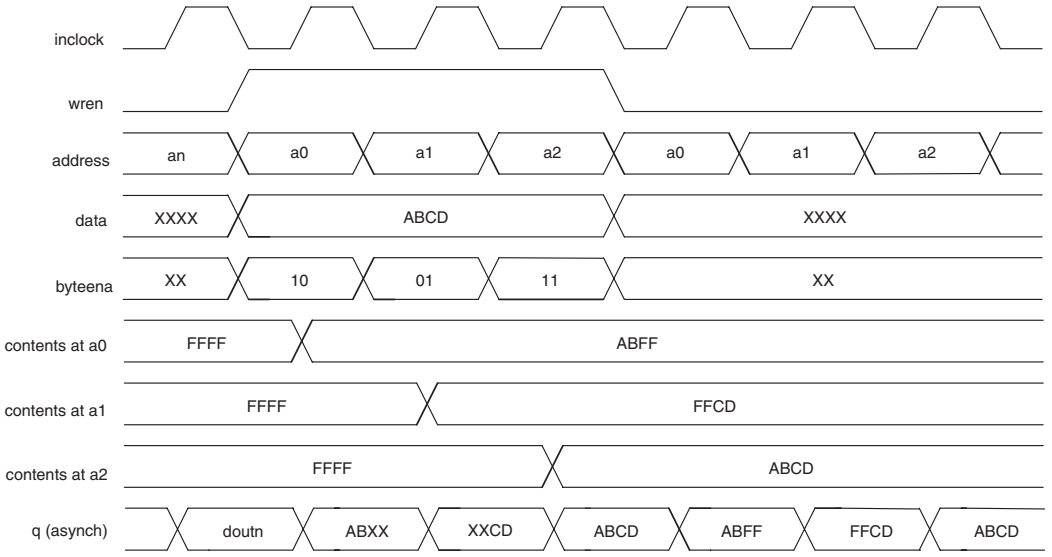
For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets the VCO frequency specifications. Then, the post-scale counters scale down the VCO frequency for each PLL clock output port. For example, if clock output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least common multiple in the VCO's range).

Programmable Duty Cycle

The programmable duty cycle feature allows you to set the PLL clock output duty cycles. The duty cycle is the ratio of the clock output high and low time to the total clock cycle time, expressed as a percentage of high time. This feature is supported on all three PLL post-scale counters, c0, c1, and c2, and when using all clock feedback modes.

The duty cycle is set by using a low- and high-time count setting for the post-scale counters. The Quartus II software uses the input frequency and target multiply/divide ratio to select the post-scale counter. The granularity of the duty cycle is determined by the post-scale counter value chosen on a PLL clock output and is defined as 50% ÷ post-scale counter value. For example, if the post-scale counter value is 3, then the allowable duty cycle precision would be 50% ÷ 3 = 16.67%. Because the `altpll` megafunction does not accept non-integer values for the duty cycle values, the allowable duty cycles are 17% 33% 50% and 67%. For example, if the c0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

Figure 8–2. Cyclone II Byte Enable Functional Waveform



Packed Mode Support

Cyclone II M4K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

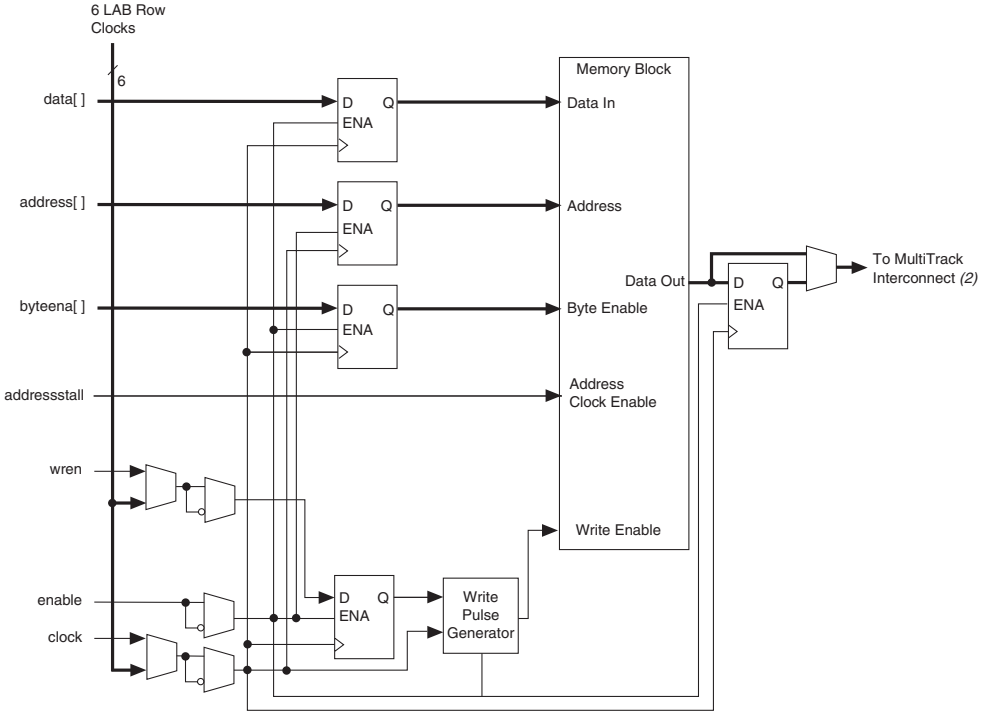
- Each of the two independent block sizes is less than or equal to half of the M4K block size. The maximum data width for each independent block is 18 bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

See "Single-Port Mode" on page 8–9 and "Single-Clock Mode" on page 8–24 for more information.

Address Clock Enable

Cyclone II M4K memory blocks support address clock enables, which holds the previous address value until needed. When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable.

Figure 8–20. Cyclone II Single-Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–20:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in Volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

Power-Up Conditions & Memory Initialization

The Cyclone II memory block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if an MIF pre-loads the contents of the memory block, the outputs still power up cleared. For example, if address 0 is pre-initialized to `FF`, M4K blocks power up with the output at `00`. A subsequent read after power up from address 0 outputs the pre-initialized value of `FF`.

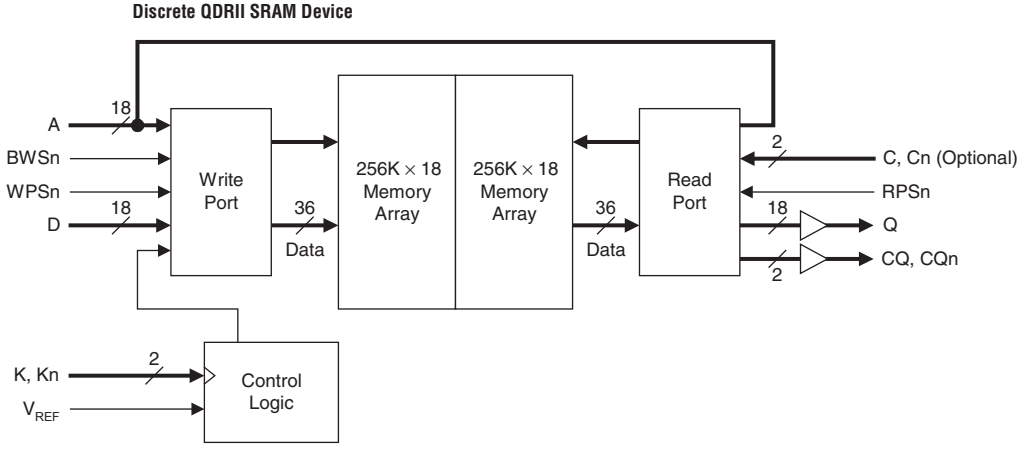
QDRII SRAM

QDRII SRAM is the second generation of QDR SRAM devices. QDRII SRAM devices, which can transfer four words per clock cycle, fulfill the requirements facing next-generation communications system designers. QDRII SRAM devices provide concurrent reads and writes, zero latency, increased data throughput, and allow simultaneous access to the same address location.

Interface Pins

QDRII SRAM devices use two separate, unidirectional data ports for read and write operations, enabling four times the data transfer compared to single data rate devices. QDRII SRAM devices use common control and address lines for read and write operations. Figure 9–3 shows the block diagram for QDRII SRAM burst-of-two architecture.

Figure 9–3. QDRII SRAM Block Diagram for Burst-of-Two Architecture

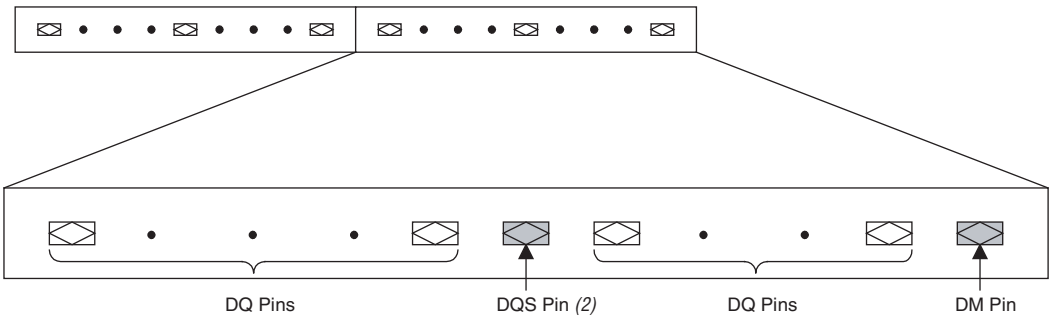


QDRII SRAM burst-of-two devices sample the read address on the rising edge of the clock and the write address on the falling edge of the clock. QDRII SRAM burst-of-four devices sample both read and write addresses on the clock's rising edge. Connect the memory device's Q ports (read data) to the Cyclone II DQ pins. You can use any of the Cyclone II device's user I/O pins in the top and bottom I/O banks for the D ports (write data), commands, and addresses. For maximum performance, Altera recommends connecting the D ports (write data) to the Cyclone II DQ pins, because the DQ pins are pre-assigned to ensure minimal skew.

DDR Memory Interface Pins

Cyclone II devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory. Figure 9–6 shows the DQ and DQS pins in the ×8/×9 mode.

Figure 9–6. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (3)*



Notes to Figure 9–6:

(1) Each DQ group consists of a DQS pin, a DM pin, and up to nine DQ pins.

(2) For the QDRII memory interface, other DQS pins implement the CQn pins. These pins are denoted by DQS/CQ# in the pin table.

(3) This is an idealized pin layout. For the actual pin layout, refer to the pin tables in the *PCB Layout Guidelines* section of the *Cyclone II Device Handbook, Volume 1*.

Data & Data Strobe Pins

Cyclone II data pins for the DDR memory interfaces are called DQ pins. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the DQS pins.

In Cyclone II devices, all the I/O banks support DDR and DDR2 SDRAM and QDRII SRAM memory at up to 167 MHz. All the I/O banks support DQS signals with the DQ bus modes of ×8/×9 and ×16/×18. Cyclone II devices can support either bidirectional data strobes or unidirectional read clocks.

DDR2 and QDRII interfaces with class II I/O standard can only be implemented on the top and bottom I/O banks of the Cyclone II device.

frequency (up to 40 MHz), which reduces your configuration time. In addition, Cyclone II devices can receive a compressed configuration bitstream and decompress this data on-the-fly in the AS or PS configuration scheme, which further reduces storage requirements and configuration time.

If you are testing the device after configuring it, the programmable weak pull-up resister or the bus hold feature overrides the CLAMP value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The HIGHZ instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.

I/O Voltage Support in JTAG Chain

A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone II devices, the TDO pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone II devices can support 2.5- or 3.3-V input levels.

For more information on MultiVolt I/O support, see the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook*.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 14–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

256-Pin FineLine Ball-Grid Array, Option 2 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

This POD is applicable to the F256 package of the Cyclone II product only.

Tables 15–11 and 15–12 show the package information and package outline figure references, respectively, for the 256-pin FineLine BGA package.

Table 15–11. 256-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MO-192 Variation: AAF-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	1.9 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–12. 256-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	1.55
A1	0.25	–	–
A2	1.05 REF		
A3	–	–	0.80
D	17.00 BSC		
E	17.00 BSC		
b	0.40	0.50	0.55
e	1.00 BSC		