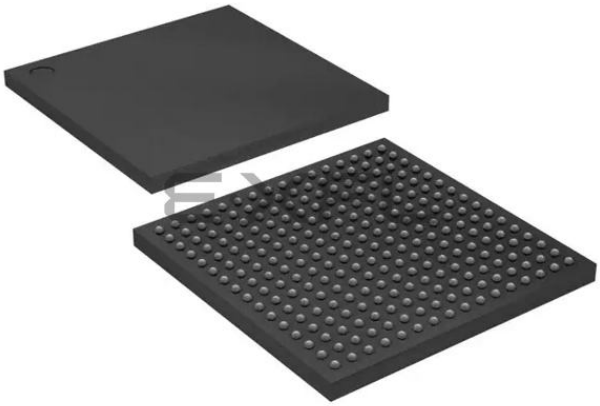

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	182
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8f256c7

Section III. Memory

Chapter 8. Cyclone II Memory Blocks

Chapter 9. External Memory Interfaces

Chapter 10. Selectable I/O Standards in Cyclone II Devices
Revised: *February 2008*
Part number: *CII51010-2.4*

Chapter 11. High-Speed Differential Interfaces in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51011-2.2*

Chapter 12. Embedded Multipliers in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51012-1.2*

Chapter 13. Configuring Cyclone II Devices
Revised: *February 2007*
Part number: *CII51013-3.1*

Chapter 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices
Revised: *February 2007*
Part number: *CII51014-2.1*

Chapter 15. Package Information for Cyclone II Devices
Revised: *February 2007*
Part number: *CII51015-2.3*

1. Introduction

CII51001-3.2

Introduction

Following the immensely successful first-generation Cyclone® device family, Altera® Cyclone II FPGAs extend the low-cost FPGA density range to 68,416 logic elements (LEs) and provide up to 622 usable I/O pins and up to 1.1 Mbits of embedded memory. Cyclone II FPGAs are manufactured on 300-mm wafers using TSMC's 90-nm low-k dielectric process to ensure rapid availability and low cost. By minimizing silicon area, Cyclone II devices can support complex digital systems on a single chip at a cost that rivals that of ASICs. Unlike other FPGA vendors who compromise power consumption and performance for low-cost, Altera's latest generation of low-cost FPGAs—Cyclone II FPGAs, offer 60% higher performance and half the power consumption of competing 90-nm FPGAs. The low cost and optimized feature set of Cyclone II FPGAs make them ideal solutions for a wide array of automotive, consumer, communications, video processing, test and measurement, and other end-market solutions. Reference designs, system diagrams, and IP, found at www.altera.com, are available to help you rapidly develop complete end-market solutions using Cyclone II FPGAs.

Low-Cost Embedded Processing Solutions

Cyclone II devices support the Nios II embedded processor which allows you to implement custom-fit embedded processing solutions. Cyclone II devices can also expand the peripheral set, memory, I/O, or performance of embedded processors. Single or multiple Nios II embedded processors can be designed into a Cyclone II device to provide additional co-processing power or even replace existing embedded processors in your system. Using Cyclone II and Nios II together allow for low-cost, high-performance embedded processing solutions, which allow you to extend your product's life cycle and improve time to market over standard product solutions.

Low-Cost DSP Solutions

Use Cyclone II FPGAs alone or as DSP co-processors to improve price-to-performance ratios for digital signal processing (DSP) applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II features and design support:

- Up to 150 18 × 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interfaces to external memory

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C50	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C70	672-pin FineLine BGA	20 *(4)*	8	8	8
	896-pin FineLine BGA	20 *(4)*	8	8	8

Notes to Table 2–15:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRI implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 2–15.

You can use any of the DQ pins for the parity pins in Cyclone II devices. The Cyclone II device family supports parity in the ×8/×9, and ×16/×18 mode. There is one parity bit available per eight bits of data pins.

The data mask, DM, pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are assigned and are the preferred pins. Each group of DQS and DQ signals requires a DM pin.

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two clock outputs is needed to generate the system and write clock. The system clock is used to clock the DQS write signals, commands, and addresses. The write clock is shifted by –90° from the system clock and is used to clock the DQ signals during writes.

Figure 2–27 illustrates DDR SDRAM interfacing from the I/O through the dedicated circuitry to the logic array.

Cyclone II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Cyclone II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Cyclone II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Cyclone II device via the JTAG port with a USB Blaster™, ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{CONF} *(5) (6)*	Value of I/O pin pull-up resistor before and during configuration	V_{IN} = 0 V; V_{CCIO} = 3.3 V	10	25	50	kΩ
		V_{IN} = 0 V; V_{CCIO} = 2.5 V	15	35	70	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.8 V	30	50	100	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.5 V	40	75	150	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.2 V	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	*(7)*	—	1	2	kΩ

Notes to Table 5–3:

(1) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltages shown in Table 5–4, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(3) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(4) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (www.altera.com) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 5–13 for more information.

(5) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_{IN} value is not 0 V. Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

(6) Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

(7) These values apply to all V_{CCIO} settings.

Table 5–4 shows the maximum V_{IN} overshoot voltage and the dependency on the duty cycle of the input signal. Refer to Table 5–3 for more information.

Table 5–4. V_{IN} Overshoot Voltage for All Input Buffers

Maximum V_{IN} (V)	Input Signal Duty Cycle
4.0	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Single-Ended I/O Standards

Tables 5–6 and 5–7 provide operating condition information when using single-ended I/O standards with Cyclone II devices. Table 5–5 provides descriptions for the voltage and current symbols used in Tables 5–6 and 5–7.

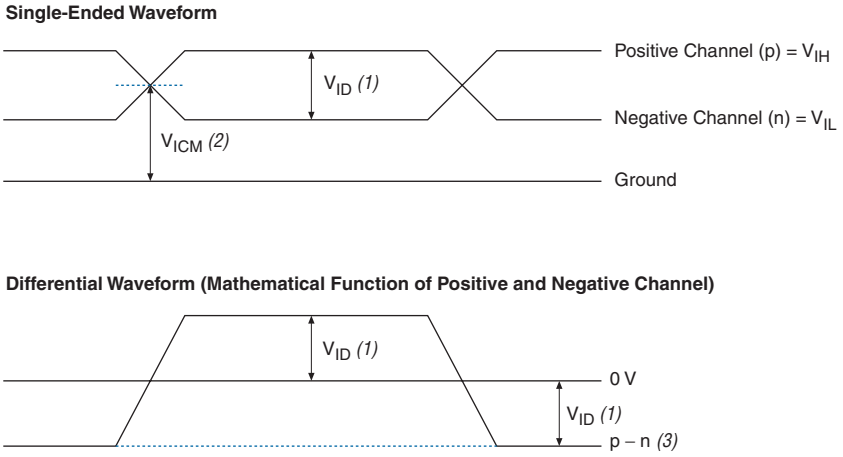
Table 5–5. Voltage and Current Symbol Definitions

Symbol	Definition
V_{CCIO}	Supply voltage for single-ended inputs and for output drivers
V_{REF}	Reference voltage for setting the input switching threshold
V_{IL}	Input voltage that indicates a low logic level
V_{IH}	Input voltage that indicates a high logic level
V_{OL}	Output voltage that indicates a low logic level
V_{OH}	Output voltage that indicates a high logic level
I_{OL}	Output current condition under which V_{OL} is tested
I_{OH}	Output current condition under which V_{OH} is tested
V_{TT}	Voltage applied to a resistor termination as specified by HSTL and SSTL standards

Table 5–6. Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3-V LVTTL and LVCMOS	3.135	3.3	3.465	—	—	—	0.8	1.7
2.5-V LVTTL and LVCMOS	2.375	2.5	2.625	—	—	—	0.7	1.7
1.8-V LVTTL and LVCMOS	1.710	1.8	1.890	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
1.5-V LVCMOS	1.425	1.5	1.575	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
PCI and PCI-X	3.000	3.3	3.600	—	—	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$
SSTL-2 class I	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-2 class II	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-18 class I	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF} - 0.125$ (DC) $V_{REF} - 0.25$ (AC)	$V_{REF} + 0.125$ (DC) $V_{REF} + 0.25$ (AC)

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
LVDS	—	11	13	16	11	13	15	11	13	15
RSDS	—	11	13	16	11	13	15	11	13	15
MINI_LVDS	—	11	13	16	11	13	15	11	13	15
SIMPLE_RSDS	—	15	19	23	15	19	23	15	19	23
1.2V_HSTL	—	130	132	133	—	—	—	—	—	—
1.2V_DIFFERENTIAL_HSTL	—	130	132	133	—	—	—	—	—	—
PCI	—	—	—	—	99	120	142	99	120	142
PCI-X	—	—	—	—	99	121	143	99	121	143
LVTTL	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
LVCMOS	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
2.5V	OCT_50_OHMS	346	369	392	324	326	327	324	326	327
1.8V	OCT_50_OHMS	198	203	209	202	203	204	202	203	204

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 2 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
SSTL-25 class II	✓	✓	✓
RSDS/mini-LVDS *(4)*		✓	✓

Notes to Table 7–6:
(1) The PCI-X I/O standard is supported only on side I/O pins.
(2) Differential SSTL and HSTL outputs are only supported on the PLL<#>_OUT pins.
(3) These I/O standards are only supported on top and bottom I/O pins.
(4) The RSDS and mini-LVDS pins are only supported on output pins.

Clock Feedback Modes

Cyclone II PLLs support four clock feedback modes: normal mode, zero delay buffer mode, no compensation mode, and source synchronous mode. Cyclone II PLLs do not have support for external feedback mode. All the supported clock feedback modes allow for multiplication and division, phase shifting, and programmable duty cycle. The phase relationships shown in the waveforms in Figures 7–4 through 7–6 are for the default (zero degree) phase shift setting. Changing the phase-shift setting changes the relationships between the output clocks from the PLL.

Normal Mode

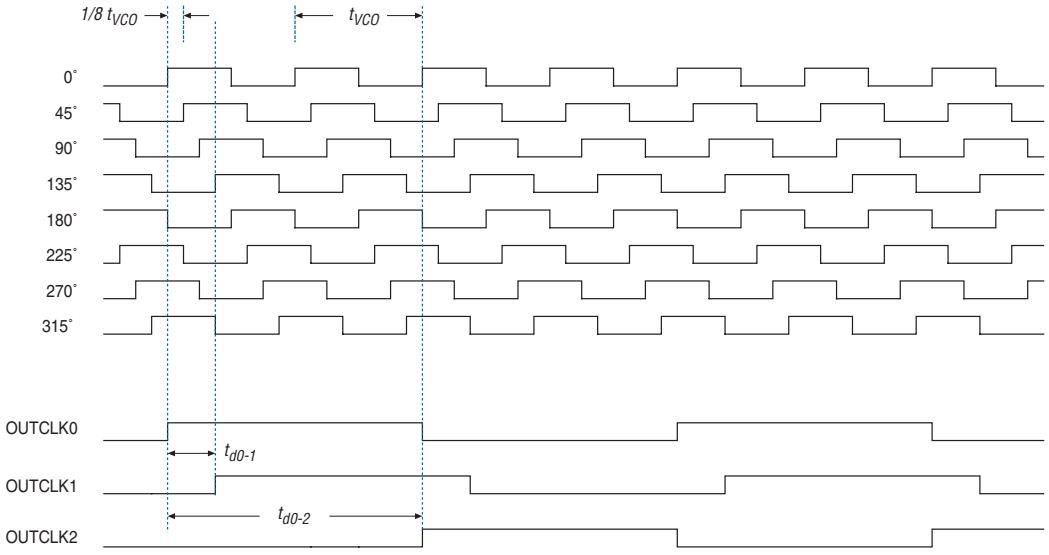
In normal mode, the PLL phase-aligns the input reference clock with the clock signal at the ports of the registers in the logic array I/O registers to compensate for the internal global clock network delay. Use the `altpll` megafunction in the Quartus II software to define which internal clock output from the PLL (c0, c1, or c2) to compensate for.

If an external clock output pin (PLL<#>_OUT) is used in this mode, there is a phase shift with respect to the clock input pin. Similarly, if the internal PLL clock outputs are used to drive general-purpose I/O pins, there is be phase shift with respect to the clock input pin.

Figure 7–4 shows an example waveform of the PLL clocks' phase relationship in this mode.

Δt_{FINE} periods. OUTCLK2 is based off the 0° phase from the VCO but has the S value for the counter set to 3. This creates a delay of two Δt_{COARSE} periods.

Figure 7–8. Cyclone II PLL Phase Shifting using VCO Phase Output & Counter Delay Time



Control Signals

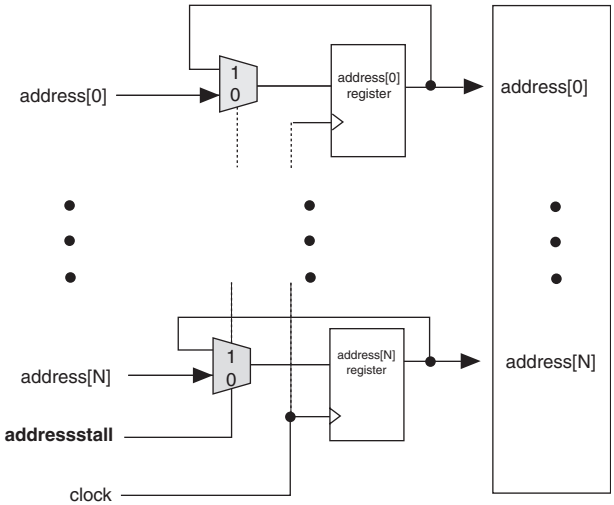
The four control signals in Cyclone II PLLs (pllena, areset, pfdena, and locked) control PLL operation.

pllena

The PLL enable signal, pllena, enables and disables the PLL. You can either enable/disable a single PLL (by connecting pllena port independently) or multiple PLLs (by connecting pllena ports together). The pllena signal is an active-high signal. When pllena is low, the PLL clock output ports are driven by GND and the PLL loses lock. All PLL counters, including gated lock counter return to default state. When pllena transitions high, the PLL relocks and resynchronizes to the input clock. In Cyclone II devices, the pllena port can be fed by an LE output or any general-purpose I/O pin. There is no dedicated pllena pin. This increases flexibility since each PLL can have its own pllena control circuitry or all PLLs can share the same pllena circuitry. The pllena signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

Figure 8–3 shows an address clock enable block diagram. The address register output is fed back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal. Address latching is enabled when the `addressstall` signal goes high (active high). The output of the address register is then continuously fed into the input of the register until the `addressstall` signal goes low.

Figure 8–3. Cyclone II Address Clock Enable Block Diagram

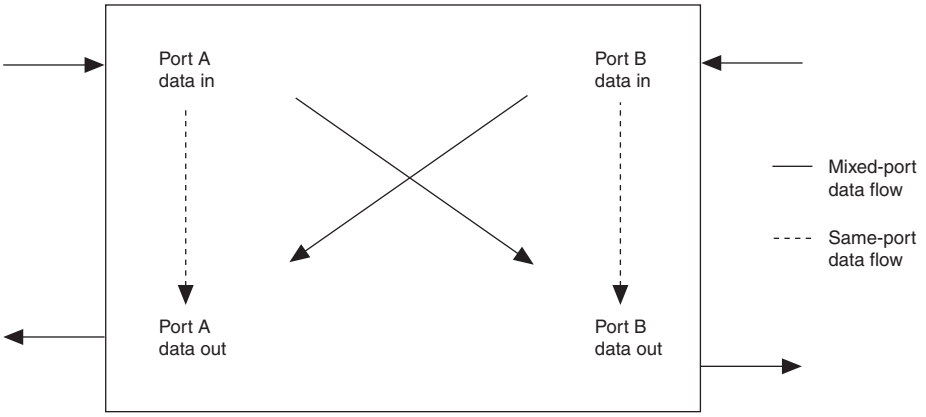


The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 8–4 and 8–5 show the address clock enable waveforms during the read and write cycles, respectively.

Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

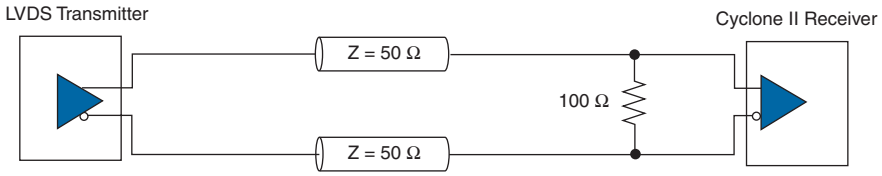
Figure 8–21. Cyclone II Read-During-Write Data Flow



Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

Figure 11–11. LVPECL I/O Interface



Differential SSTL Support in Cyclone II Devices

The differential SSTL I/O standard is a memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. The differential SSTL I/O standard is similar to voltage referenced SSTL and requires two differential inputs with an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected. A 2.5-V output source voltage is required for differential SSTL-2, while a 1.8-V output source voltage is required for differential SSTL-18. The differential SSTL output standard is only supported at PLLCLKOUT pins using two single-ended SSTL output buffers programmed to have opposite polarity.

The differential SSTL input standard is supported at the global clock (GCLK) pins only, treating differential inputs as two single-ended SSTL, and only decoding one of them.

For SSTL signaling characteristics, see the *DC Characteristics & Timing Specification* chapter and the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Figures 11–12 and 11–13 show the differential SSTL class I and II interfaces, respectively.

Section V. DSP

This section provides information for design and optimization of digital signal processing (DSP) functions and arithmetic operations using the embedded multiplier blocks.

This section includes the following chapter:

- Chapter 12, Embedded Multipliers in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone II devices read configuration data via the serial interface, decompress data if necessary, and configure their SRAM cells. The FPGA controls the configuration interface in the AS configuration scheme, while the external host (e.g., the configuration device or microprocessor) controls the interface in the PS configuration scheme.

The Cyclone II decompression feature is available when configuring your Cyclone II device using AS mode.

Table 13–4 shows the MSEL pin settings when using the AS configuration scheme.

Table 13–4. Cyclone II Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
AS (20 MHz)	0	0
Fast AS (40 MHz) *(1)*	1	0

Note to Table 13–4:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

Single Device AS Configuration

Serial configuration devices have a four-pin interface: serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS). This four-pin interface connects to Cyclone II device pins, as shown in Figure 13–3.

devices and to the slave configuration devices. Connect the first configuration device's nCS pin to all the Cyclone II device's CONF_DONE pins, and connect the nCASC pin to the nCS pin of the next configuration device in the chain. Leave the nCASC pin of the last configuration device floating. When the master configuration device sends all the data to the Cyclone II device, the configuration device transitions the nCASC pin low, which drives nCS on the next configuration device. Because a configuration device requires less than one clock cycle to activate a subsequent configuration device, the data stream is uninterrupted.

Enhanced configuration devices (EPC16, EPC8, and EPC4 devices) cannot be cascaded.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, the master configuration device stops configuration for the entire chain and the entire chain must be reconfigured. For example, if the master configuration device does not detect the Cyclone II device's CONF_DONE pin transitioning high at the end of configuration, it resets the entire chain by transitioning its OE pin low. This low signal drives the OE pin low on the slave configuration device(s) and drives nSTATUS low on all Cyclone II devices, causing them to enter a reset state. This behavior is similar to the FPGA detecting an error in the configuration data.

Figure 13–17 shows how to configure multiple devices using cascaded EPC2 or EPC1 devices.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document Revision History

Table 14–4 shows the revision history for this document.

Table 14–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.1	• Added document revision history. • Added new section "BST for Configured Devices".	• Added infomation about 'Always Enable Input Buffer' option.
July 2005 v2.0	Moved the "JTAG Timing Specifications" section to the *DC Characteristics & Timing Specifications* chapter.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline