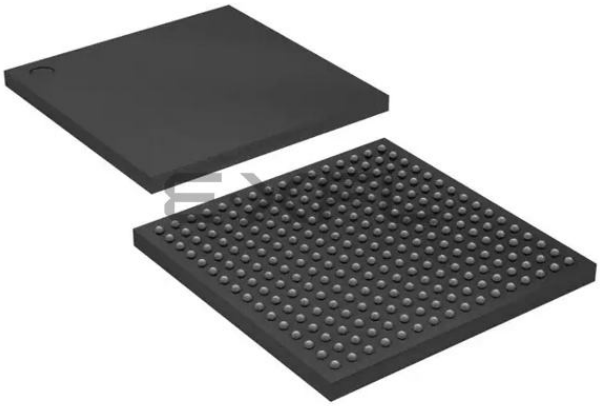

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	182
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8f256c7n

Section IV. I/O Standards

Chapter 10. Selectable I/O Standards in Cyclone II Devices

2. Cyclone II Architecture

CII51002-3.1

Functional Description

Cyclone® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varying speeds provide signal interconnects between logic array blocks (LABs), embedded memory blocks, and embedded multipliers.

The logic array consists of LABs, with 16 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone II devices range in density from 4,608 to 68,416 LEs.

Cyclone II devices provide a global clock network and up to four phase-locked loops (PLLs). The global clock network consists of up to 16 global clock lines that drive throughout the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), LEs, embedded multipliers, and embedded memory blocks. The global clock lines can also be used for other high fan-out signals. Cyclone II PLLs provide general-purpose clocking with clock synthesis and phase shifting as well as external outputs for high-speed differential I/O support.

M4K memory blocks are true dual-port memory blocks with 4K bits of memory plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 260 MHz. These blocks are arranged in columns across the device in between certain LABs. Cyclone II devices offer between 119 to 1,152 Kbits of embedded memory.

Each embedded multiplier block can implement up to either two 9 × 9-bit multipliers, or one 18 × 18-bit multiplier with up to 250-MHz performance. Embedded multipliers are arranged in columns across the device.

Each Cyclone II device I/O pin is fed by an IOE located at the ends of LAB rows and columns around the periphery of the device. I/O pins support various single-ended and differential I/O standards, such as the 66- and 33-MHz, 64- and 32-bit PCI standard, PCI-X, and the LVDS I/O standard at a maximum data rate of 805 megabits per second (Mbps) for inputs and 640 Mbps for outputs. Each IOE contains a bidirectional I/O buffer and three registers for registering input, output, and output-enable signals. Dual-purpose DQS, DQ, and DM pins along with delay chains (used to

4. Hot Socketing & Power-On Reset

CII51004-3.1

Introduction

Cyclone® II devices offer hot socketing (also known as hot plug-in, hot insertion, or hot swap) and power sequencing support without the use of any external devices. You can insert or remove a Cyclone II board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot-socketing feature lessens the board design difficulty when using Cyclone II devices on printed circuit boards (PCBs) that also contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices. With the Cyclone II hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone II hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Cyclone II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Cyclone II Hot-Socketing Specifications

Cyclone II devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone II devices offers the following:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.

Table 5–15. Cyclone II Performance (Part 3 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Burst, 4 Mults/2 Adders FFT function	2400	10	12	235.07	195.0	140.11	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	4343	14	18	200.0	195.0	152.67	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	4043	14	24	200.0	195.0	149.72	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	7496	28	36	200.0	195.0	150.01	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	6896	28	48	200.0	195.0	151.33	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Buffered Burst, 3 Mults/5 Adders FFT function	2934	18	9	235.07	195.0	148.89	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Buffered Burst, 4 Mults/2 Adders FFT function	2784	18	12	235.07	195.0	151.51	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	4720	30	18	200.0	195.0	149.76	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	4420	30	24	200.0	195.0	151.08	163.02

Table 5–18. DSP Block Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPIPE2OUTREG	47	104	45	142	45	185	ps
	—	—	47	—	47	—	ps
TPD9	529	2470	505	3353	505	4370	ps
	—	—	529	—	529	—	ps
TPD18	425	2903	406	3941	406	5136	ps
	—	—	425	—	425	—	ps
TCLR	2686	—	3572	—	3572	—	ps
	—	—	3129	—	3572	—	ps
TCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Notes to Table 5–18:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–19. M4K Block Internal Timing Microparameters (Part 1 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KRC	2387	3764	2275	4248	2275	4736	ps
	—	—	2387	—	2387	—	ps
TM4KWERESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KWEREH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KBESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 2 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
LVPECL	—	—	—	—	—	—	402	402	402
LVDS	402	402	402	402	402	402	402	402	402
1.2V_HSTL	110	90	80	—	—	—	110	90	80
1.2V_DIFFERENTIAL_HSTL	110	90	80	—	—	—	110	90	80

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
	12 mA	280	230	190	280	230	190	280	230	190
	16 mA	290	240	200	290	240	200	290	240	200
	20 mA	330	280	230	330	280	230	330	280	230
	24 mA	360	300	250	360	300	250	360	300	250

JTAG Timing Specifications

Figure 5–7 shows the timing requirements for the JTAG signals.

Figure 5–7. Cyclone II JTAG Waveform

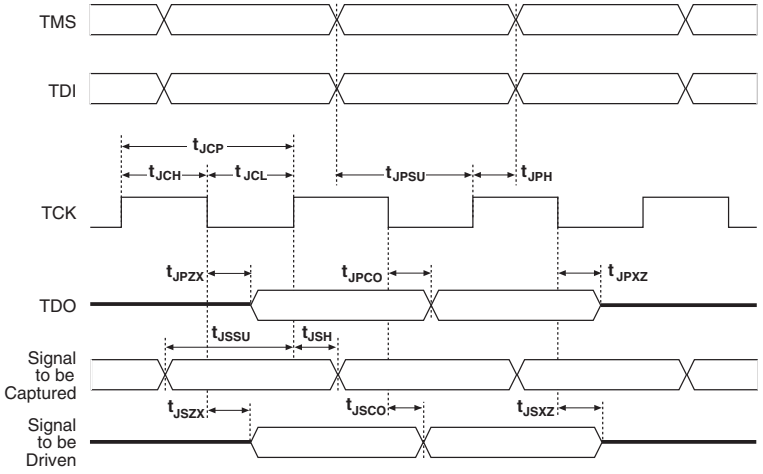


Table 5–53 shows the JTAG timing parameters and values for Cyclone II devices.

Table 5–53. Cyclone II JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time *(2)*	5	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	13	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	13	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	13	ns
t_{JSSU}	Capture register setup time *(2)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–53:

(1) This information is preliminary.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port and capture register clock setup time is 3 ns and port clock to output time is 15 ns.

Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone II devices are in the 18th position or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.

For more information on JTAG, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*.

Table 7–5. PLL Output signals

Port	Description	Source	Destination
c[2..0]	PLL clock outputs driving the internal global clock network or external clock output pin (PLL<#>_OUT)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
LVTTL (3.3, 2.5, and 1.8 V)	✓	✓	✓
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X *(1)*	✓	✓	✓
LVPECL	✓		
LVDS	✓	✓	✓
1.5 and 1.8 V differential HSTL class I and class II	✓		✓ *(2)*
1.8 and 2.5 V differential SSTL class I and class II	✓		✓ *(2)*
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II *(3)*	✓	✓	✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II *(3)*	✓	✓	✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II *(3)*	✓	✓	✓
SSTL-25 class I	✓	✓	✓

clock sources and the clkena signals for the global clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction.

clkena signals

In Cyclone II devices, the clkena signals are supported at the clock network level. Figure 7–14 shows how the clkena is implemented. This allows you to gate off the clock even when a PLL is not being used. Upon re-enabling the output clock, the PLL does not need a resynchronization or relock period because the clock is gated off at the clock network level. Also, the PLL can remain locked independent of the clkena signals since the loop-related counters are not affected.

Figure 7–14. clkena Implementation

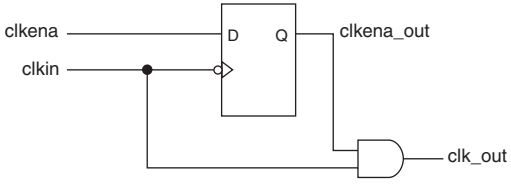


Figure 7–15 shows the waveform example for a clock output enable. clkena is synchronous to the falling edge of the clock (clkin).

This feature is useful for applications that require a low power or sleep mode. The exact amount of power saved when using this feature is pending device characterization.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 2 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C50	129	594,432
EP2C70	250	1,152,000

Control Signals

Figure 8–1 shows how the register clocks, clears, and control signals are implemented in the Cyclone II memory block.

The clock enable control signal controls the clock entering the entire memory block, not just the input and output registers. The signal disables the clock so that the memory block does not see any clock edges and will not perform any operations.

Cyclone II devices do not support asynchronous clear signals to input registers. Only output registers support asynchronous clears. There are three ways to reset the registers in the M4K blocks: power up the device, use the `aclr` signal for output register only, or assert the device-wide reset signal using the `DEV_CLRn` option.

When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

case writing is controlled only by the write enable signals. There is no clear port to the byte enable registers. M4K blocks support byte enables when the write port has a data width of 1, 2, 4, 8, 9, 16, 18, 32, or 36 bits. When using data widths of 1, 2, 4, 8, and 9 bits, the byte enable behaves as a redundant write enable because the data width is less than or equal to a single byte. Table 8–3 summarizes the byte selection.

Table 8–3. Byte Enable for Cyclone II M4K Blocks *Note (1)*

byteena[3..0]	Affected Bytes								
	datain ×1	datain ×2	datain ×4	datain ×8	datain ×9	datain ×16	datain ×18	datain ×32	datain ×36
[0] = 1	[0]	[1..0]	[3..0]	[7..0]	[8..0]	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 1	-	-	-	-	-	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 1	-	-	-	-	-	-	-	[23..16]	[26..18]
[3] = 1	-	-	-	-	-	-	-	[31..24]	[35..27]

Note to Table 8–3:
(1) Any combination of byte enables is possible.

Table 8–4 shows the byte enable port control for true dual-port mode.

Table 8–4. Byte Enable Port Control for True Dual-Port Mode

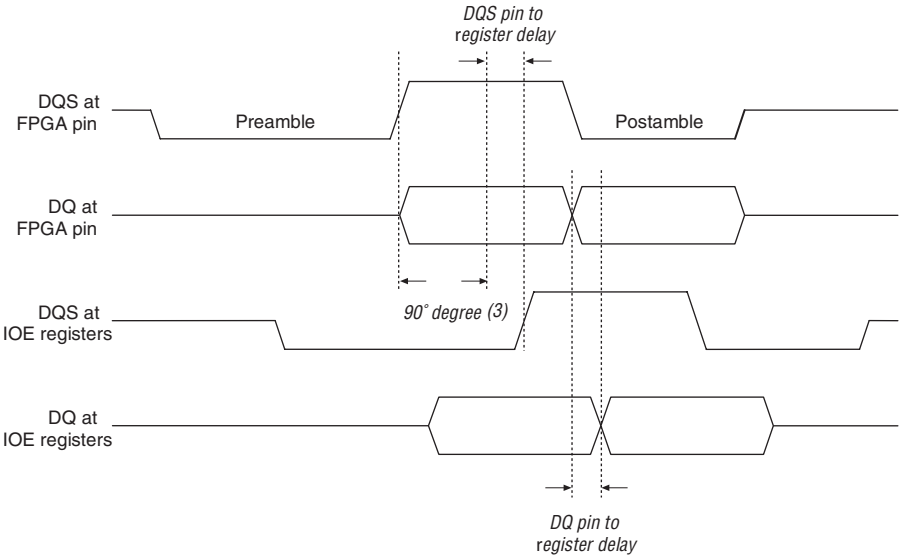
byteena [3:0]	Affected Port
[1:0]	Port A *(1)*
[3:2]	Port B *(1)*

Note to Table 8–4:
(1) For any data width up to ×18 for each port.

Figure 8–2 shows how the `wren` and `byteena` signals control the operations of the RAM.

When a byte enable bit is de-asserted during a write cycle, the corresponding data byte output appears as a "don't care" or unknown value. When a byte enable bit is asserted during a write cycle, the corresponding data byte output is the newly written data.

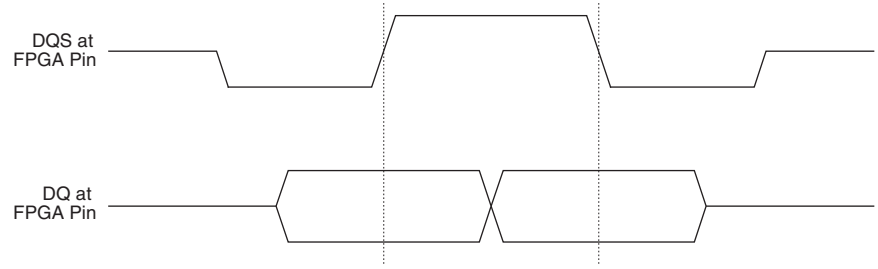
Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write



Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per VCCIO and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per VCCIO and ground pair.

For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per VCCIO and ground pair.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

Software Support

Altera provides two methods for implementing multipliers in your design using embedded multiplier resources: instantiation and inference. Both methods use the following three Quartus II megafunctions:

- `lpm_mult`
- `altmult_add`
- `altmult_accum`

You can instantiate the megafunctions in the Quartus II software to use the embedded multipliers. You can use the `lpm_mult` and `altmult_add` megafunctions to implement multipliers. Additionally, you can use the `altmult_add` megafunctions to implement multiplier-adders where the embedded multiplier is used to implement the multiply function and the adder function is implemented in LEs. The `altmult_accum` megafunction implements multiply accumulate functions where the embedded multiplier implements the multiplier and the accumulator function is implemented in LEs.

See Quartus II On-Line Help for instructions on using the megafunctions and the MegaWizard Plug-In Manager.

For information on our complete DSP Design and Intellectual Property offerings, see **www.Altera.com**.

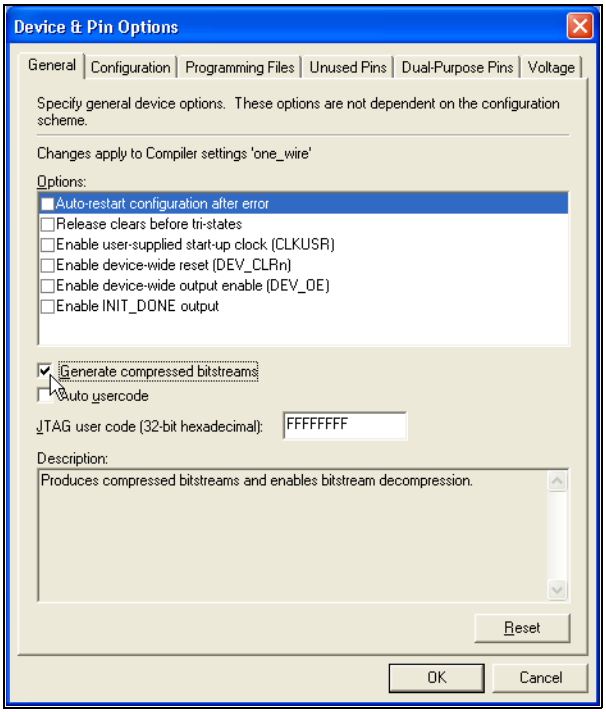
You can also infer the megafunctions by creating an HDL design and synthesize it using Quartus II integrated synthesis or a third-party synthesis tool that recognizes and infers the appropriate multiplier megafunction. Using either method, the Quartus II software maps the multiplier functionality to the embedded multipliers during compilation.

See the Synthesis section in Volume 1 of the ***Quartus II Handbook*** for more information.

Conclusion

The Cyclone II device embedded multipliers are optimized to support multiplier-intensive DSP applications such as FIR filters, FFT functions and encoders. These embedded multipliers can be configured to implement multipliers of various bit widths up to 18-bits to suit a particular application resulting in efficient resource utilization and improved performance and data throughput. The Quartus II software, together with the LeonardoSpectrum and Synplify software provide a complete and easy-to-use flow for implementing multiplier functions using embedded multipliers.

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

Cyclone II devices offer an optional INIT_DONE pin which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** window. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor is required to pull the signal high when nCONFIG is low and during the beginning of configuration. Once the optional bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the FPGA has entered user mode. If you do not use the INIT_DONE pin, the initialization period is complete after CONF_DONE goes high and 299 clock cycles are sent to the CLKUSR pin or after the time t_{CF2UM} (see Table 13–8) if the Cyclone II device uses the internal oscillator.

User Mode

When initialization is complete, the FPGA enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

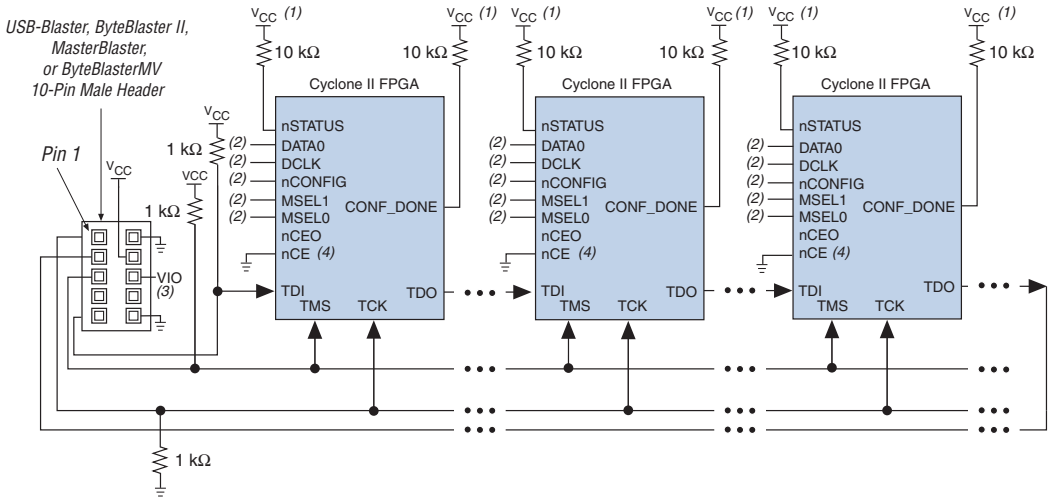
When the Cyclone II device is in user mode, you can initiate reconfiguration by pulling the nCONFIG signal low. The nCONFIG signal should be low for at least 2 µs. When nCONFIG is pulled low, the Cyclone II device is reset and enters the reset stage. The Cyclone II device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Once nCONFIG returns to a logic high level and nSTATUS is released by the Cyclone II device, reconfiguration begins.

Error During Configuration

If an error occurs during configuration, the Cyclone II device drives the nSTATUS signal low to indicate a data frame error, and the CONF_DONE signal stays low. If you enable the **Auto-restart configuration after error** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box, the Cyclone II device resets the serial configuration device by pulsing nCSO, releases nSTATUS after a reset time-out period (about 40 µs), and retries configuration. If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pull nCONFIG low for at least 2 µs to restart configuration.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure CLKUSR continues to toggle during the time nSTATUS is low (a maximum of 40 µs).

Figure 13–24. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 13–24:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II or ByteBlasterMV cable.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) nCE must be connected to ground or driven low for successful JTAG configuration.

Connect the nCE pin to GND or pull it low during JTAG configuration. In multiple device AS and PS configuration chains, connect the first device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain or you can use it as a user I/O pin after configuration.

After the first device completes configuration in a multiple device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, you should make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multiple device configuration chain, the nCEO pin of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured.

14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

CII51014-2.1

Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (e.g., external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared with expected results. Figure 14–1 shows the concept of boundary-scan testing.

Figure 14–1. IEEE Std. 1149.1 Boundary-Scan Testing

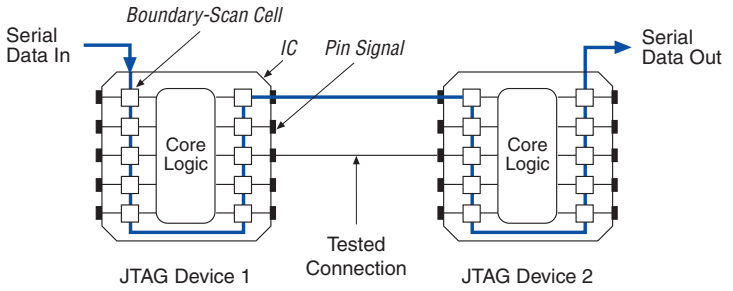


Figure 15–7 shows a 672-pin FineLine BGA package outline.

Figure 15–7. 672-Pin FineLine BGA Package Outline