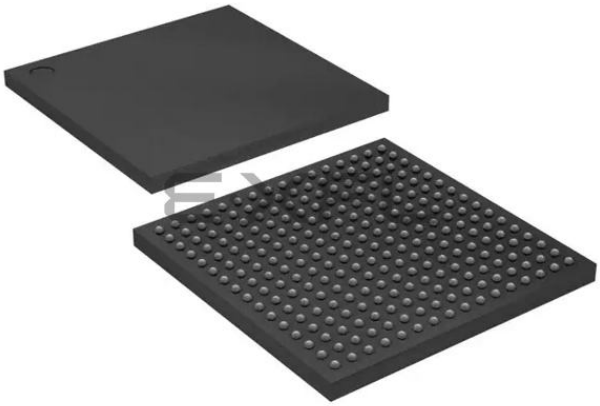

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	182
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8f256c8n

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 2 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
3.3			✓ *(4)*	✓	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓

Notes to Table 2–20:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** option in Device setting option in the Quartus II software.

(3) When V_{CCIO} = 1.8-V, a Cyclone II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin or when V_{CCIO} = 1.8-V and a 1.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected. The reason for this increase is that the input signal level does not drive to the V_{CCIO} rail, which causes the input buffer to not completely shut off.

(5) When V_{CCIO} = 2.5-V, a Cyclone II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(6) When V_{CCIO} = 3.3-V, a Cyclone II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

SRAM configuration elements allow Cyclone II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with the nCONFIG pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

You can load the configuration data for a Cyclone II device with one of three configuration schemes (see Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone II device. A low-cost configuration device can automatically configure a Cyclone II device at system power-up.

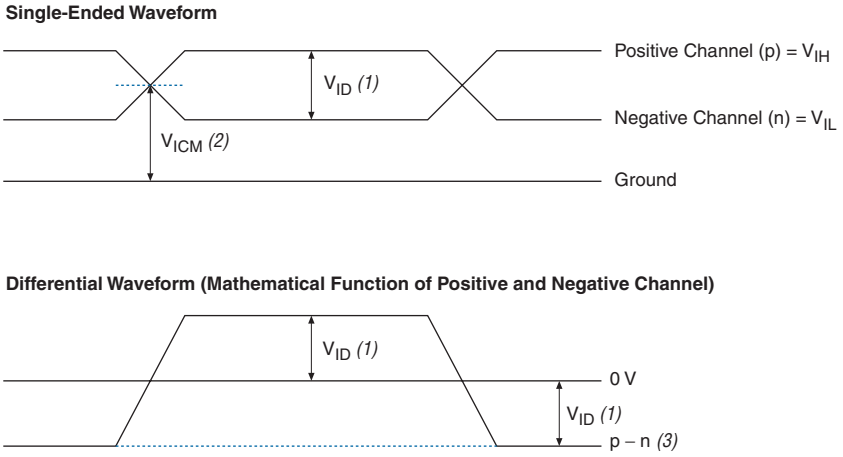
Multiple Cyclone II devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 3–4. Data Sources for Configuration

Configuration Scheme	Data Source
Active serial (AS)	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable, or serial data source
JTAG	MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable or a microprocessor with a Jam or JBC file

For more information on configuration, see the *Configuring Cyclone II Devices* chapter of the *Cyclone II Handbook, Volume 2*.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

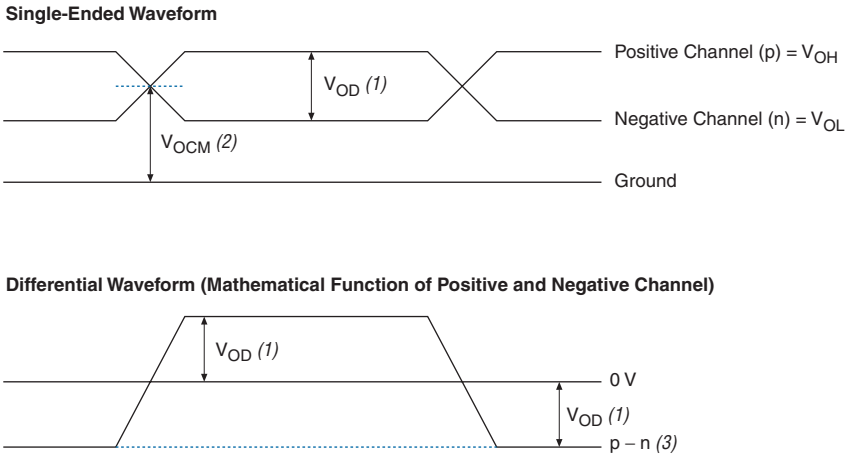
(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2:
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

IOE Programmable Delay

Refer to Table 5–36 and 5–37 for IOE programmable delay.

Table 5–36. Cyclone II IOE Programmable Delay on Column Pins *Notes (1), (2)*

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2233	0	3827	0	4232	0	4349	ps
			0	2344	—	—	0	4088	—	—	ps
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2656	0	4555	0	4914	0	4940	ps
			0	2788	—	—	0	4748	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	303	0	563	0	638	0	670	ps
			0	318	—	—	0	617	—	—	ps

Notes to Table 5–36:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row for each parameter represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins *Notes (1), (2)* ***(Part 1 of 2)***

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2240	0	3776	0	4174	0	4290	ps
			0	2352	—	—	0	4033	—	—	ps

Tables 5–50 and 5–51 show the LVDS timing budget for Cyclone II devices. Cyclone II devices support LVDS receivers at data rates up to 805 Mbps, and LVDS transmitters at data rates up to 640 Mbps.

Table 5–50. LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×8	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×7	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×4	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×2	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (8)	402.5 (8)	MHz
HSIODR	×10	100	—	640	640	100	—	550	640	100	—	311 (5)	550 (7)	Mbps
	×8	80	—	640	640	80	—	550	640	80	—	311 (5)	550 (7)	Mbps
	×7	70	—	640	640	70	—	550	640	70	—	311 (5)	550 (7)	Mbps
	×4	40	—	640	640	40	—	550	640	40	—	311 (5)	550 (7)	Mbps
	×2	20	—	640	640	20	—	550	640	20	—	311 (5)	550 (7)	Mbps
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (9)	402.5 (9)	Mbps
t_{DUTY}	—	45	—	55	—	45	—	55	—	45	—	55	—	%
	—	—	—	—	160	—	—	—	312.5	—	—	—	363.6	ps
TCCS (3)	—	—	—	200		—	—	200		—	—	200		ps
Output jitter (peak to peak)	—	—	—	500		—	—	500		—	—	550 (10)		ps
t_{RISE}	20–80%	150	200	250		150	200	250		150	200	250 (11)		ps

February 2007 v3.1	• Added document revision history. • Added V_{CCA} minimum and maximum limitations in Table 5–1. • Updated *Note (1)* in Table 5–2. • Updated the maximum V_{CC} rise time for Cyclone II "A" devices in Table 5–2. • Updated R_{CONF} information in Table 5–3. • Changed V_I to I_i in Table 5–3. • Updated LVPECL clock inputs in *Note (6)* to Table 5–8. • Updated *Note (1)* to Table 5–12. • Updated C_{VREF} capacitance description in Table 5–13. • Updated "Timing Specifications" section. • Updated Table 5–45. • Added Table 5–46 with information on toggle rate derating factors. • Corrected calculation of the period based on a 640 Mbps data rate as 1562.5 ps in *Note (2)* to Table 5–50. • Updated "PLL Timing Specifications" section. • Updated V_{CO} range of 300–500 MHz in *Note (3)* to Table 5–54. • Updated chapter with extended temperature information.	—
December 2005 v2.2	Updated PLL Timing Specifications	—
November 2005 v2.1	Updated technical content throughout.	—
July 2005 v2.0	Updated technical content throughout.	—
November 2004 v1.1	Updated the "Differential I/O Standards" section. Updated Table 5–54.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Table 7–9. Clock Control Block Inputs (Part 2 of 2)

Input	Description
PLL outputs	The PLL counter outputs can drive the global clock network.
Internal logic	The global clock network can also be driven through the logic array routing to enable internal logic (LEs) to drive a high fan-out, low skew signal path.

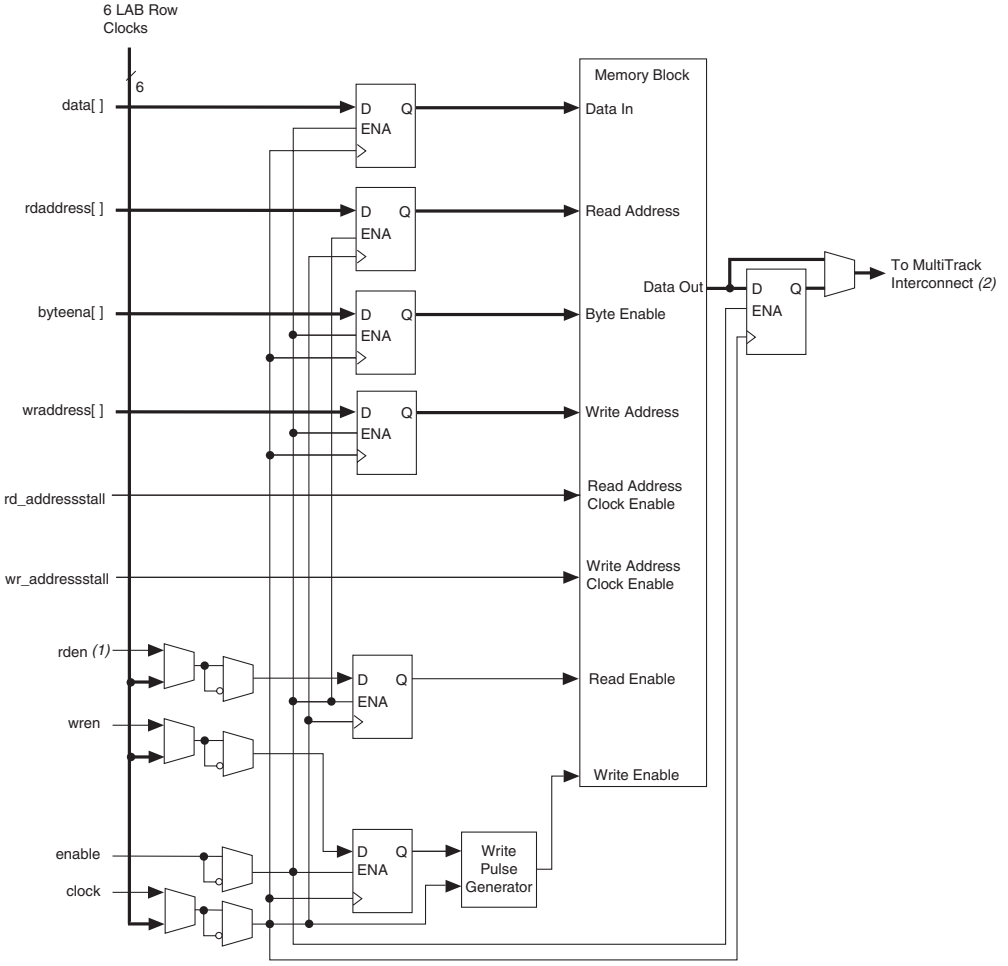
In Cyclone II devices, the dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each global clock network. The output from the clock control block in turn feeds the corresponding global clock network. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device.

The control block has two functions:

- Dynamic global clock network clock source selection
- Global clock network power-down (dynamic enable and disable)

Figure 7–11 shows the clock control block.

Figure 8–19. Cyclone II Single-Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*



Notes to Figure 8–19:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

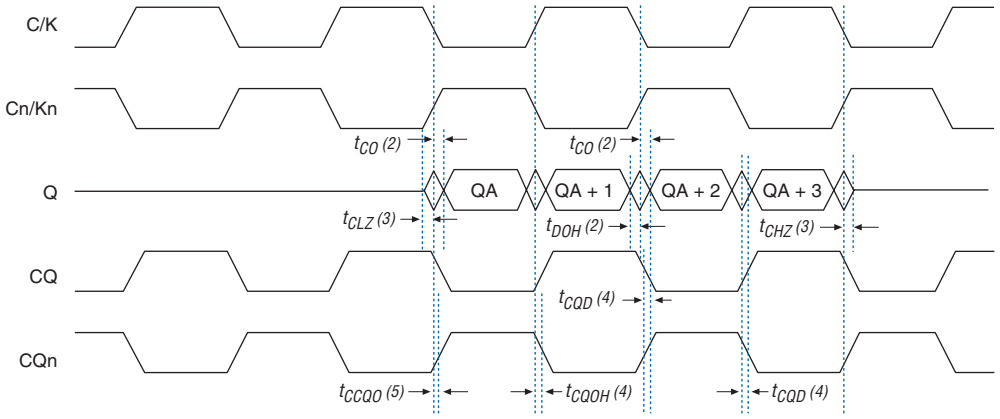
You can use any of the user I/O pins for commands and addresses. Because of the symmetrical setup and hold time for the command and address pins at the memory device, you may need to generate these signals from the negative edge of the system clock.

The clocks to the SDRAM device are called CK and CK#. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the t_{DQSS} requirements of the DDR SDRAM or DDR2 SDRAM device. The memory device's t_{DQSS} requires the positive edge of the write DQS signal to be within 25% of the positive edge of the DDR SDRAM and DDR2 SDRAM clock input. Because of strict skew requirements between CK and CK# signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and pins tied to ground for better noise immunity from other signals.

Read & Write Operation

When reading from the memory, DDR and DDR2 SDRAM devices send the data edge-aligned relative to the data strobe. To properly read the data, the data strobe must be center-aligned relative to the data inside the FPGA. Cyclone II devices feature clock delay control circuitry to shift the data strobe to the middle of the data window. Figure 9–1 shows an example of how the memory sends out the data and data strobe for a burst-of-two operation.

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

Figure 9–9. Cyclone II DQS Postamble Circuitry Connection

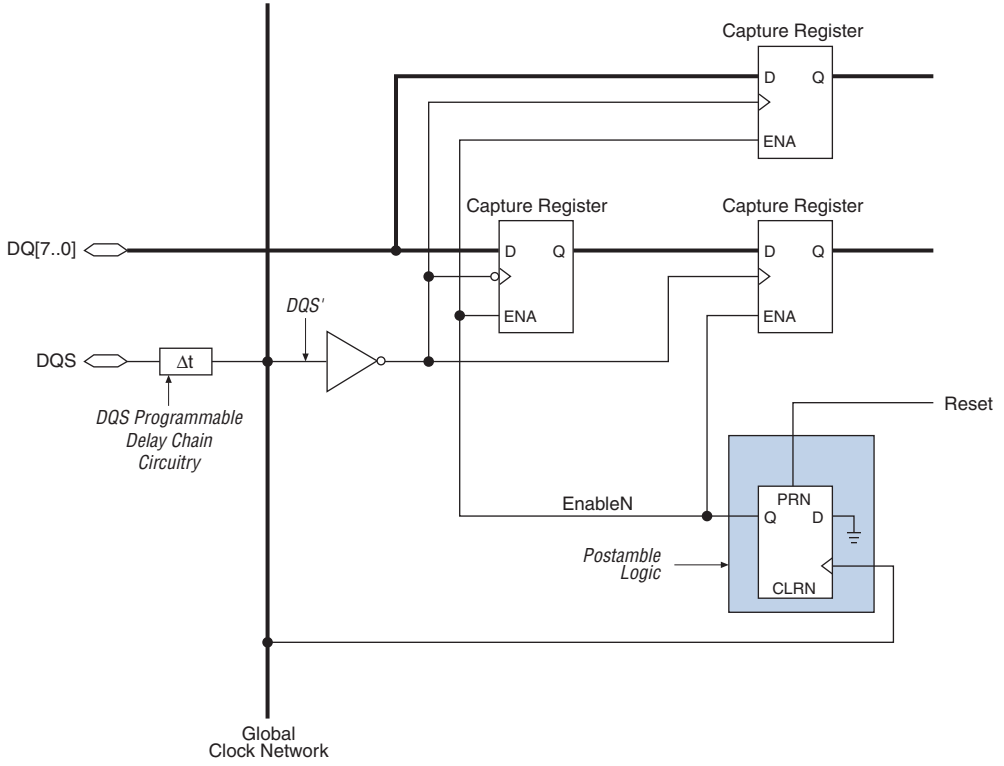


Figure 9–10 shows the timing waveform for Figure 9–9. When the postamble logic detects the falling DQS edge at the start of postamble, it sends out a signal to disable the capture registers to prevent any accidental latching.

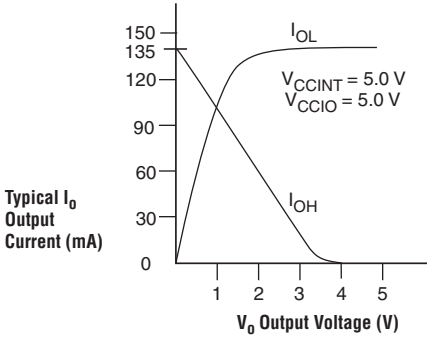
Programmable Current Drive Strength

The Cyclone II device I/O standards support various output current drive settings as shown in Table 10–6. These programmable drive-strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for I_{OH} and I_{OL} of the corresponding I/O standard.

Table 10–6. Programmable Drive Strength (Part 1 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
LVTTL (3.3 V)	4	4
	8	8
	12	12
	16	16
	20	20
	24	24
LVCMOS (3.3 V)	4	4
	8	8
	12	12
	16	—
	20	—
	24	—
LVTTL and LVCMOS (2.5 V)	4	4
	8	8
	12	—
	16	—
LVTTL and LVCMOS (1.8 V)	2	2
	4	4
	6	6
	8	8
	10	10
	12	12
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	—

Figure 10–22. Output Drive Characteristics of a 5.0-V Device



As shown above, R_1 = 5.0-V/135 mA.

The values shown in data sheets usually reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction when applied in the example in Figure 10–22 gives R_1 a value of 30 Ω

R_2 should be selected so that it does not violate the driving device's I_{OH} specification. For example, if the device has a maximum I_{OH} of 8 mA, given that the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$, and the maximum supply load of a 5.0-V device (V_{CC}) is 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 164\ \Omega$$

This analysis assumes worst case conditions. If your system does not have a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in Cyclone II devices requires use of the PCI clamp, and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

Conclusion

Cyclone II device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone II devices to fit into a wide variety of applications. The Quartus II

Altera programming hardware (APU) or other third-party programming hardware can be used to program blank serial configuration devices before they are mounted onto PCBs. Alternatively, you can use an on-board microprocessor to program the serial configuration device on the PCB using C-based software drivers provided by Altera (i.e., the SRunner software driver).

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming, which can be easily customized to fit in different embedded systems. SRunner can read a Raw Programming Data File (**.rpd**) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II Programmer.

For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming White Paper* and the source code on the Altera web site at www.altera.com. For more information on programming serial configuration devices, see the *Serial Configuration Devices Data Sheet* in the *Configuration Handbook*.

Figure 13–8 shows the timing waveform for the AS configuration scheme using a serial configuration device.

Figure 13–8. AS Configuration Timing

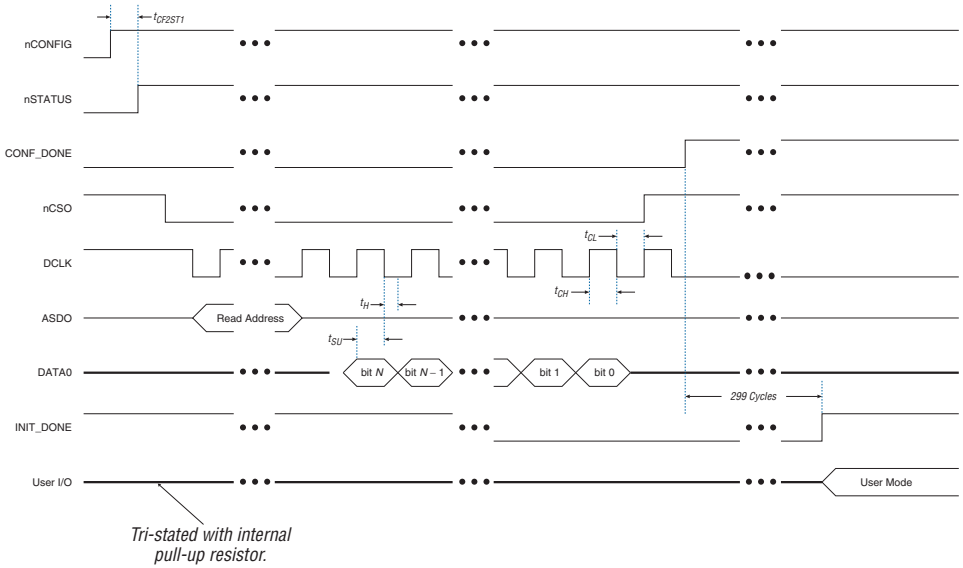
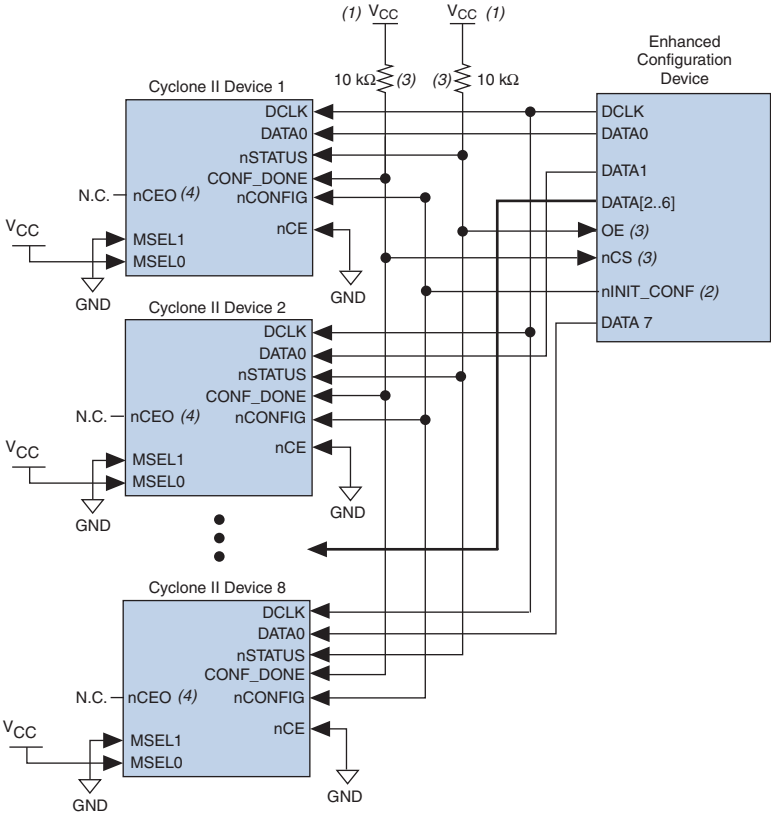


Figure 13–15. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device



Notes to Table 13–15:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

The Quartus II software only allows you to set *n* to 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. For example, if you configure three FPGAs, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding SOF data is transmitted from the configuration device to the FPGA. For

672-Pin FineLine BGA Package, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 15–17 and 15–18 show the package information and package outline figure references, respectively, for the 672-pin FineLine BGA package.

Table 15–17. 672-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–18. 672-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		