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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8q208c7

1. Introduction

CII51001-3.2

Introduction

Following the immensely successful first-generation Cyclone® device family, Altera® Cyclone II FPGAs extend the low-cost FPGA density range to 68,416 logic elements (LEs) and provide up to 622 usable I/O pins and up to 1.1 Mbits of embedded memory. Cyclone II FPGAs are manufactured on 300-mm wafers using TSMC's 90-nm low-k dielectric process to ensure rapid availability and low cost. By minimizing silicon area, Cyclone II devices can support complex digital systems on a single chip at a cost that rivals that of ASICs. Unlike other FPGA vendors who compromise power consumption and performance for low-cost, Altera's latest generation of low-cost FPGAs—Cyclone II FPGAs, offer 60% higher performance and half the power consumption of competing 90-nm FPGAs. The low cost and optimized feature set of Cyclone II FPGAs make them ideal solutions for a wide array of automotive, consumer, communications, video processing, test and measurement, and other end-market solutions. Reference designs, system diagrams, and IP, found at www.altera.com, are available to help you rapidly develop complete end-market solutions using Cyclone II FPGAs.

Low-Cost Embedded Processing Solutions

Cyclone II devices support the Nios II embedded processor which allows you to implement custom-fit embedded processing solutions. Cyclone II devices can also expand the peripheral set, memory, I/O, or performance of embedded processors. Single or multiple Nios II embedded processors can be designed into a Cyclone II device to provide additional co-processing power or even replace existing embedded processors in your system. Using Cyclone II and Nios II together allow for low-cost, high-performance embedded processing solutions, which allow you to extend your product's life cycle and improve time to market over standard product solutions.

Low-Cost DSP Solutions

Use Cyclone II FPGAs alone or as DSP co-processors to improve price-to-performance ratios for digital signal processing (DSP) applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II features and design support:

- Up to 150 18 × 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interfaces to external memory

Each M4K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and first-in first-out (FIFO) buffers. The M4K blocks support the following features:

- 4,608 RAM bits
- 250-MHz performance
- True dual-port memory
- Simple dual-port memory
- Single-port memory
- Byte enable
- Parity bits
- Shift register
- FIFO buffer
- ROM
- Various clock modes
- Address clock enable

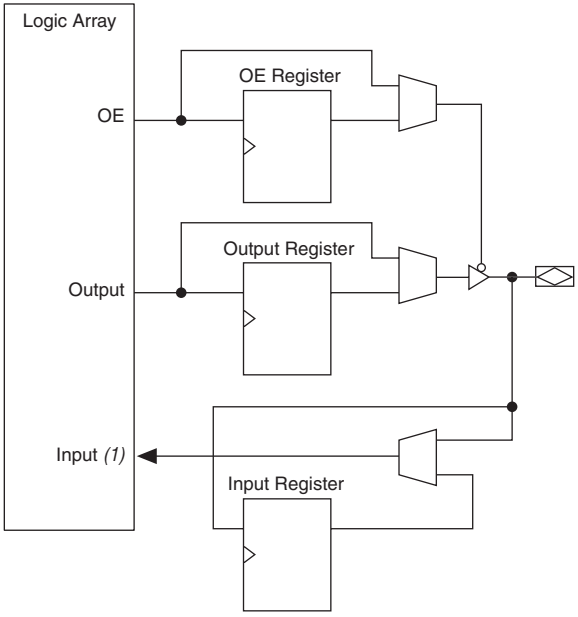
Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Table 2–5 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device.

Table 2–5. M4K Memory Capacity & Distribution in Cyclone II Devices

Device	M4K Columns	M4K Blocks	Total RAM Bits
EP2C5	2	26	119,808
EP2C8	2	36	165,888
EP2C15	2	52	239,616
EP2C20	2	52	239,616
EP2C35	3	105	483,840
EP2C50	3	129	594,432
EP2C70	5	250	1,152,000

Figure 2–20. Cyclone II IOE Structure



Note to Figure 2–20:

(1) There are two paths available for combinational or registered inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone II device. There are up to five IOEs per row I/O block and up to four IOEs per column I/O block (column I/O blocks span two columns). The row I/O blocks drive row, column (only C4 interconnects), or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–21 shows how a row I/O block connects to the logic array. Figure 2–22 shows how a column I/O block connects to the logic array.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI). Cyclone II devices support the RSDS and mini-LVDS I/O standards at data rates up to 311 Mbps at the transmitter.

A subset of pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. The dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry. Therefore, internal logic performs serialization and deserialization functions.

Cyclone II pin tables list the pins that support the high-speed I/O interface. The number of LVDS channels supported in each device family member is listed in Table 2–18.

Table 2–18. Cyclone II Device LVDS Channels (Part 1 of 2)

Device	Pin Count	Number of LVDS Channels *(1)*
EP2C5	144	31 (35)
	208	56 (60)
	256	61 (65)
EP2C8	144	29 (33)
	208	53 (57)
	256	75 (79)
EP2C15	256	52 (60)
	484	128 (136)
EP2C20	240	45 (53)
	256	52 (60)
	484	128 (136)
EP2C35	484	131 (139)
	672	201 (209)
EP2C50	484	119 (127)
	672	189 (197)

Document Revision History

Table 3–5 shows the revision history for this document.

Table 3–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section. • Updated "Cyclone II Automated Single Event Upset Detection" section.	• Added information about limitation of cascading multi devices in the same JTAG chain. • Corrected information on CRC calculation.
July 2005 v2.0	Updated technical content.	
February 2005 v1.2	Updated information on JTAG chain limitations.	
November 2004 v1.1	Updated Table 3–4.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–17. IOE Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TCOMBIN2PIN_C	1418	2622	1352	2831	1352	3041	ps
	—	—	1418	—	1418	—	ps
TCLR	137	—	165	—	165	—	ps
	—	—	151	—	165	—	ps
TPRE	192	—	233	—	233	—	ps
	—	—	212	—	233	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps

Notes to Table 5–17:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–18. DSP Block Internal Timing Microparameters (Part 1 of 2)

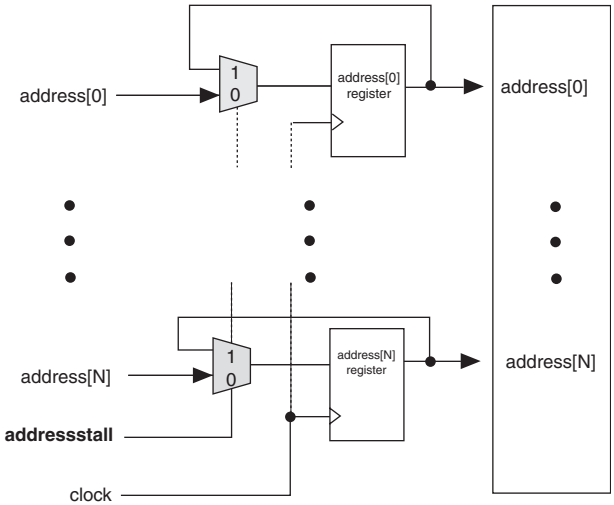
Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	47	—	62	—	62	—	ps
	—	—	54	—	62	—	ps
TH	110	—	113	—	113	—	ps
	—	—	111	—	113	—	ps
TCO	0	0	0	0	0	0	ps
	—	—	0	—	0	—	ps
TINREG2PIPE9	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps
TINREG2PIPE18	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_HSTL_CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.8V_HSTL_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_HSTL_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
LVDS	t_{PI}	623	653	1072	1075	1078	1078	ps
	t_{PCOUT}	409	429	610	630	650	650	ps
1.2V_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Figure 8–3 shows an address clock enable block diagram. The address register output is fed back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal. Address latching is enabled when the `addressstall` signal goes high (active high). The output of the address register is then continuously fed into the input of the register until the `addressstall` signal goes low.

Figure 8–3. Cyclone II Address Clock Enable Block Diagram



The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 8–4 and 8–5 show the address clock enable waveforms during the read and write cycles, respectively.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

Table 10–5. Cyclone II Regular I/O Standards Support

I/O Standard	I/O Banks for EP2C15, EP2C20, EP2C35, EP2C50 and EP2C70 Devices								I/O Banks for EP2C5 and EP2C8 Devices			
	1	2	3	4	5	6	7	8	1	2	3	4
LVTTL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
3.3-V PCI-X	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
SSTL-2 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.8-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.5-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
Pseudo-differential SSTL-2	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
Pseudo-differential SSTL-18	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.8-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.5-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
LVDS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RSDS and mini-LVDS	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
Differential LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*

Notes to Table 10–5:

(1) These I/O banks support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.

(2) Pseudo-differential I/O standards are only supported for clock inputs and dedicated `PLL_OUT` outputs. Refer to Table 10–1 for more information.

(3) This I/O standard is only supported for outputs.

(4) This I/O standard is only supported for the clock inputs.

I/O Driver Impedance Matching (R_S) and Series Termination (R_S)

Cyclone II devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 Ω When used with the output drivers, on-chip termination (OCT) sets the output driver impedance to 25 or 50 Ωby choosing the driver strength. Once matching impedance is selected, driver current can not be changed. Table 10–7 provides a list of output standards that support impedance matching. All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

Table 10–7. Selectable I/O Drivers with Impedance Matching and Series Termination

I/O Standard	Target R_S (Ω)
3.3-V LVTTL/CMOS	25 *(1)*
2.5-V LVTTL/CMOS	50 *(1)*
1.8-V LVTTL/CMOS	50 *(1)*
SSTL-2 class I	50 *(1)*
SSTL-18 class I	50 *(1)*

Note to Table 10–7:

(1) These RS values are nominal values. Actual impedance varies across process, voltage, and temperature conditions. Tolerance is specified in the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Handbook*.

Pad Placement and DC Guidelines

This section provides pad placement guidelines for the programmable I/O standards supported by Cyclone II devices and includes essential information for designing systems using the devices' selectable I/O capabilities. This section also discusses the DC limitations and guidelines.

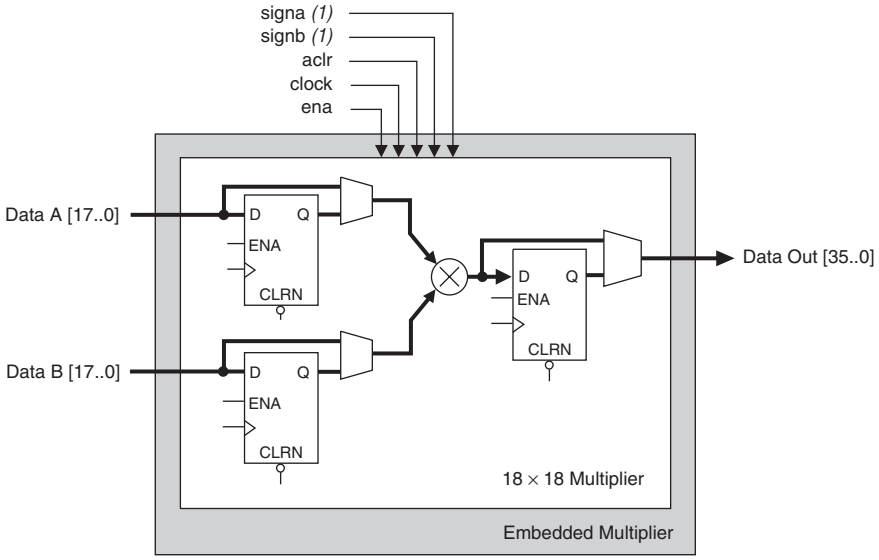
Quartus II software provides user controlled restriction relaxation options for some placement constraints. When a default restriction is relaxed by a user, the Quartus II fitter generates warnings.

For more information about how Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

18-Bit Multipliers

Each embedded multiplier can be configured to support a single 18 × 18 multiplier for input widths from 10- to 18-bits. Figure 12–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 12–3. 18-Bit Multiplier Mode



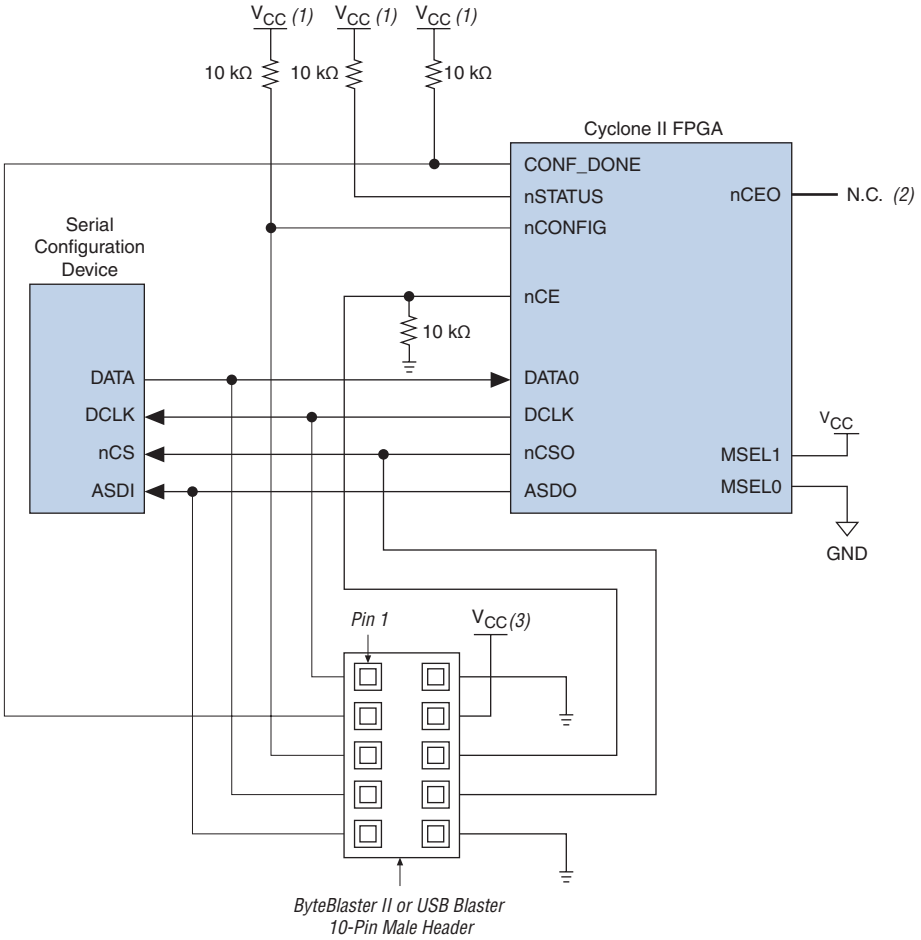
Note to Figure 12–3:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 18-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and can send these signals through dedicated input registers.

9-Bit Multipliers

Each embedded multiplier can also be configured to support two 9 × 9 independent multipliers for input widths up to 9-bits. Figure 12–4 shows the embedded multiplier configured to support two 9-bit multipliers.

Figure 13–7. In-System Programming of Serial Configuration Devices



Notes to Figure 13–7:

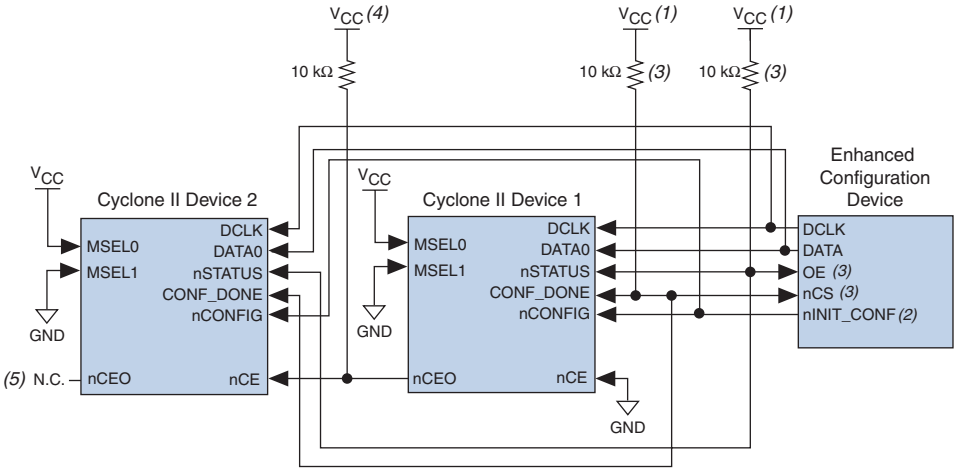
(1) Connect these pull-up resistors to 3.3-V supply.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(3) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with a 3.3-V supply.

You can use the Quartus II software with the APU and the appropriate configuration device programming adapter to program serial configuration devices. All serial configuration devices are offered in an 8-pin or 16-pin small outline integrated circuit (SOIC) package and can be programmed using the PLMSEPC-8 adapter.

Figure 13–14. Multiple Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 13–14:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You cannot cascade enhanced configuration devices (EPC16, EPC8, and EPC4 devices).

When configuring multiple devices, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multiple device configuration chains, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

When configuring multiple devices with the PS scheme, connect the first Cyclone II device's nCE pin to GND and connect its nCEO pin to the nCE pin of the Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin to the V_{CCIO} level when

operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

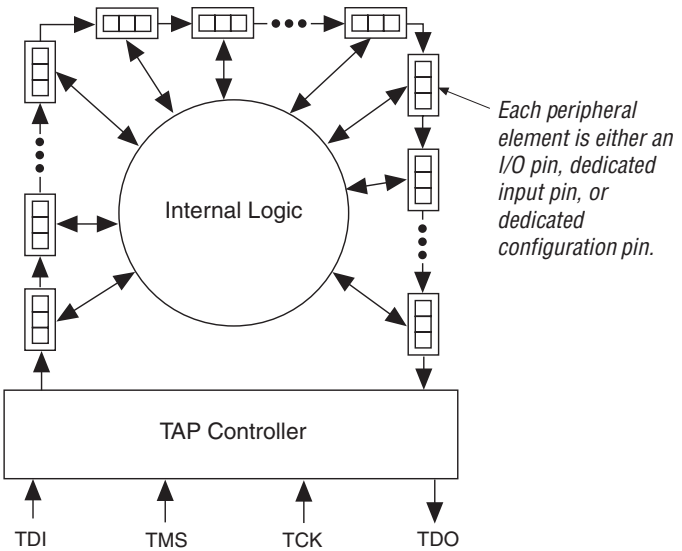
IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Cyclone II I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

See the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook* for the Cyclone II device boundary-scan register lengths.

Figure 14–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 14–3. Boundary-Scan Register

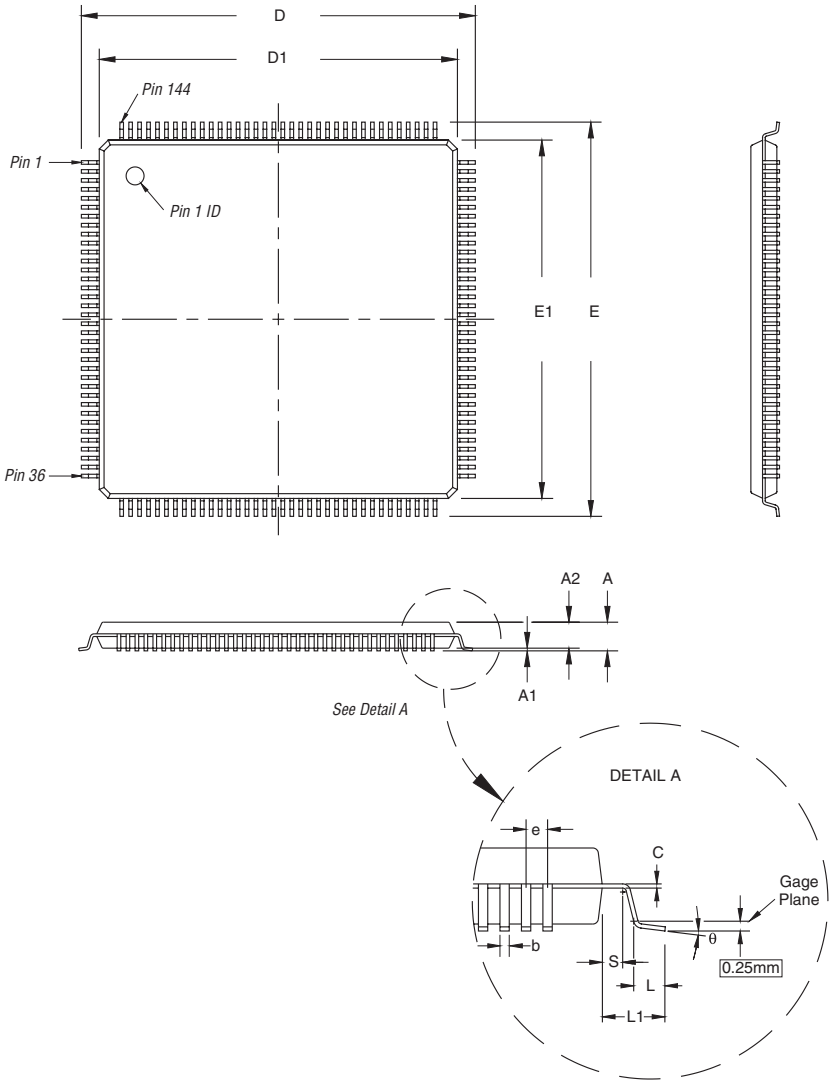


Boundary-Scan Cells of a Cyclone II Device I/O Pin

The Cyclone II device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ and OEJ signals, and connect

Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline



240-Pin Plastic Quad Flat Pack (PQFP)

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin 1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–9 and 15–10 show the package information and package outline figure references, respectively, for the 240-pin PQFP package.

Table 15–9. 240-Pin PQFP Package Information

Description	Specification
Ordering Code Reference	Q
Package Acronym	PQFP
Leadframe Material	Copper
Lead Finish (Plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-029 Variation: GA
Maximum Lead Coplanarity	0.003 inches (0.08mm)
Weight	7.0 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 1 of 2)

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	4.10
A1	0.25	–	0.50
A2	3.20	3.40	3.60
D	34.60 BSC		
D1	32.00 BSC		
E	34.60 BSC		
E1	32.00 BSC		
L	0.45	0.60	0.75
L1	1.30 REF		
S	0.20	–	–
b	0.17	–	0.27
c	0.09	–	0.20

Figure 15–7 shows a 672-pin FineLine BGA package outline.

Figure 15–7. 672-Pin FineLine BGA Package Outline