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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8q208c8

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI). Cyclone II devices support the RSDS and mini-LVDS I/O standards at data rates up to 311 Mbps at the transmitter.

A subset of pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. The dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry. Therefore, internal logic performs serialization and deserialization functions.

Cyclone II pin tables list the pins that support the high-speed I/O interface. The number of LVDS channels supported in each device family member is listed in Table 2–18.

Table 2–18. Cyclone II Device LVDS Channels (Part 1 of 2)

Device	Pin Count	Number of LVDS Channels *(1)*
EP2C5	144	31 (35)
	208	56 (60)
	256	61 (65)
EP2C8	144	29 (33)
	208	53 (57)
	256	75 (79)
EP2C15	256	52 (60)
	484	128 (136)
EP2C20	240	45 (53)
	256	52 (60)
	484	128 (136)
EP2C35	484	131 (139)
	672	201 (209)
EP2C50	484	119 (127)
	672	189 (197)

The Cyclone II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone II devices.

Table 3–2. Cyclone II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2C5	498
EP2C8	597
EP2C15	969
EP2C20	969
EP2C35	1,449
EP2C50	1,374
EP2C70	1,890

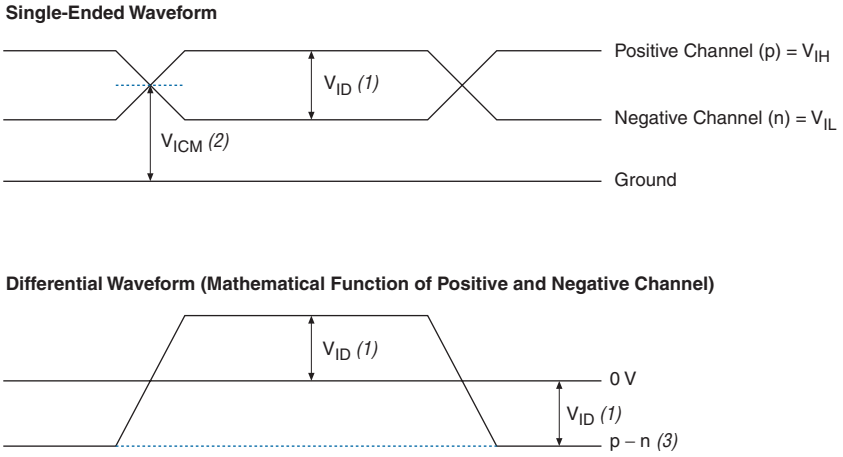
Table 3–3. 32-Bit Cyclone II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2C5	0000	0010 0000 1011 0001	000 0110 1110	1
EP2C8	0000	0010 0000 1011 0010	000 0110 1110	1
EP2C15	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C20	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C35	0000	0010 0000 1011 0100	000 0110 1110	1
EP2C50	0000	0010 0000 1011 0101	000 0110 1110	1
EP2C70	0000	0010 0000 1011 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

For more information on the Cyclone II JTAG specifications, refer to the *DC Characteristics & Timing Specifications* chapter in the *Cyclone II Device Handbook, Volume 1*.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

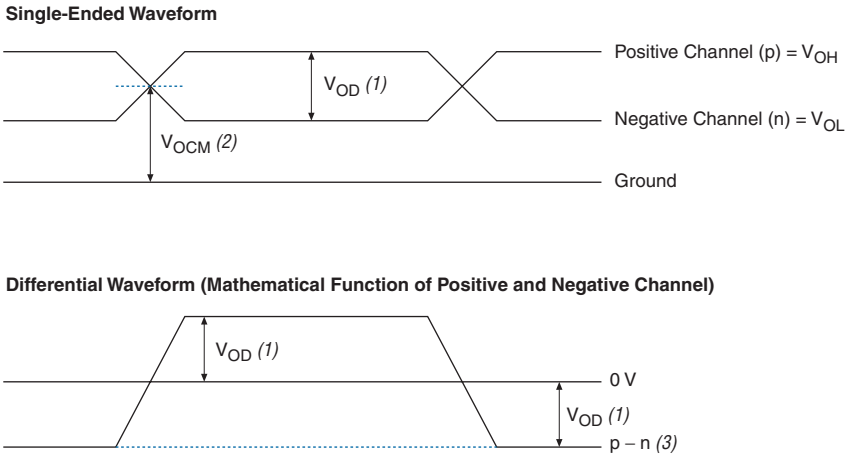
(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2:
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 5–14. Cyclone II Device Timing Model Status

Device	Speed Grade	Preliminary	Final
EP2C5/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C8/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C15A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C20/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C35	Commercial/Industrial	—	✓
EP2C50	Commercial/Industrial	—	✓
EP2C70	Commercial/Industrial	—	✓

Performance

Table 5–15 shows Cyclone II performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

Table 5–15. Cyclone II Performance (Part 1 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
LE	16-to-1 multiplexer *(1)*	21	0	0	385.35	313.97	270.85	286.04
	32-to-1 multiplexer *(1)*	38	0	0	294.2	260.75	228.78	191.02
	16-bit counter	16	0	0	401.6	349.4	310.65	310.65
	64-bit counter	64	0	0	157.15	137.98	126.08	126.27

ROM Mode

Cyclone II memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

A single clock or dual clock FIFO buffer may be implemented in the memory blocks. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. All FIFO memory configurations have synchronous inputs. However, the FIFO buffer outputs are always combinational (i.e., not registered). Simultaneous read and write from an empty FIFO buffer is not supported.

For more information on FIFO buffers, refer to the *Single- & Dual-Clock FIFO Megafunctions User Guide*.

Clock Modes

Depending on which memory mode is selected, the following clock modes are available:

- Independent
- Input/output
- Read/write
- Single-clock

Table 8–7 shows these clock modes supported by all memory blocks when configured in each respective memory modes.

Table 8–7. Cyclone II Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

Figure 10–13. 1.5-V HSTL Class I Termination

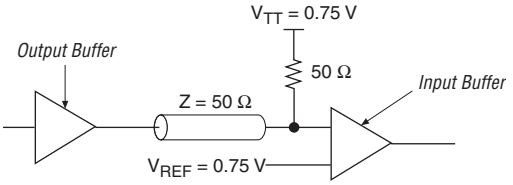
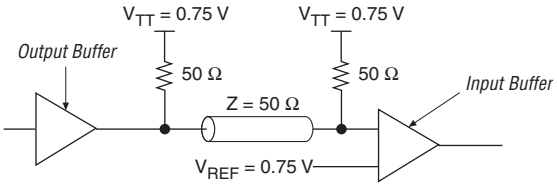


Figure 10–14. 1.5-V HSTL Class II Termination



1.5-V Pseudo-Differential HSTL Class I and II

The 1.5-V differential HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–15 and 10–16 for details on the 1.5-V differential HSTL termination.

Cyclone II devices do not support true 1.5-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Figure 10–15. 1.5-V Differential HSTL Class I Termination

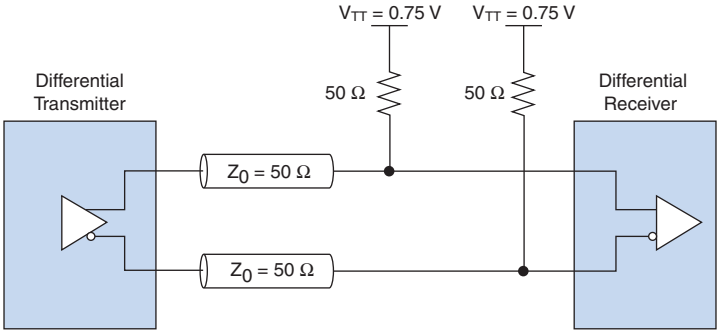
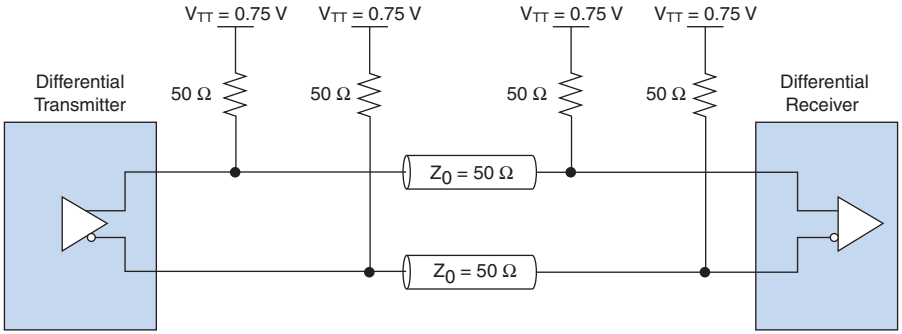


Figure 10–16. 1.5-V Differential HSTL Class II Termination



LVDS, RSDS and mini-LVDS

The LVDS standard is formulated under ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. Cyclone II devices are capable of running at a maximum data rate of 805 Mbps for input and 640 Mbps for output and still meet the ANSI/TIA/EIA-644 standard.

Because of the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS),

After applying the equation above, apply one of the equations in Table 10–11, depending on the package type.

Table 10–11. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤9 (per VCCIO/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤5 (per VCCIO/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (refer to Table 10–4 for more details) and compatible V_{REF} voltage levels.

DDR and QDR Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads have to be on the same power bank as DQS pads. With the DDR and DDR2 memory interfaces, a VCCIO and ground pair can have a maximum of five DQ pads.

For a QDR interface, D is the QDR output and Q is the QDR input. D pads and Q pads have to be on the same power bank as CQ. With the QDR and QDRII memory interfaces, a VCCIO and ground pair can have a maximum of five D and Q pads.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone II QDR and QDRII performance is not guaranteed.

DC Guidelines

There is a current limit of 240 mA per eight consecutive output top and bottom pins per power pair, as shown by the following equation:

$$\sum_{pin}^{pin+7} I_{PIN} < 240mA \text{ per power pair}$$

There is a current limit of 240 mA per 12 consecutive output side (left and right) pins per power pair, as shown by the following equation:

Table 10–12. Cyclone II I/O Standard DC Current Specification (Preliminary) (Part 2 of 2)

I/O Standard	I_{PIN} (mA)	
	Top and Bottom Banks	Side Banks
1.5-V differential HSTL class II *(3)*	16 *(4)*	
LVDS, RSDS and mini-LVDS	12	12

Notes to Table 10–12:

(1) The DC power specification of each I/O standard depends on the current sourcing and sinking capabilities of the I/O buffer programmed with that standard, as well as the load being driven. LVTTL and LVCMOS, and 2.5-, 1.8-, and 1.5-V outputs are not included in the static power calculations because they normally do not have resistor loads in real applications. The voltage swing is rail-to-rail with capacitive load only. There is no DC current in the system.

(2) This I_{PIN} value represents the DC current specification for the default current strength of the I/O standard. The I_{PIN} varies with programmable drive strength and is the same as the drive strength as set in Quartus II software. Refer to the *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook* for more information on the programmable drive strength feature of voltage referenced I/O standards.

(3) The current value obtained for differential HSTL and differential SSTL standards is per pin and not per differential pair, as opposed to the per-pair current value of LVDS standard.

(4) This I/O standard is only supported for clock input pins and `PLL_OUT` pins.

Table 10–12 only shows the limit on the static power consumed by an I/O standard. The amount of total power used at any moment could be much higher, and is based on the switching activities.

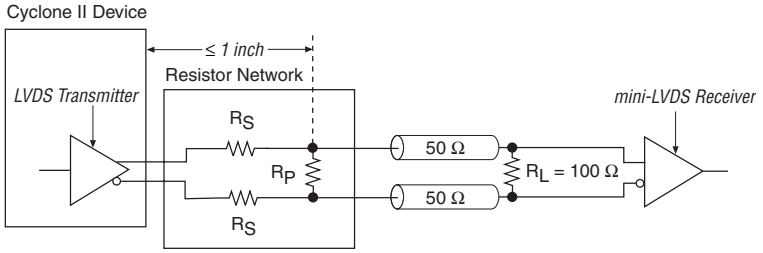
5.0-V Device Compatibility

A Cyclone II device may not correctly interoperate with a 5.0-V device if the output of the Cyclone II device is connected directly to the input of the 5.0-V device. If V_{OUT} of the Cyclone II device is greater than V_{CCIO}, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0-V.

A Cyclone II device can drive a 5.0-V LVTTL device by connecting the V_{CCIO} pins of the Cyclone II device to 3.3 V. This is because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4-V of a 5.0-V LVTTL device. (A Cyclone II device cannot drive a 5.0-V LVCMOS device.)

Because the Cyclone II devices are 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI and 64-bit 133-MHz PCI-X compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.1-V. To drive a Cyclone II device with a 5.0-V device, you must connect a resistor (R_2) between the Cyclone II device and the 5.0-V device. Refer to Figure 10–21.

Figure 11–10. mini-LVDS Resistor Network



Note to Figure 11–10:
(1) R_S = 120 Ω and R_P = 170 Ω

mini-LVDS Software Support

When designing for the mini-LVDS I/O standard, assign the mini-LVDS I/O standard to the I/O pins intended for mini-LVDS in the Quartus II software. Contact Altera Applications for reference designs.

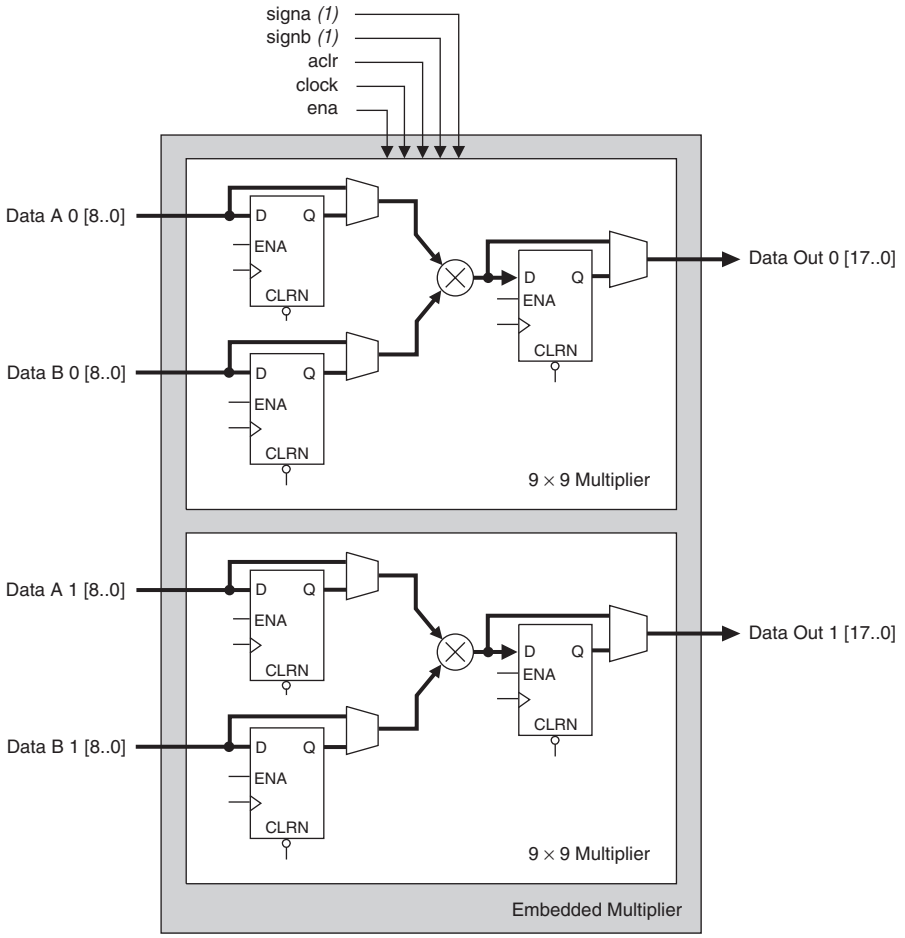
LVPECL Support in Cyclone II

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V V_{CCIO} and is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. Cyclone II devices support the LVPECL input standard at the clock input pins only. Table 11–4 shows the LVPECL electrical characteristics for Cyclone II devices. Figure 11–11 shows the LVPECL I/O interface.

Table 11–4. LVPECL Electrical Characteristics for Cyclone II Devices

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		3.135	3.3	3.465	V
V_{IH}	Input high voltage		2,100		2,880	mV
V_{IL}	Input low voltage		0		2,200	mV
V_{ID}	Differential input voltage	Peak to peak	100	600	950	mV

Figure 12–4. 9-Bit Multiplier Mode



Note to Figure 12–4:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 9-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Each embedded multiplier only has one `signa` signal to control the sign representation of both data A inputs (one for each 9 × 9 multiplier) and one `signb` signal to control the sign representation of both data B inputs. Therefore, all of the data A inputs feeding the same embedded multiplier must have the same sign representation. Similarly, all of the data B inputs feeding the same embedded multiplier must have the same sign representation.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone II devices read configuration data via the serial interface, decompress data if necessary, and configure their SRAM cells. The FPGA controls the configuration interface in the AS configuration scheme, while the external host (e.g., the configuration device or microprocessor) controls the interface in the PS configuration scheme.

The Cyclone II decompression feature is available when configuring your Cyclone II device using AS mode.

Table 13–4 shows the MSEL pin settings when using the AS configuration scheme.

Table 13–4. Cyclone II Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
AS (20 MHz)	0	0
Fast AS (40 MHz) *(1)*	1	0

Note to Table 13–4:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

Single Device AS Configuration

Serial configuration devices have a four-pin interface: serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS). This four-pin interface connects to Cyclone II device pins, as shown in Figure 13–3.

You should put a buffer before the DATA and DCLK output from the master Cyclone II device to avoid signal strength and signal integrity issues. The buffer should not significantly change the DATA-to-DCLK relationships or delay them with respect to other AS signals (ASDI and nCS). Also, the buffer should only drive the slave Cyclone II devices, so that the timing between the master Cyclone II device and serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed SOFs. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the SOF file used or you can select a larger serial configuration device.

Estimating AS Configuration Time

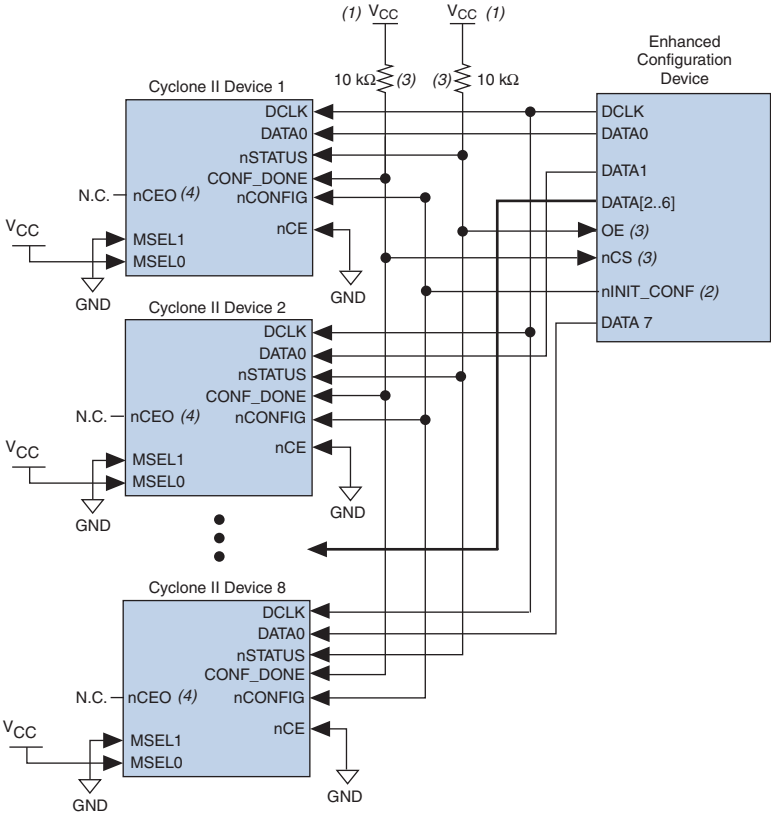
The AS configuration time is the time it takes to transfer data from the serial configuration device to the Cyclone II device. The Cyclone II DCLK output (generated from an internal oscillator) clocks this serial interface. As listed in Table 13–5, if you are using the 40-MHz oscillator, the DCLK minimum frequency is 20 MHz (50 ns). Therefore, the maximum configuration time estimate for an EP2C5 device (1,223,980 bits of uncompressed data) is:

RBF size × (maximum DCLK period / 1 bit per DCLK cycle) = estimated maximum configuration time

1,223,980 bits × (50 ns / 1 bit) = 61.2 ms

To estimate the typical configuration time, use the typical DCLK period listed in Table 13–5. With a typical DCLK period of 38.46 ns, the typical configuration time is 47.1 ms. Enabling compression reduces the amount of configuration data that is transmitted to the Cyclone II device, which also reduces configuration time. On average, compression reduces configuration time by 50%.

Figure 13–15. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device



Notes to Table 13–15:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

The Quartus II software only allows you to set *n* to 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. For example, if you configure three FPGAs, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding SOF data is transmitted from the configuration device to the FPGA. For

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

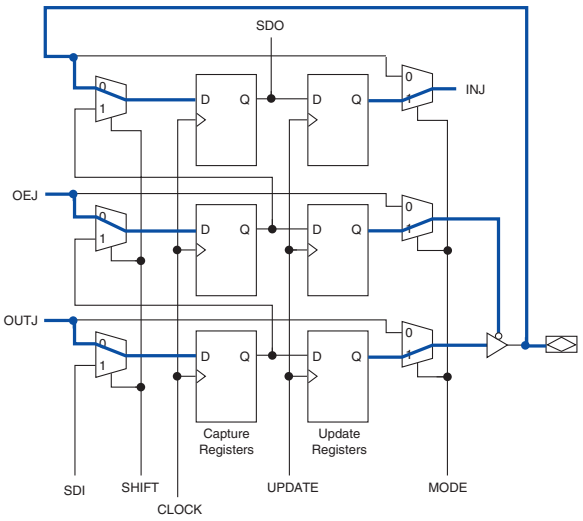
Figure 14–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 14–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_IN, INJ, and allows the I/O pin to tri-state or drive a signal out.

A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_IN, INJ, and allow the I/O pin to tri-state or drive a signal out.

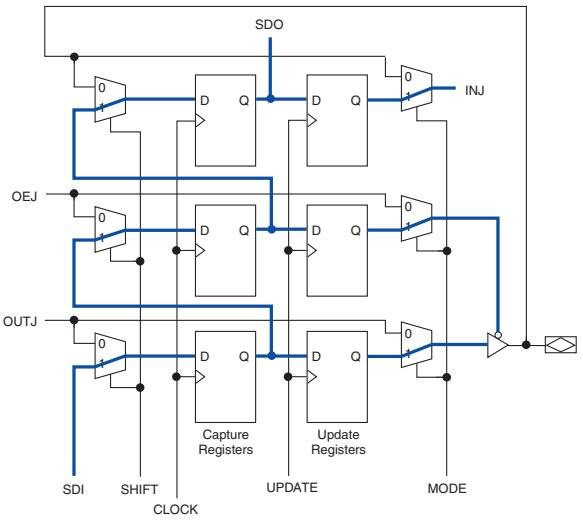


Table 15–4 provides θ_{JA} (junction-to-ambient thermal resistance) values, θ_{JC} (junction-to-case thermal resistance) values, θ_{JB} (junction-to-board thermal resistance) values for Cyclone II devices on a typical board.

Table 15–4. Thermal Resistance of Cyclone II Devices for Typical Board

Device	Pin Count	Package	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 100 ft./min.	θ_{JA} (°C/W) 200 ft./min.	θ_{JA} (°C/W) 400 ft./min.	θ_{JC} (°C/W)	θ_{JB} (°C/W)
EP2C5	256	FineLine BGA	30.2	25.8	22.9	20.6	8.7	14.8
EP2C8	256	FineLine BGA	27.9	23.2	20.5	18.4	7.1	12.3
EP2C15	256	FineLine BGA	24.7	20.1	17.5	15.3	5.5	9.1
	484	FineLine BGA	20.5	16.2	13.9	12.2	4.2	7.2
EP2C20	256	FineLine BGA	24.7	20.1	17.5	15.3	5.5	9.1
	484	FineLine BGA	20.5	16.2	13.9	12.2	4.2	7.2
EP2C35	484	FineLine BGA	18.8	14.5	12.3	10.6	3.3	5.7
	484	Ultra FineLine BGA	20	15.5	13.2	11.3	5	5.3
	672	FineLine BGA	17.4	13.3	11.3	9.8	3.1	5.5
EP2C50	484	FineLine BGA	17.7	13.5	11.4	9.8	2.8	4.5
	484	FineLine BGA	18.1	13.8	11.7	10.1	2.8	4.6
	484	Ultra FineLine BGA	19	14.6	12.3	10.6	4.4	4.4
	484	Ultra FineLine BGA	19.4	15	12.7	10.9	4.4	4.6
	672	FineLine BGA	16.5	12.4	10.5	9	2.6	4.6
EP2C70	672	FineLine BGA	15.7	11.7	9.8	8.3	2.2	3.8
	672	FineLine BGA	15.9	11.9	9.9	8.4	2.2	3.9
	896	FineLine BGA	14.6	10.7	8.9	7.6	2.1	3.7

Package Outlines

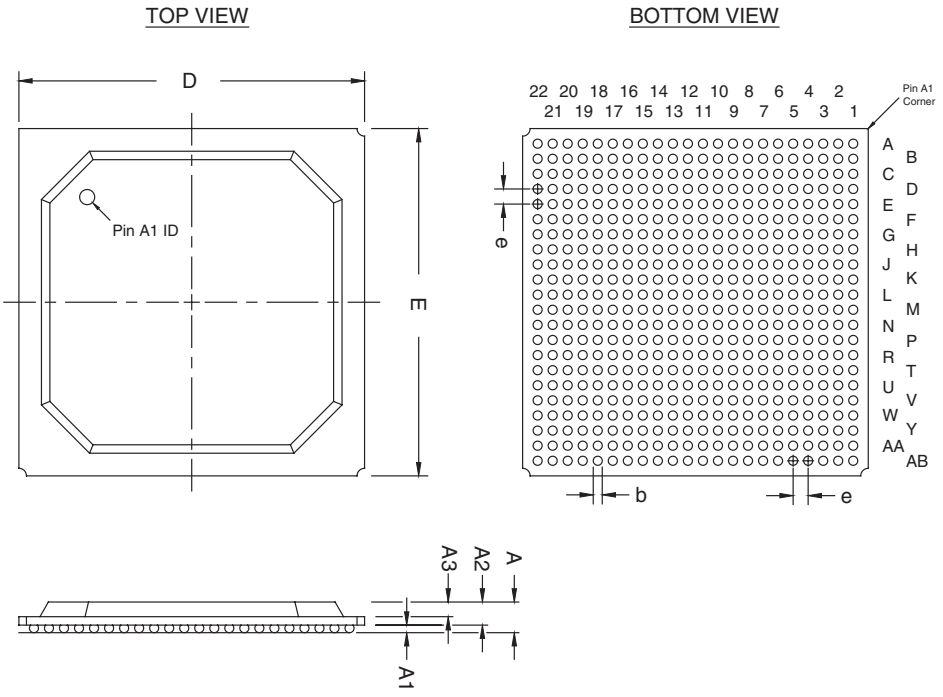
The package outlines on the following pages are listed in order of ascending pin count.

144-Pin Plastic Thin Quad Flat Pack (TQFP) – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin 1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Figure 15–5 shows a 484-pin FineLine BGA package outline.

Figure 15–5. 484-Pin FineLine BGA Package Outline



896-Pin FineLine BGA Package – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1's location may be indicated by an ID dot in its proximity on the package surface.

Tables 15–19 and 15–20 show the package information and package outline figure references, respectively, for the 896-pin FineLine BGA.

Table 15–19. 896-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn: 37Pb (typical) Pb-free: Sn: 3.0Ag: 0.5Cu (typical)
JEDEC outline reference	MS-034 variation AAN-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	11.5 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–20. 896-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	31.00 BSC		
E	31.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		