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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8q208i8

Table 2–1. Cyclone II Device Routing Scheme (Part 2 of 2)

Source	Destination												
	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	LE	M4K RAM Block	Embedded Multiplier	PLL	Column IOE	Row IOE
LE	✓	✓	✓	✓		✓							
M4K memory Block		✓	✓	✓		✓							
Embedded Multipliers		✓	✓	✓		✓							
PLL			✓	✓		✓							
Column IOE						✓	✓						
Row IOE			✓	✓	✓	✓							

Global Clock Network & Phase-Locked Loops

Cyclone II devices provide global clock networks and up to four PLLs for a complete clock management solution. Cyclone II clock network features include:

- Up to 16 global clock networks
- Up to four PLLs
- Global clock network dynamic clock source selection
- Global clock network dynamic enable and disable

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren , and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, wraddress , and wren . The read clock controls the data output, rdaddress , and rden .
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

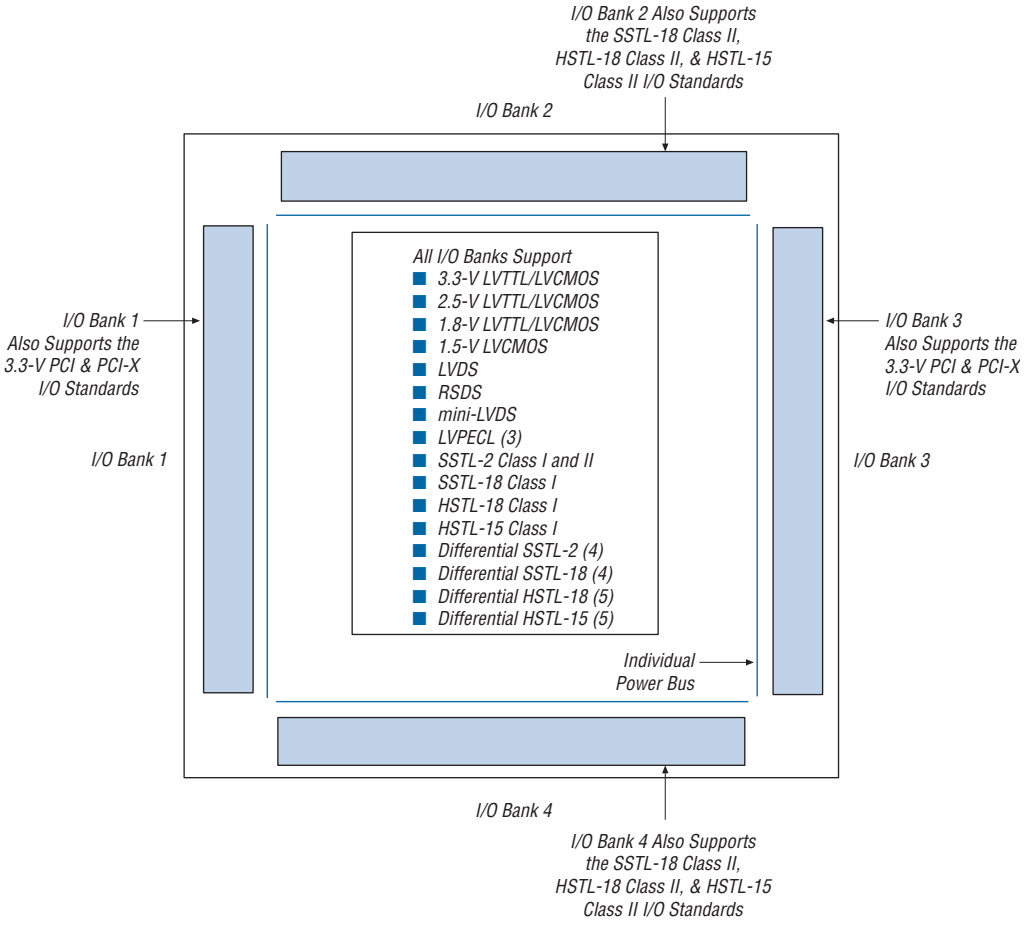
Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Figure 2–28. EP2C5 & EP2C8 I/O Banks *Notes (1), (2)*



Notes to Figure 2–28:

(1) This is a top view of the silicon die.
(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.
(5) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Table 5–8 shows the recommended operating conditions for user I/O pins with differential I/O standards.

Table 5–8. Recommended Operating Conditions for User I/O Pins Using Differential Signal I/O Standards

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			V_{ICM} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	2.375	2.5	2.625	0.1	—	0.65	0.1	—	2.0	—	—	—	—
Mini-LVDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
RSDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
LVPECL *(3) (6)*	3.135	3.3	3.465	0.1	0.6	0.95	—	—	—	0	2.2	2.1	2.88
Differential 1.5-V HSTL class I and II *(4)*	1.425	1.5	1.575	0.2	—	V_{CCIO} + 0.6	0.68	—	0.9	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential 1.8-V HSTL class I and II *(4)*	1.71	1.8	1.89	—	—	—	—	—	—	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential SSTL-2 class I and II *(5)*	2.375	2.5	2.625	0.36	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.35	V_{REF} + 0.35	—
Differential SSTL-18 class I and II *(5)*	1.7	1.8	1.9	0.25	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.25	V_{REF} + 0.25	—

Notes to Table 5–8:

(1) Refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook* for measurement conditions on V_{ID}.

(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

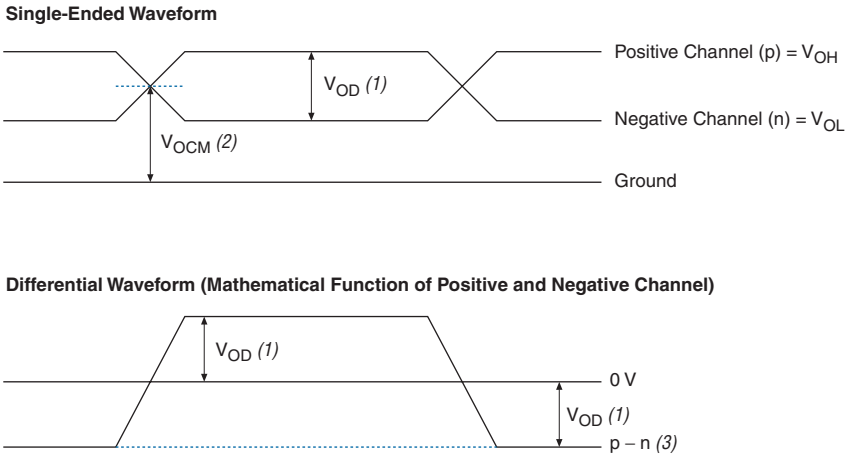
(4) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

(5) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(6) The LVPECL clock inputs are powered by V_{CCINT} and support all V_{CCIO} settings. However, it is recommended to connect V_{CCIO} to typical value of 3.3V.

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2:
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

Table 5–16. LE_FF Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPRE	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
tLUT	180	438	172	545	172	651	ps
	—	—	180	—	180	—	ps

Notes to Table 5–16:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–17. IOE Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	76	—	101	—	101	—	ps
	—	—	89	—	101	—	ps
TH	88	—	106	—	106	—	ps
	—	—	97	—	106	—	ps
TCO	99	155	95	171	95	187	ps
	—	—	99	—	99	—	ps
TPIN2COMBOUT_R	384	762	366	784	366	855	ps
	—	—	384	—	384	—	ps
TPIN2COMBOUT_C	385	760	367	783	367	854	ps
	—	—	385	—	385	—	ps
TCOMBIN2PIN_R	1344	2490	1280	2689	1280	2887	ps
	—	—	1344	—	1344	—	ps

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 3 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
SSTL_2_ CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
SSTL_2_ CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps
SSTL_18_ CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
SSTL_18_ CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps

Table 5–47. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. Sampling window is the sum of the setup time, hold time, and jitter. The window of t_{SU} + t_H is expected to be centered in the sampling window. SW = TUI – TCCS – (2 × RSKM)
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2
Input jitter (peak to peak)	—	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak to peak)	—	Peak-to-peak output jitter on high-speed PLLs.
Signal rise time	t_{RISE}	Low-to-high transmission time.
Signal fall time	t_{FALL}	High-to-low transmission time.
Lock time	t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Figure 5–3. High-Speed I/O Timing Diagram

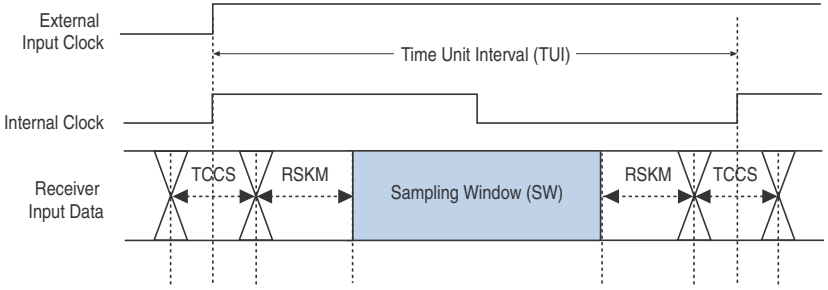
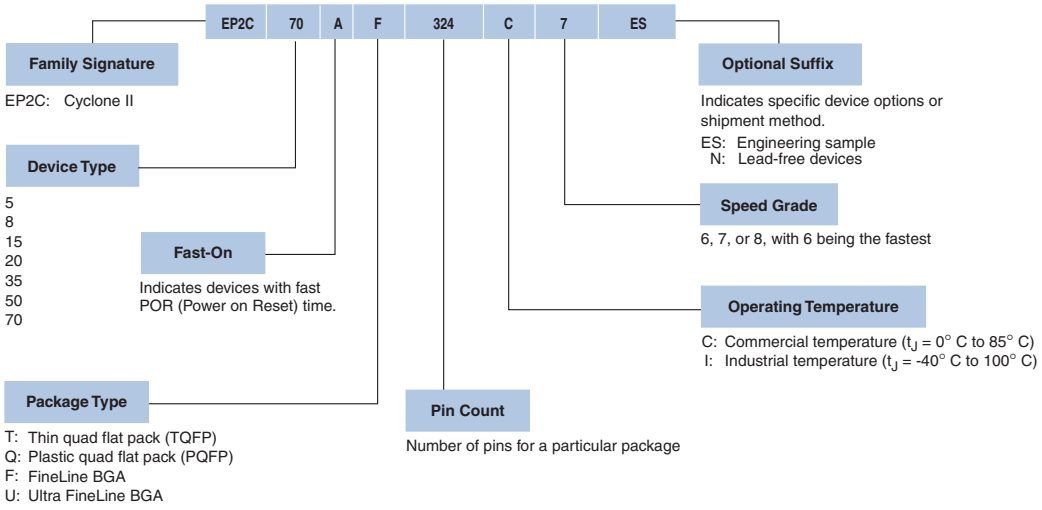


Figure 5–4 shows the high-speed I/O timing budget.

Figure 6–1. Cyclone II Device Packaging Ordering Information



Document Revision History

Table 6–1 shows the revision history for this document.

Table 6–1. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.5	Added document revision history. Updated Figure 6–1.	Added Ultra FineLine BGA detail in UBGA Package information in Figure 6–1.
November 2005 v1.2	Updated software introduction.	
November 2004 v1.1	Updated Figure 6–1.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

clock sources and the clkena signals for the global clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction.

clkena signals

In Cyclone II devices, the clkena signals are supported at the clock network level. Figure 7–14 shows how the clkena is implemented. This allows you to gate off the clock even when a PLL is not being used. Upon re-enabling the output clock, the PLL does not need a resynchronization or relock period because the clock is gated off at the clock network level. Also, the PLL can remain locked independent of the clkena signals since the loop-related counters are not affected.

Figure 7–14. clkena Implementation

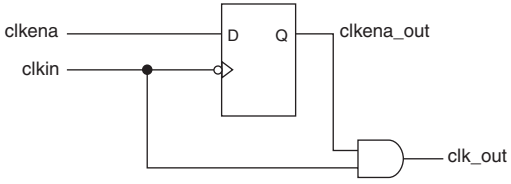


Figure 7–15 shows the waveform example for a clock output enable. clkena is synchronous to the falling edge of the clock (clkin).

This feature is useful for applications that require a low power or sleep mode. The exact amount of power saved when using this feature is pending device characterization.

Section III. Memory

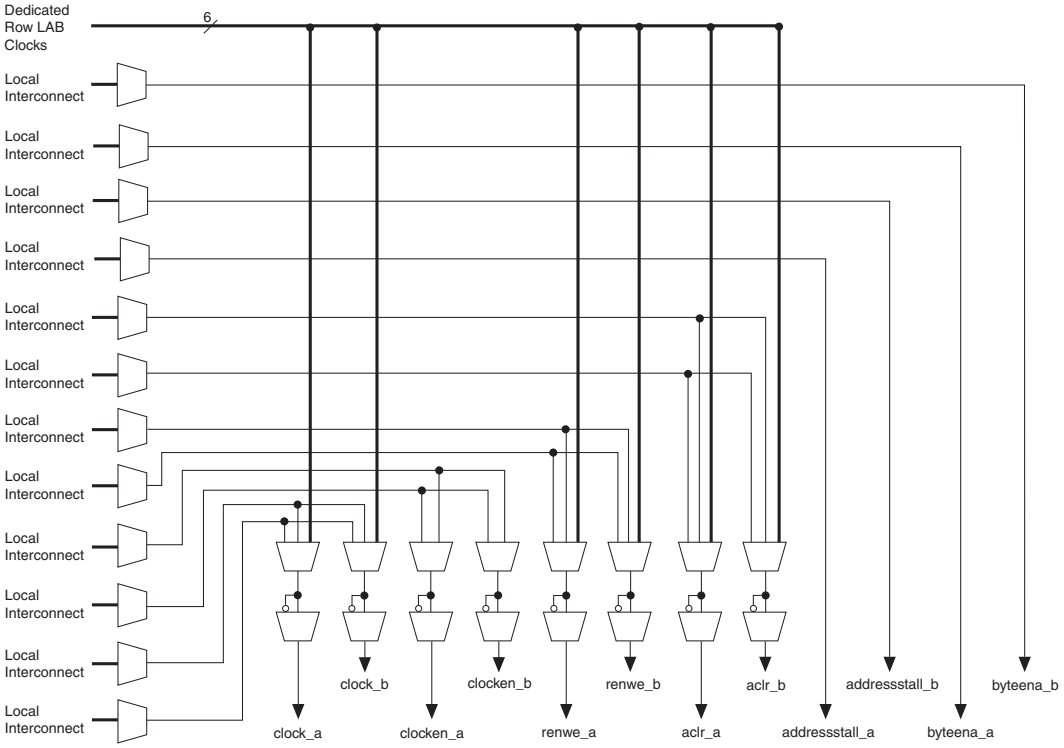
This section provides information on embedded memory blocks in Cyclone® II devices and the supported external memory interfaces.

This section includes the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

Refer to the *Using Parity to Detect Errors White Paper* for more information.

Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (wren) signals, along with the byte enable (byteena) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	Added document revision history. Updated "Packed Mode Support" section. Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

You can use any of the user I/O pins for commands and addresses. Because of the symmetrical setup and hold time for the command and address pins at the memory device, you may need to generate these signals from the negative edge of the system clock.

The clocks to the SDRAM device are called CK and CK#. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the t_{DQSS} requirements of the DDR SDRAM or DDR2 SDRAM device. The memory device's t_{DQSS} requires the positive edge of the write DQS signal to be within 25% of the positive edge of the DDR SDRAM and DDR2 SDRAM clock input. Because of strict skew requirements between CK and CK# signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and pins tied to ground for better noise immunity from other signals.

Read & Write Operation

When reading from the memory, DDR and DDR2 SDRAM devices send the data edge-aligned relative to the data strobe. To properly read the data, the data strobe must be center-aligned relative to the data inside the FPGA. Cyclone II devices feature clock delay control circuitry to shift the data strobe to the middle of the data window. Figure 9–1 shows an example of how the memory sends out the data and data strobe for a burst-of-two operation.

Section IV. I/O Standards

This section provides information on Cyclone® II single-ended, voltage referenced, and differential I/O standards.

This section includes the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Referenced Documents

This chapter references the following documents:

Altera Reliability Report
AN 75: High-Speed Board Designs
Cyclone II Architecture chapter in volume 1 of the *Cyclone II Device Handbook*
Cyclone II Device Family Data Sheet, *section 1* of the *Cyclone II Device Handbook*
DC Characteristics and Timing Specifications chapter in volume 1 of the *Cyclone II Device Handbook*
External Memory Interfaces chapter in volume 1 of the *Cyclone II Device Handbook*
High Speed Differential Interfaces in Cyclone II Devices chapter in volume 1 of the *Cyclone II Device Handbook*
Hot Socketing & Power-On Reset chapter in volume 1 of the *Cyclone II Device Handbook*
I/O Management chapter in volume 2 of the *Quartus II Handbook*

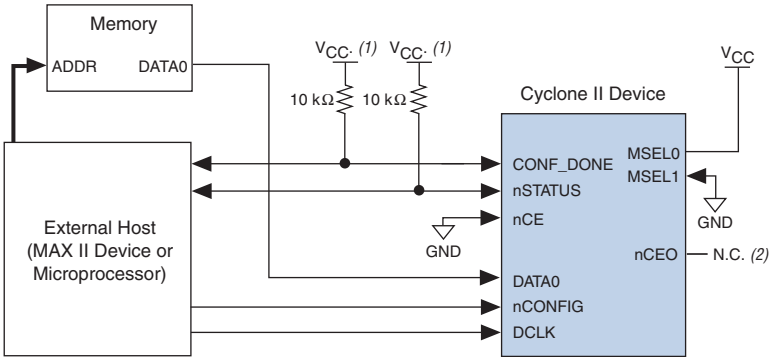
Document Revision History

Table 10–13 shows the revision history for this document.

Table 10–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Added "Referenced Documents" section. Updated "Differential Pad Placement Guidelines" section.	—
February 2007 v2.3	Added document revision history. Updated "Introduction" and its feetpara note. Updated *Note (2)* in Table 10–4. Updated "Differential LVPECL" section. Updated "Differential Pad Placement Guidelines" section. Updated "Output Pads" section. Added new section "5.0-V Device Compatibility" with two new figures.	Added reference detail for ESD specifications. Added information about differential placement restrictions applying only to pins in the same bank. Added information that Cyclone II device supports LVDS on clock inputs at 3.3V V_{CCIO}. Added more information on DC placement guidelines. Added information stating SSTL and HSTL outputs can be closer than 2 pads from V_{REF}. Added 5.0 Device tolerence solution.

Figure 13–9. Single Device PS Configuration Using an External Host



Notes to Figure 13–9:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} should be high enough to meet the VIH specification of the I/O on the device and the external host.

(2) The nCEOpin can be left unconnected or used as a user I/O pin when it does not feed other device's nCEpin.

Upon power-up, the Cyclone II device goes through a POR, which lasts approximately 100 ms. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the FPGA successfully exits POR, all user I/O pins continue to be tri-stated.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration can be found in the *Cyclone II Device Handbook*.

The configuration cycle consists of three stages: reset, configuration, and initialization.

Reset Stage

While the Cyclone II device's nCONFIGor nSTATUSpins are low, the device is in reset. To initiate configuration, the MAX II device must transition the Cyclone II nCONFIGpin from low to high.

V_{CCINT} and V_{CCIO} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When the Cyclone II nCONFIGpin transitions high, the Cyclone II device comes out of reset and releases the open-drain nSTATUSpin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUSis released, the FPGA is ready to receive configuration data and the MAX II device can start the configuration at any time.

You must connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. You should buffer the DCLK and DATA lines for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

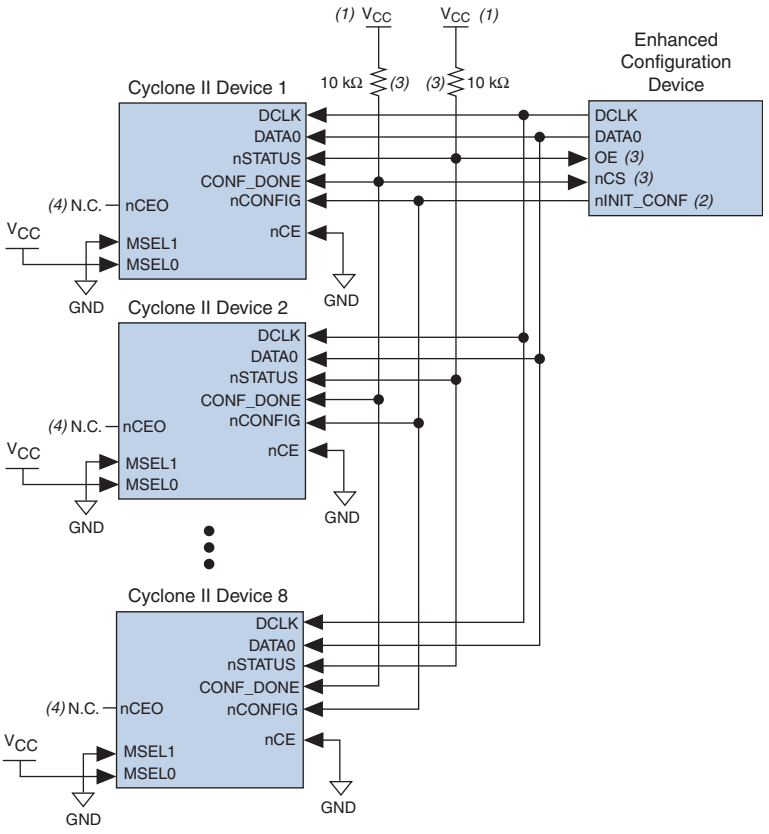
Since all nSTATUS and CONF_DONE pins are connected, if any Cyclone II device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first Cyclone II detects an error, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single Cyclone II device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the Cyclone II devices release their nSTATUS pins after a reset time-out period (maximum of 40 µs). After all nSTATUS pins are released and pulled high, the MAX II device reconfigures the chain without pulsing nCONFIG low. If the **Auto-restart configuration after error** option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

Figure 13–16. Multiple Device PS Configuration Using an Enhanced Configuration Device When FPGAs Receive the Same Data



Notes to Figure 13–16:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIGline. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OEand nCSpins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEOpin can be left unconnected or used as a user I/O pin when it does not feed other device's nCEpin.

You can cascade several EPC2 or EPC1 devices to configure multiple Cyclone II devices. The first configuration device in the chain is the master configuration device, and the subsequent devices are the slave devices. The master configuration device sends DCLKto the Cyclone II