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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8q208i8n

Section I. Cyclone II Device Family Data Sheet

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

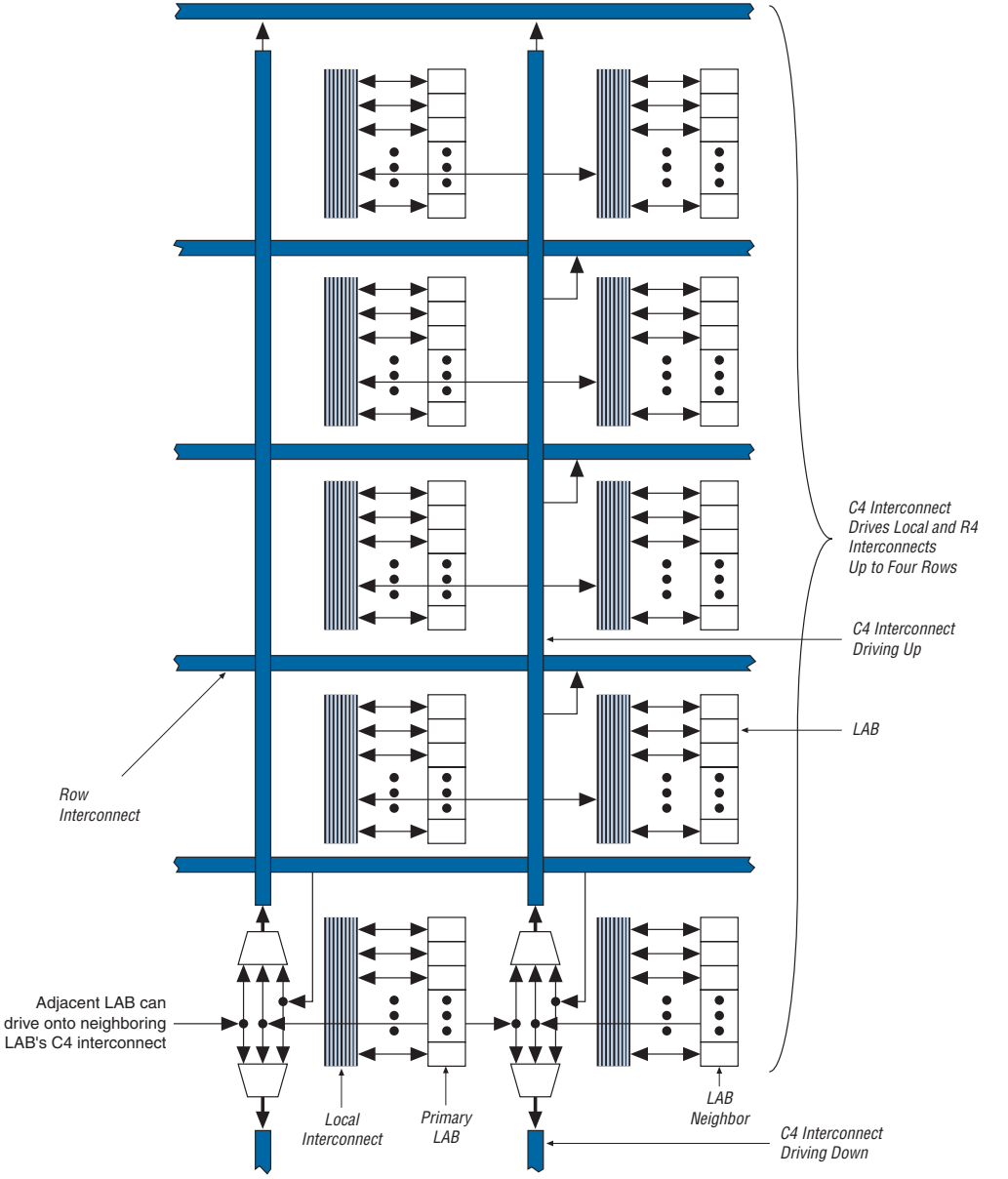
This section includes the following chapters:

- Chapter 1. Introduction
- Chapter 2. Cyclone II Architecture
- Chapter 3. Configuration & Testing
- Chapter 4. Hot Socketing & Power-On Reset
- Chapter 5. DC Characteristics and Timing Specifications
- Chapter 6. Reference & Ordering Information

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 2–10. C4 Interconnect Connections *Note (1)*



Note to Figure 2–10:
(1) Each C4 interconnect can drive either up or down four rows.

Slew Rate Control

Slew rate control is performed by using programmable output drive strength.

Bus Hold

Each Cyclone II device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus hold circuitry is not available on the dedicated clock pins.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to pull the signal level to the last-driven state. Refer to the *DC Characteristics & Timing Specifications* chapter in Volume 1 of the *Cyclone II Device Handbook* for the specific sustaining current for each V_{CCIO} voltage level driven through the resistor and overdrive current used to identify the next driven input level.

Programmable Pull-Up Resistor

Each Cyclone II device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank.

If the programmable pull-up is enabled, the device cannot use the bus-hold feature. The programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

Table 2–18. Cyclone II Device LVDS Channels (Part 2 of 2)		
Device	**Pin Count**	**Number of LVDS Channels** *(1)*
EP2C70	672	160 (168)
	896	257 (265)

Note to Table 2–18:
(1) The first number represents the number of bidirectional I/O pins which can be used as inputs or outputs. The number in parenthesis includes dedicated clock input pin pairs which can only be used as inputs.

You can use I/O pins and internal logic to implement a high-speed I/O receiver and transmitter in Cyclone II devices. Cyclone II devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal PLLs, and IOEs are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

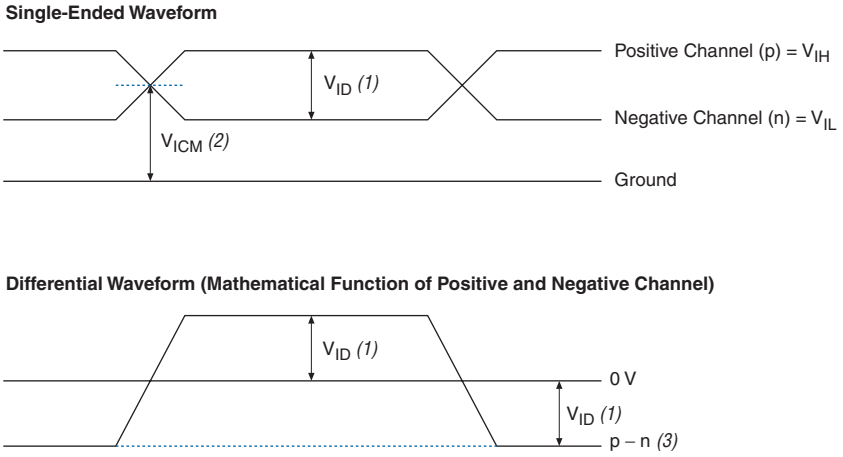
The maximum internal clock frequency for a receiver and for a transmitter is 402.5 MHz. The maximum input data rate of 805 Mbps and the maximum output data rate of 640 Mbps is only achieved when DDIO registers are used. The LVDS standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side.

For more information on Cyclone II differential I/O interfaces, see the *High-Speed Differential Interfaces in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Series On-Chip Termination

On-chip termination helps to prevent reflections and maintain signal integrity. This also minimizes the need for external resistors in high pin count ball grid array (BGA) packages. Cyclone II devices provide I/O driver on-chip impedance matching and on-chip series termination for single-ended outputs and bidirectional pins.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins Notes (1), (2) (Part 2 of 2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2669	0	4482	0	4834	0	4859	ps
			0	2802	—	—	0	4671	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	308	0	572	0	648	0	682	ps
			0	324	—	—	0	626	—	—	ps

Notes to Table 5–37 :

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Default Capacitive Loading of Different I/O Standards

Refer to Table 5–38 for default capacitive loading of different I/O standards.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5V	0	pF
1.8V	0	pF
1.5V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL_2_CLASS_I	0	pF
SSTL_2_CLASS_II	0	pF
SSTL_18_CLASS_I	0	pF

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 2 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
2.5V	4 mA	t_{OP}	1208	1267	2478	2614	2743	2750	ps
		t_{DIP}	1340	1406	2648	2808	2969	2969	ps
	8 mA	t_{OP}	1190	1248	2307	2434	2554	2561	ps
		t_{DIP}	1322	1387	2477	2628	2780	2780	ps
	12 mA	t_{OP}	1154	1210	2192	2314	2430	2437	ps
		t_{DIP}	1286	1349	2362	2508	2656	2656	ps
	16 mA (1)	t_{OP}	1140	1195	2152	2263	2375	2382	ps
		t_{DIP}	1272	1334	2322	2457	2601	2601	ps
1.8V	2 mA	t_{OP}	1682	1765	3988	4279	4563	4570	ps
		t_{DIP}	1814	1904	4158	4473	4789	4789	ps
	4 mA	t_{OP}	1567	1644	3301	3538	3768	3775	ps
		t_{DIP}	1699	1783	3471	3732	3994	3994	ps
	6 mA	t_{OP}	1475	1547	2993	3195	3391	3398	ps
		t_{DIP}	1607	1686	3163	3389	3617	3617	ps
	8 mA	t_{OP}	1451	1522	2882	3074	3259	3266	ps
		t_{DIP}	1583	1661	3052	3268	3485	3485	ps
	10 mA	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
	12 mA (1)	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
1.5V	2 mA	t_{OP}	2083	2186	4477	4870	5256	5263	ps
		t_{DIP}	2215	2325	4647	5064	5482	5482	ps
	4 mA	t_{OP}	1793	1881	3649	3965	4274	4281	ps
		t_{DIP}	1925	2020	3819	4159	4500	4500	ps
	6 mA	t_{OP}	1770	1857	3527	3823	4112	4119	ps
		t_{DIP}	1902	1996	3697	4017	4338	4338	ps
	8 mA (1)	t_{OP}	1703	1787	3537	3827	4111	4118	ps
		t_{DIP}	1835	1926	3707	4021	4337	4337	ps

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVCMOS	4 mA	250	210	170	250	210	170	250	210	170
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	310	260	210	310	260	210	310	260	210
	16 mA	320	270	220	—	—	—	—	—	—
	20 mA	350	290	240	—	—	—	—	—	—
	24 mA	370	310	250	—	—	—	—	—	—
2.5V	4 mA	180	150	120	180	150	120	180	150	120
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	440	370	300	—	—	—	—	—	—
	16 mA	450	405	350	—	—	—	—	—	—
1.8V	2 mA	120	100	80	120	100	80	120	100	80
	4 mA	180	150	120	180	150	120	180	150	120
	6 mA	220	180	150	220	180	150	220	180	150
	8 mA	240	200	160	240	200	160	240	200	160
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	350	290	240	350	290	240	350	290	240
1.5V	2 mA	80	60	50	80	60	50	80	60	50
	4 mA	130	110	90	130	110	90	130	110	90
	6 mA	180	150	120	180	150	120	180	150	120
	8 mA	230	190	160	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—

Table 8–1. Summary of M4K Memory Features (Part 2 of 2)	
Feature	**M4K Blocks**
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓
Embedded shift register mode *(2)*	✓
ROM mode	✓
FIFO buffer *(2)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support	✓
Memory Initialization File (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register clears	Output registers only
Same-port read-during-write	New data available at positive clock edge
Mixed-port read-during-write	Old data available at positive clock edge

Notes to Table 8–1:
(1) Maximum performance information is preliminary until device characterization.
(2) FIFO buffers and embedded shift registers require external logic elements (LEs) for implementing control logic.

Table 8–2 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device family member.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 1 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C5	26	119,808
EP2C8	36	165,888
EP2C15	52	239,616
EP2C20	52	239,616
EP2C35	105	483,840

Figure 8–4. Cyclone II Address Clock Enable During Read Cycle Waveform

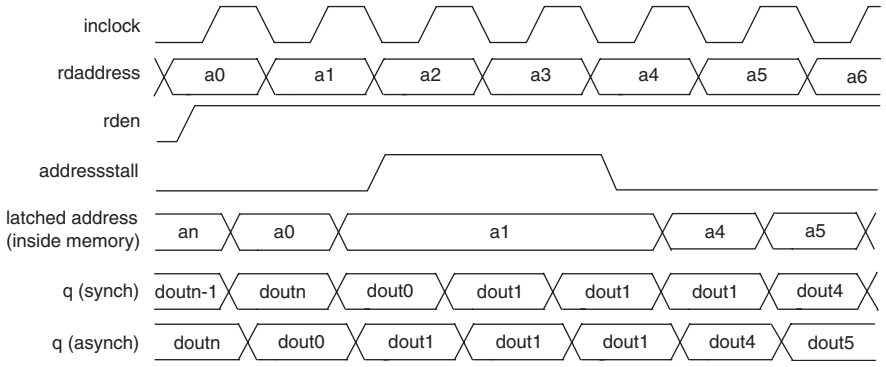
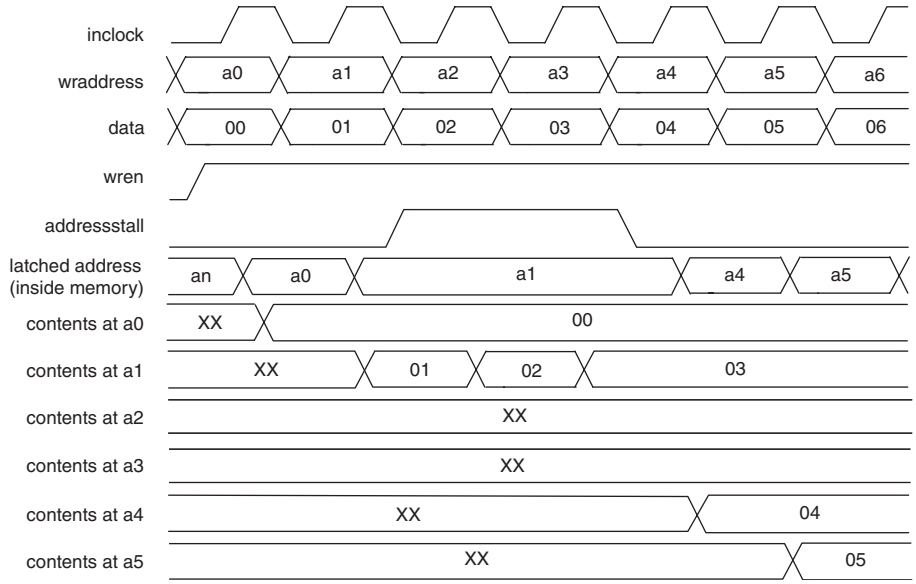


Figure 8–5. Cyclone II Address Clock Enable During Write Cycle Waveform



Memory Modes

Cyclone II M4K memory blocks include input registers that synchronize writes and output registers to pipeline data, thereby improving system performance. All M4K memory blocks are fully synchronous, meaning that you must send all inputs through a register, but you can either send outputs through a register (pipelined) or bypass the register (flow-through).

Single-Clock Mode

Cyclone II memory blocks support single-clock mode for true dual-port, simple dual-port, and single-port memory. In this mode, a single clock, together with a clock enable, controls all registers of the memory block. This mode does not support asynchronous clear signals for the registers. Figures 8–18 through 8–20 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by –90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

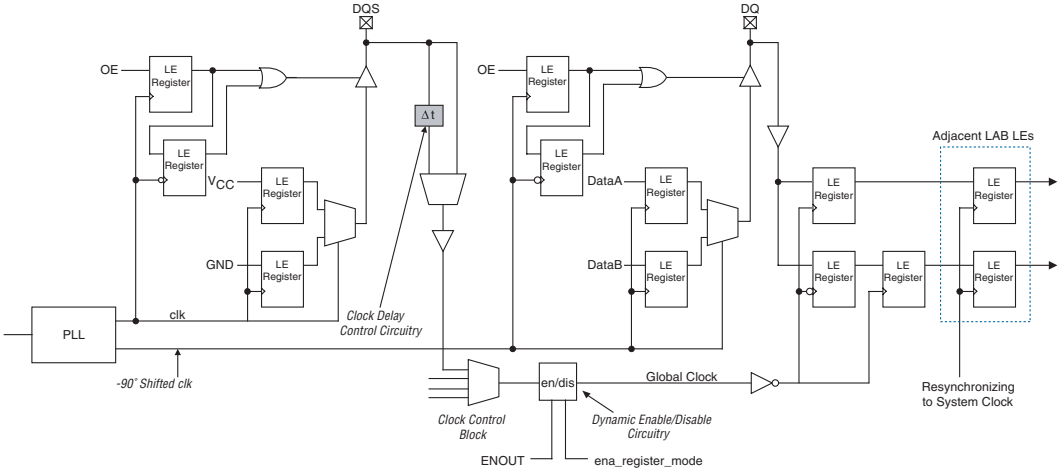


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only goes through routing delays from the DQ pin to the DQ LE registers. The delay from

10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

Figure 10–13. 1.5-V HSTL Class I Termination

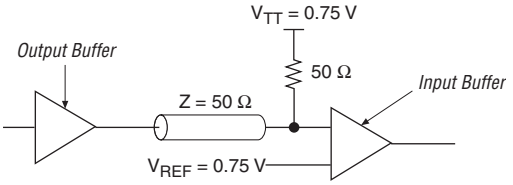
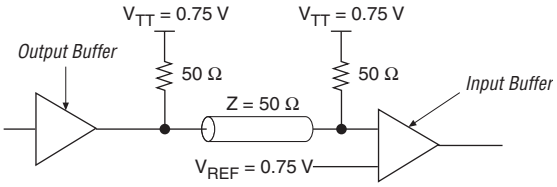


Figure 10–14. 1.5-V HSTL Class II Termination



1.5-V Pseudo-Differential HSTL Class I and II

The 1.5-V differential HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–15 and 10–16 for details on the 1.5-V differential HSTL termination.

Cyclone II devices do not support true 1.5-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Referenced Documents

This chapter references the following documents:

- *Altera Reliability Report*
- *AN 75: High-Speed Board Designs*
- *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Cyclone II Device Family Data Sheet*, *section 1* of the *Cyclone II Device Handbook*
- *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*
- *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 10–13 shows the revision history for this document.

Table 10–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v2.4	• Added "Referenced Documents" section. • Updated "Differential Pad Placement Guidelines" section.	—
February 2007 v2.3	• Added document revision history. • Updated "Introduction" and its feetpara note. • Updated *Note (2)* in Table 10–4. • Updated "Differential LVPECL" section. • Updated "Differential Pad Placement Guidelines" section. • Updated "Output Pads" section. • Added new section "5.0-V Device Compatibility" with two new figures.	• Added reference detail for ESD specifications. • Added information about differential placement restrictions applying only to pins in the same bank. • Added information that Cyclone II device supports LVDS on clock inputs at 3.3V V_{CCIO}. • Added more information on DC placement guidelines. • Added information stating SSTL and HSTL outputs can be closer than 2 pads from V_{REF}. • Added 5.0 Device tolerence solution.

data A signal through a register and send the data B signal directly to the multiplier). The following control signals are available to each register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, or asynchronous clear signal.

Multiplier Stage

The multiplier stage supports 9 × 9 or 18 × 18 multipliers as well as other smaller multipliers in between these configurations. See "Operational Modes" on page 12–6 for details. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel.

Each multiplier operand can be a unique signed or unsigned number. Two signals, `signa` and `signb`, control whether a multiplier's input is a signed or unsigned value. If the `signa` signal is high, the data A operand is a signed number, and if the `signa` signal is low, the data A operand is an unsigned number. Table 12–3 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 12–3. Multiplier Sign Representation

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

There is only one `signa` and one `signb` signal for each embedded multiplier. The `signa` and `signb` signals can be changed dynamically to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision regardless of the sign representation.

All information in the "Single Device PS Configuration Using a MAX II Device as an External Host" on page 13–22 section is also applicable when using a microprocessor as an external host. Refer to that section for all configuration information.

The MicroBlaster™ software driver allows you to configure Altera FPGAs, including Cyclone II devices, through the ByteBlaster II or ByteBlasterMV cable in PS mode. The MicroBlaster software driver supports a RBF programming input file and is targeted for embedded PS configuration. The source code is developed for the Windows NT operating system, although you can customize it to run on other operating systems.

Since the Cyclone II device can decompress the compressed configuration data on-the-fly during PS configuration, the MicroBlaster software can accept a compressed RBF file as its input file.

For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* and source files on the Altera web site at **www.altera.com**.

If you turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software, the Cyclone II devices does not enter user mode after the MicroBlaster has transmitted all the configuration data in the RBF file. You need to supply enough initialization clock cycles to `CLKUSR` pin to enter user mode.

Single Device PS Configuration Using a Configuration Device

You can use an Altera configuration device (for example, an EPC2, EPC1, or enhanced configuration device) to configure Cyclone II devices using a serial configuration bitstream. Configuration data is stored in the configuration device. Figure 13–13 shows the configuration interface connections between the Cyclone II device and a configuration device.

The figures in this chapter only show the configuration-related pins and the configuration pin connections between the configuration device and the FPGA.

For more information on enhanced configuration devices and flash interface pins (e.g., `PGM[2..0]`, `EXCLK`, `PORSEL`, `A[20..0]`, and `DQ[15..0]`), see the *Enhanced Configuration Devices (EPC4, EPC8 & EPC16) Data Sheet*.

A device operating in JTAG mode uses the TDI, TDO, TMS, and TCK pins. The TCK pin has a weak internal pull-down resistor while the other JTAG input pins, TDI and TMS, have weak internal pull-up resistors. All user I/O pins are tri-stated during JTAG configuration. Table 13–9 explains each JTAG pin's function.

Table 13–9. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.

The TDO output is powered by the V_{CCIO} power supply. If V_{CCIO} is tied to 3.3-V, both the I/O pins and the JTAG TDO port drive at 3.3-V levels.

If you are testing the device after configuring it, the programmable weak pull-up resister or the bus hold feature overrides the CLAMP value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The HIGHZ instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.

I/O Voltage Support in JTAG Chain

A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone II devices, the TDO pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone II devices can support 2.5- or 3.3-V input levels.

For more information on MultiVolt I/O support, see the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook*.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 14–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.