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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

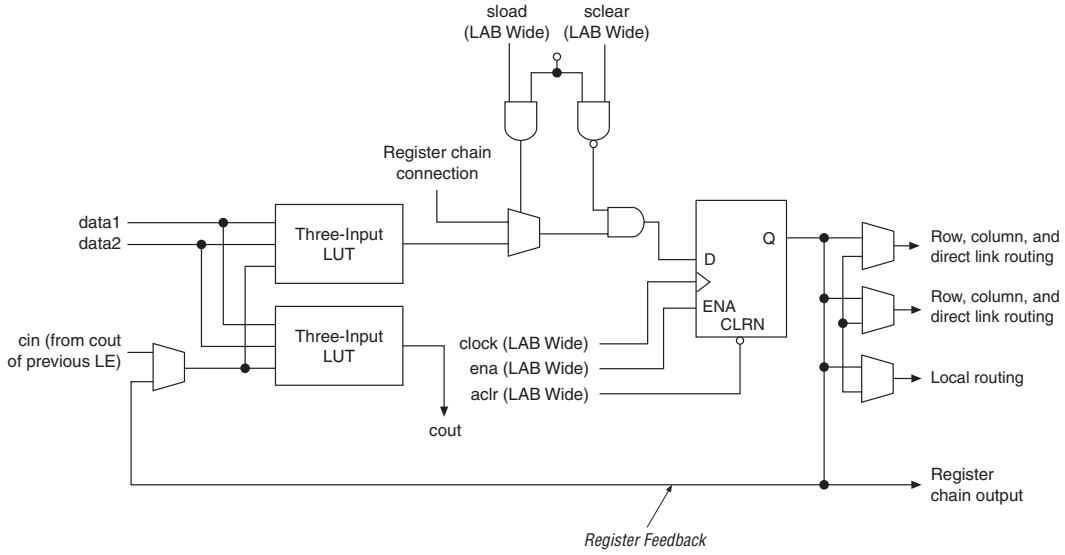
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	85
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8t144c6n

Contents

Figure 2–4. LE in Arithmetic Mode



The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 LEs by automatically linking LABs in the same column. For enhanced fitting, a long carry chain runs vertically, which allows fast horizontal connections to M4K memory blocks or embedded multipliers through direct link interconnects. For example, if a design has a long carry chain in a LAB column next to a column of M4K memory blocks, any LE output can feed an adjacent M4K memory block through the direct link interconnect. Whereas if the carry chains ran horizontally, any LAB not next to the column of M4K memory blocks would use other row or column interconnects to drive a M4K memory block. A carry chain continues as far as a full column.

Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Table 5–15. Cyclone II Performance (Part 4 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	8053	60	36	200.0	195.0	149.23	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	7453	60	48	200.0	195.0	151.28	163.02

Notes to Table 5–15 :

(1) This application uses registered inputs and outputs.
(2) This application uses registered multiplier input and output stages within the DSP block.
(3) This application uses the same clock source for both A and B ports.
(4) This application uses independent clock sources for A and B ports.
(5) This application uses PLL clock outputs that are globally routed to connect and drive M4K clock ports. Use of non-PLL clock sources or local routing to drive M4K clock ports may result in lower performance numbers than shown here. Refer to the Quartus II timing report for actual performance numbers.
(6) These numbers are for commercial devices.
(7) These numbers are for automotive devices.

Internal Timing

Refer to Tables 5–16 through 5–19 for the internal timing parameters.

Table 5–16. LE_FF Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TSU	–36	—	–40	—	–40	—	ps
	—	—	–38	—	–40	—	ps
TH	266	—	306	—	306	—	ps
	—	—	286	—	306	—	ps
TCO	141	250	135	277	135	304	ps
	—	—	141	—	141	—	ps
TCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
LVDS	—	11	13	16	11	13	15	11	13	15
RSDS	—	11	13	16	11	13	15	11	13	15
MINI_LVDS	—	11	13	16	11	13	15	11	13	15
SIMPLE_RSDS	—	15	19	23	15	19	23	15	19	23
1.2V_HSTL	—	130	132	133	—	—	—	—	—	—
1.2V_DIFFERENTIAL_HSTL	—	130	132	133	—	—	—	—	—	—
PCI	—	—	—	—	99	120	142	99	120	142
PCI-X	—	—	—	—	99	121	143	99	121	143
LVTTL	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
LVCMOS	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
2.5V	OCT_50_OHMS	346	369	392	324	326	327	324	326	327
1.8V	OCT_50_OHMS	198	203	209	202	203	204	202	203	204

Table 7–5. PLL Output signals

Port	Description	Source	Destination
c[2..0]	PLL clock outputs driving the internal global clock network or external clock output pin (PLL<#>_OUT)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
LVTTL (3.3, 2.5, and 1.8 V)	✓	✓	✓
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X *(1)*	✓	✓	✓
LVPECL	✓		
LVDS	✓	✓	✓
1.5 and 1.8 V differential HSTL class I and class II	✓		✓ *(2)*
1.8 and 2.5 V differential SSTL class I and class II	✓		✓ *(2)*
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II *(3)*	✓	✓	✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II *(3)*	✓	✓	✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II *(3)*	✓	✓	✓
SSTL-25 class I	✓	✓	✓

Each output port has a unique post-scale counter to divide down the high-frequency VCO. There are three post-scale counters (c0, c1, and c2), which range from 1 to 32. The following equations show the frequencies for the three post-scale counters:

$$f_{C0} = \frac{f_{VCO}}{C0} = f_{IN} \frac{m}{n \times C0}$$

$$f_{C1} = \frac{f_{VCO}}{C1} = f_{IN} \frac{m}{n \times C1}$$

$$f_{C2} = \frac{f_{VCO}}{C2} = f_{IN} \frac{m}{n \times C2}$$

All three output counters can drive the global clock network. The c2 output counter can also drive a dedicated external I/O pin (single ended or differential). This counter output can drive a dedicated external clock output pin (`PLL<#>_OUT`) and the global clock network at the same time.

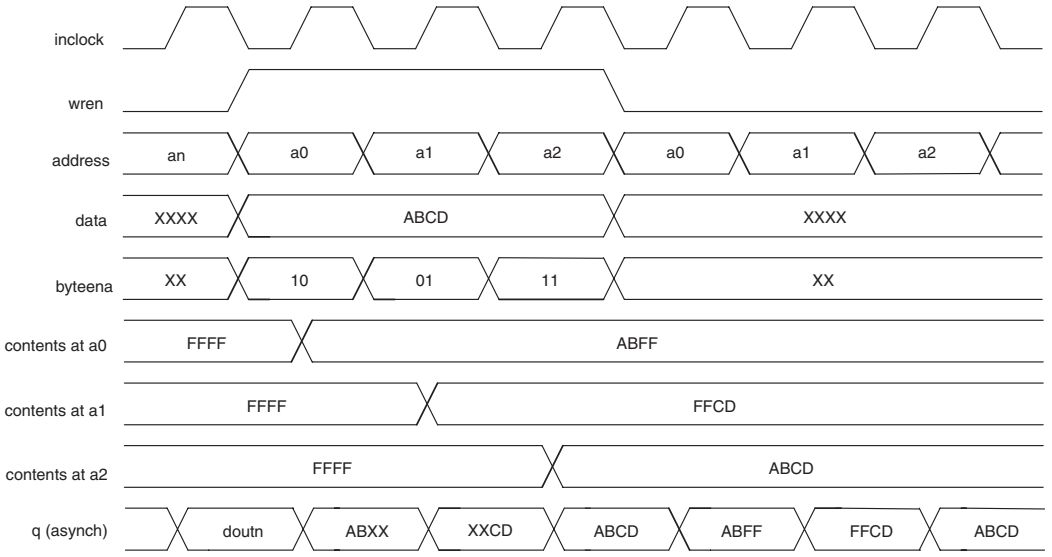
For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets the VCO frequency specifications. Then, the post-scale counters scale down the VCO frequency for each PLL clock output port. For example, if clock output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least common multiple in the VCO's range).

Programmable Duty Cycle

The programmable duty cycle feature allows you to set the PLL clock output duty cycles. The duty cycle is the ratio of the clock output high and low time to the total clock cycle time, expressed as a percentage of high time. This feature is supported on all three PLL post-scale counters, c0, c1, and c2, and when using all clock feedback modes.

The duty cycle is set by using a low- and high-time count setting for the post-scale counters. The Quartus II software uses the input frequency and target multiply/divide ratio to select the post-scale counter. The granularity of the duty cycle is determined by the post-scale counter value chosen on a PLL clock output and is defined as 50% ÷ post-scale counter value. For example, if the post-scale counter value is 3, then the allowable duty cycle precision would be 50% ÷ 3 = 16.67%. Because the `altpll` megafunction does not accept non-integer values for the duty cycle values, the allowable duty cycles are 17% 33% 50% and 67%. For example, if the c0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

Figure 8–2. Cyclone II Byte Enable Functional Waveform



Packed Mode Support

Cyclone II M4K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

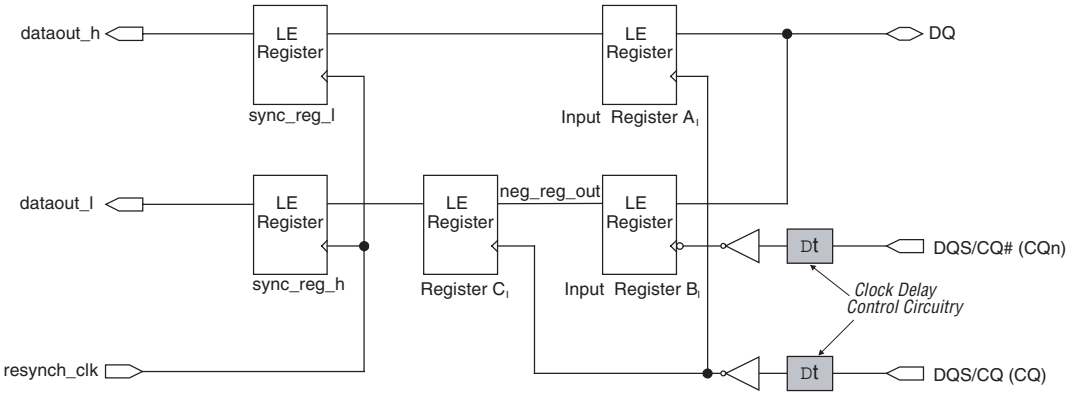
- Each of the two independent block sizes is less than or equal to half of the M4K block size. The maximum data width for each independent block is 18 bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

See "Single-Port Mode" on page 8–9 and "Single-Clock Mode" on page 8–24 for more information.

Address Clock Enable

Cyclone II M4K memory blocks support address clock enables, which holds the previous address value until needed. When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable.

Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Cyclone II DDR Memory Support Overview

Table 9–1 shows the external memory interfaces supported in Cyclone II devices.

Table 9–1. External Memory Support in Cyclone II Devices *Note (1)*

Memory Standard	I/O Standard	Maximum Bus Width	Maximum Clock Rate Supported (MHz)	Maximum Data Rate Supported (Mbps)
DDR SDRAM	SSTL-2 class I *(2)*	72	167	333 *(1)*
	SSTL-2 class II *(2)*	72	133	267 *(1)*
DDR2 SDRAM	SSTL-18 class I *(2)*	72	167	333 *(1)*
	SSTL-18 class II *(3)*	72	125	250 *(1)*
QDRII SRAM *(4)*	1.8-V HSTL class I *(2)*	36	167	667 *(1)*
	1.8-V HSTL class II *(3)*	36	100	400 *(1)*

Notes to Table 9–1:

(1) The data rate is for designs using the clock delay control circuitry.
(2) These I/O standards are supported on all the I/O banks of the Cyclone II device.
(3) These I/O standards are supported only on the I/O banks on the top and bottom of the Cyclone II device.
(4) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard because of higher I/O drive strength. QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR SDRAM with the clock delay control circuitry that can shift the incoming DQS signals to center them within the data window. To achieve DDR operation, the DDR input and output registers are implemented using the internal logic element (LE) registers. You should use the `altdqs` and `altdq` megafunctions in the Quartus II software to implement the DDR registers used for DQS and DQ signals, respectively.

In ×8 and ×16 modes, one DQS pin drives up to 8 or 16 DQ pins, respectively, within the group. In the ×9 and ×18 modes, a pair of DQS pins (CQ and CQ#) drives up to 9 or 18 DQ pins within the group to support one or two parity bits and the corresponding data bits. If the parity bits or any data bits are not used, the extra DQ pins can be used as regular user I/O pins. The ×9 and ×18 modes are used to support the QDRII memory interface. Table 9–2 shows the number of DQS/DQ groups supported in each Cyclone II density/package combination.

Table 9–2. Cyclone II DQS & DQ Bus Mode Support *Note (1)*

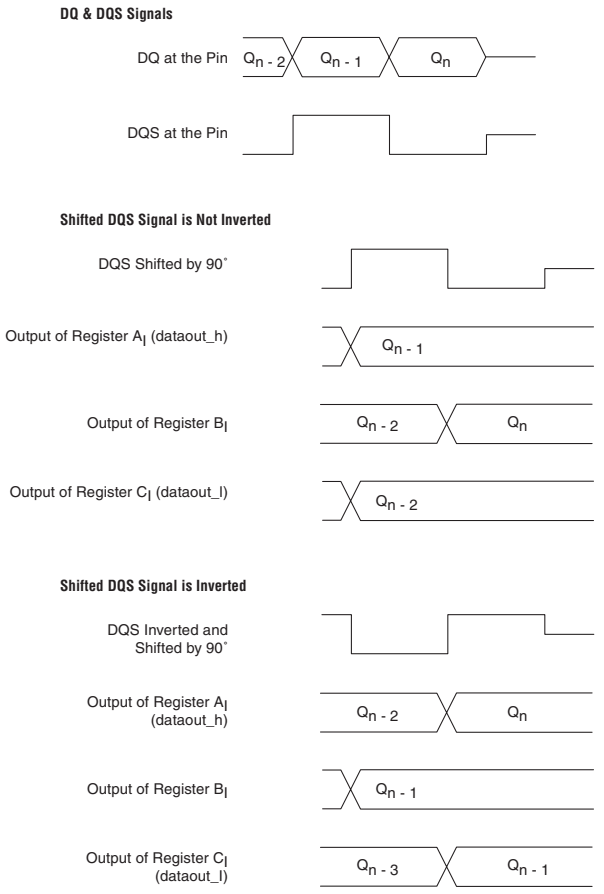
Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C5	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4	3	3
	256-pin FineLine BGA	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C8	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4 *(7)*	3	3
	256-pin FineLine BGA®	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C20	240-pin PQFP	8	4	4	4
	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C50	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C70	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
	896-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*

Notes to Table 9–2:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRII implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 9–2.
(7) Because of available clock resources, only a total of 3 DQ/DQS groups can be implemented.
(8) Because of available clock resources, only a total of 7 DQ/DQS groups can be implemented.

Figure 9–13 shows waveforms of the circuit shown in Figure 9–11. The first set of waveforms in Figure 9–13 shows the edge-aligned relationship between the DQ and DQS signals at the Cyclone II device pins. The second set of waveforms in Figure 9–13 shows what happens if the shifted DQS signal is not inverted. In this case, the last data, Q_n, does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in Figure 9–13 shows a proper read operation with the DQS signal inverted after the 90° shift. The last data, Q_n, does get latched. In this case the outputs of register A_I and register C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_I, register B_I, and register C_I refer to the nomenclature in Figure 9–11.

Figure 9–13. DQ Captures With Noninverted & Inverted Shifted DQS



transistor-to-transistor logic (TTL), and positive (or pseudo) emitter coupled logic (PECL). This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage. However, it does require a termination resistor of 90 to 110 Ωbetween the two signals at the input buffer. Cyclone II devices support true differential LVDS inputs and outputs.

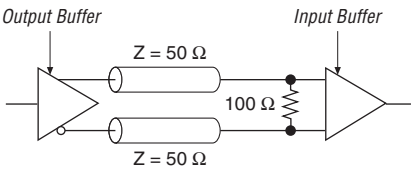
LVDS outputs on Cyclone II need external resistor network to work properly. Refer to the *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook* for more information.

For reduced swing differential signaling (RSDS), V_{OD} ranges from 100 to 600 mV. For mini-LVDS, V_{OD} ranges from 300 to 600 mV. The differential termination resistor value ranges from 95 to 105 Ωfor both RSDS and mini-LVDS. Cyclone II devices support RSDS/mini-LVDS outputs only.

Differential LVPECL

The low voltage positive (or pseudo) emitter coupled logic (LVPECL) standard is a differential interface standard recommending V_{CCIO} of 3.3 V. The LVPECL standard also supports V_{CCIO} of 2.5 V, 1.8 V and 1.5 V. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require an external 100-Ωtermination resistor between the two signals at the input buffer. Figures 10–17 and 10–18 show two alternate termination schemes for LVPECL. LVPECL input standard is supported at the clock input pins on Cyclone II devices. LVPECL output standard is not supported.

Figure 10–17. LVPECL DC Coupled Termination



After applying the equation above, apply one of the equations in Table 10–9, depending on the package type.

Table 10–9. Bidirectional Pad Limitation Formulas (Where V_{REF} Inputs Exist)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) ≤9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) ≤5 (per VCCIO and ground pair)

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 10–10.

Table 10–10. Bidirectional Pad Limitation Formulas (Where V_{REF} Outputs Exist)

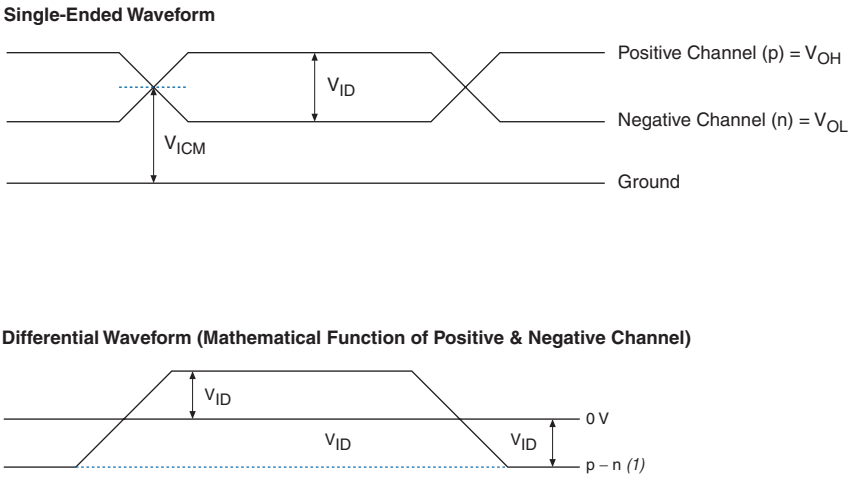
Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤5 (per VCCIO and ground pair)

When additional voltage referenced inputs and other outputs exist in the same V_{REF} bank, the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. As such, the following rules apply:

Total number of bidirectional pads + total number of input pads ≤30 (15 on each side of your V_{REF} pad) for Fineline BGA packages

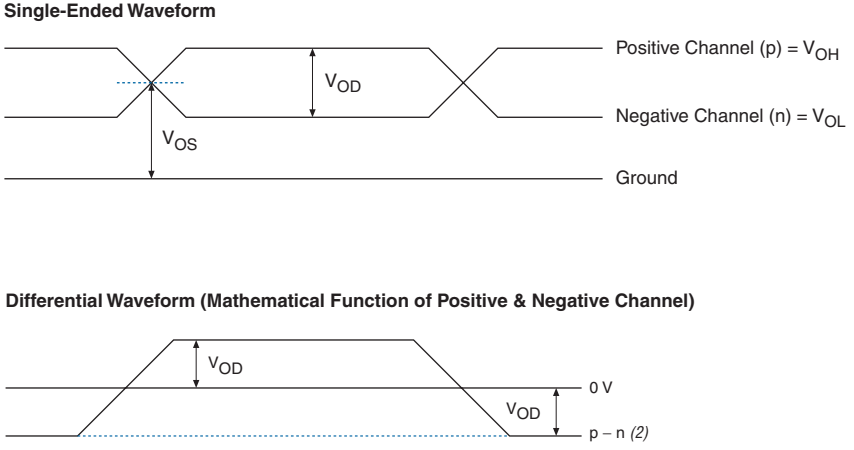
Total number of bidirectional pads + total number of input pads ≤20 (10 on each side of your V_{REF} pad) for QFP packages

Figure 11–4. Receiver Input Waveforms for the LVDS Differential I/O Standard



Note to Figure 11–4:
(1) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–5. Transmitter Output Waveform for the LVDS Differential I/O Standard *Note (2)*



Notes to Figure 11–5:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

When the `signa` and `signb` signals are unused, the Quartus® II software sets the multiplier to perform unsigned multiplication by default.

Output Registers

You can choose to register the embedded multiplier output using the output registers in 18- or 36-bit sections depending on the operational mode of the multiplier. The following control signals are available to each output register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, or asynchronous clear signal.

See the *Cyclone II Architecture* chapter in Volume 1 of the ***Cyclone II Device Handbook*** for more information on the embedded multiplier routing and interface.

Operational Modes

The embedded multiplier can be used in one of two operational modes, depending on the application needs:

- One 18-bit multiplier
- Up to two 9-bit independent multipliers

The Quartus II software includes megafunctions used to control the mode of operation of the multipliers. After you have made the appropriate parameter settings using the megafunction's MegaWizard® Plug-In Manager, the Quartus II software automatically configures the embedded multiplier.

The Cyclone II embedded multipliers can also be used to implement multiplier adder and multiplier accumulator functions where the multiplier portion of the function is implemented using embedded multipliers and the adder or accumulator function is implemented in logic elements (LEs).

For more information on megafunction and Quartus II support for Cyclone II embedded multipliers, see the "Software Support" section.

device also pulls nSTATUS and CONF_DONE low and tri-states all I/O pins. Once the nCONFIG pin returns to a logic high level and the Cyclone II device releases the nSTATUS pin, the MAX II device can begin reconfiguration.

Error During Configuration

If an error occurs during configuration, the Cyclone II device transitions its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin tells the MAX II device that there is an error. If you turn on the **Auto-restart configuration after error** option in the Quartus II software, the Cyclone II device releases nSTATUS after a reset time-out period (maximum of 40 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The MAX II device must monitor the Cyclone II device's CONF_DONE pin to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE do not transition high, the MAX II device must reconfigure the target device.

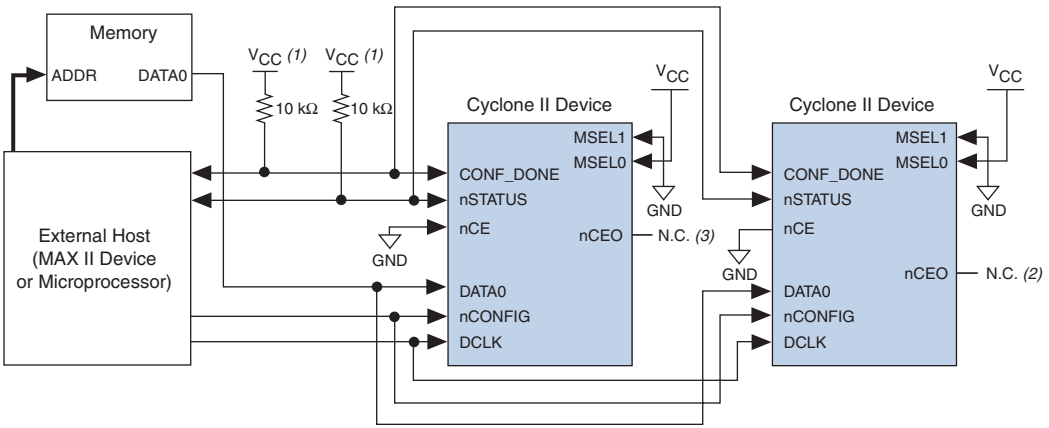
For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multiple Device PS Configuration Using a MAX II Device as an External Host

Figure 13–10 shows how to configure multiple devices using a MAX II device. This circuit is similar to the PS configuration circuit for a single device, except Cyclone II devices are cascaded for multiple device configuration.

If your system has multiple Cyclone II devices (in the same density and package) with the same configuration data, you can configure them in one configuration cycle by connecting all device's nCE pins to ground and connecting all the Cyclone II device's configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) together. You can also use the nCEO pin as a user I/O pin after configuration. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–11 shows multiple device PS configuration when both Cyclone II devices are receiving the same configuration data.

Figure 13–11. Multiple Device PS Configuration When Both FPGAs Receive the Same Data



Notes to Figure 13–11:

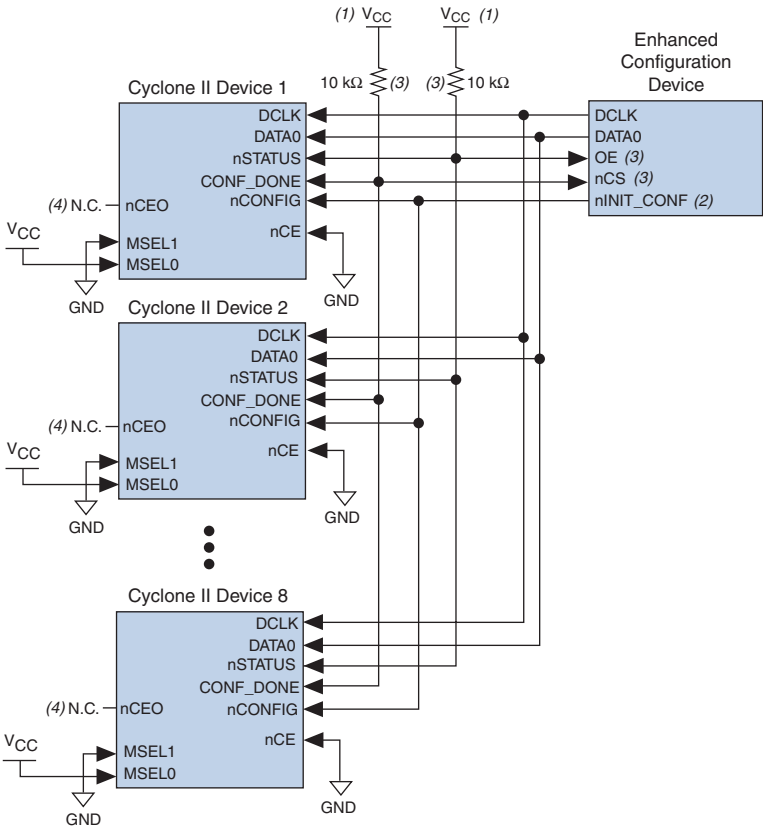
(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

You can use a single configuration chain to configure Cyclone II devices with other Altera devices. Connect all the Cyclone II device's and all other Altera device's CONF_DONE and nSTATUS pins together so all devices in the chain complete configuration at the same time or that an error reported by one device initiates reconfiguration in all devices.

For more information on configuring multiple Altera devices in the same configuration chain, see *Configuring Mixed Altera FPGA Chains* in the *Configuration Handbook*.

Figure 13–16. Multiple Device PS Configuration Using an Enhanced Configuration Device When FPGAs Receive the Same Data



Notes to Figure 13–16:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You can cascade several EPC2 or EPC1 devices to configure multiple Cyclone II devices. The first configuration device in the chain is the master configuration device, and the subsequent devices are the slave devices. The master configuration device sends DCLK to the Cyclone II