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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	85
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8t144c7

Section VII. PCB Layout Guidelines

Chapter 15. Package Information for Cyclone II Devices

Embedded multipliers can operate at up to 250 MHz (for the fastest speed grade) for 18 × 18 and 9 × 9 multiplications when using both input and output registers.

Each Cyclone II device has one to three columns of embedded multipliers that efficiently implement multiplication functions. An embedded multiplier spans the height of one LAB row. Table 2–10 shows the number of embedded multipliers in each Cyclone II device and the multipliers that can be implemented.

Table 2–10. Number of Embedded Multipliers in Cyclone II Devices *Note (1)*

Device	Embedded Multiplier Columns	Embedded Multipliers	9 × 9 Multipliers	18 × 18 Multipliers
EP2C5	1	13	26	13
EP2C8	1	18	36	18
EP2C15	1	26	52	26
EP2C20	1	26	52	26
EP2C35	1	35	70	35
EP2C50	2	86	172	86
EP2C70	3	150	300	150

Note to Table 2–10:

(1) Each device has either the number of 9 × 9-, or 18 × 18-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

The embedded multiplier consists of the following elements:

- Multiplier block
- Input and output registers
- Input and output interfaces

Figure 2–18 shows the multiplier block architecture.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{CONF} *(5) (6)*	Value of I/O pin pull-up resistor before and during configuration	V_{IN} = 0 V; V_{CCIO} = 3.3 V	10	25	50	kΩ
		V_{IN} = 0 V; V_{CCIO} = 2.5 V	15	35	70	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.8 V	30	50	100	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.5 V	40	75	150	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.2 V	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	*(7)*	—	1	2	kΩ

Notes to Table 5–3:

(1) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltages shown in Table 5–4, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(3) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(4) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (www.altera.com) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 5–13 for more information.

(5) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_{IN} value is not 0 V. Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

(6) Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

(7) These values apply to all V_{CCIO} settings.

Table 5–4 shows the maximum V_{IN} overshoot voltage and the dependency on the duty cycle of the input signal. Refer to Table 5–3 for more information.

Table 5–4. V_{IN} Overshoot Voltage for All Input Buffers

Maximum V_{IN} (V)	Input Signal Duty Cycle
4.0	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Table 5–15. Cyclone II Performance (Part 4 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	8053	60	36	200.0	195.0	149.23	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	7453	60	48	200.0	195.0	151.28	163.02

Notes to Table 5–15 :

(1) This application uses registered inputs and outputs.
(2) This application uses registered multiplier input and output stages within the DSP block.
(3) This application uses the same clock source for both A and B ports.
(4) This application uses independent clock sources for A and B ports.
(5) This application uses PLL clock outputs that are globally routed to connect and drive M4K clock ports. Use of non-PLL clock sources or local routing to drive M4K clock ports may result in lower performance numbers than shown here. Refer to the Quartus II timing report for actual performance numbers.
(6) These numbers are for commercial devices.
(7) These numbers are for automotive devices.

Internal Timing

Refer to Tables 5–16 through 5–19 for the internal timing parameters.

Table 5–16. LE_FF Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TSU	–36	—	–40	—	–40	—	ps
	—	—	–38	—	–40	—	ps
TH	266	—	306	—	306	—	ps
	—	—	286	—	306	—	ps
TCO	141	250	135	277	135	304	ps
	—	—	141	—	141	—	ps
TCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Table 5–51. LVDS Receiver Timing Specification

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×8	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×7	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×4	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×2	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(3)*	MHz
HSIODR	×10	100	—	805	100	—	640	100	—	640 *(2)*	Mbps
	×8	80	—	805	80	—	640	80	—	640 *(2)*	Mbps
	×7	70	—	805	70	—	640	70	—	640 *(2)*	Mbps
	×4	40	—	805	40	—	640	40	—	640 *(2)*	Mbps
	×2	20	—	805	20	—	640	20	—	640 *(2)*	Mbps
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(4)*	Mbps
SW	—	—	—	300	—	—	400	—	—	400	ps
Input jitter tolerance	—	—	—	500	—	—	500	—	—	550	ps
t_{LOCK}	—	—	—	100	—	—	100	—	—	100 *(5)*	ps

Notes to Table 5–51:
(1) For extended temperature devices, the maximum input clock frequency for x10 through x2 modes is 275 MHz.
(2) For extended temperature devices, the maximum data rate for x10 through x2 modes is 550 Mbps.
(3) For extended temperature devices, the maximum input clock frequency for x1 mode is 340 MHz.
(4) For extended temperature devices, the maximum data rate for x1 mode is 340 Mbps.
(5) For extended temperature devices, the maximum lock time is 500 us.

External Memory Interface Specifications

Table 5–52 shows the DQS bus clock skew adder specifications.

Table 5–52. DQS Bus Clock Skew Adder Specifications

Mode	DQS Clock Skew Adder	Unit
×9	155	ps
×18	190	ps

Note to Table 5–52:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×9 DQ group is 155 ps or ±77.5 ps.

Table 5–56. Maximum DCD for SDR Output on Column I/O Notes (1), (2) *(Part 2 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
2.5-V	140	140	155	ps
1.8-V	115	115	165	ps
1.5-V	745	745	770	ps
SSTL-2 Class I	60	60	75	ps
SSTL-2 Class II	60	60	80	ps
SSTL-18 Class I	60	130	130	ps
SSTL-18 Class II	60	135	135	ps
HSTL-18 Class I	60	115	115	ps
HSTL-18 Class II	75	75	100	ps
HSTL-15 Class I	150	150	150	ps
HSTL-15 Class II	135	135	155	ps
Differential SSTL-2 Class I	60	60	75	ps
Differential SSTL-2 Class II	60	60	80	ps
Differential SSTL-18 Class I	60	130	130	ps
Differential SSTL-18 Class II	60	135	135	ps
Differential HSTL-18 Class I	60	115	115	ps
Differential HSTL-18 Class II	75	75	100	ps
Differential HSTL-15 Class I	150	150	150	ps
Differential HSTL-15 Class II	135	135	155	ps
LVDS	60	60	60	ps
Simple RSDS	60	70	70	ps
Mini-LVDS	60	60	60	ps

Notes to Table 5–56:

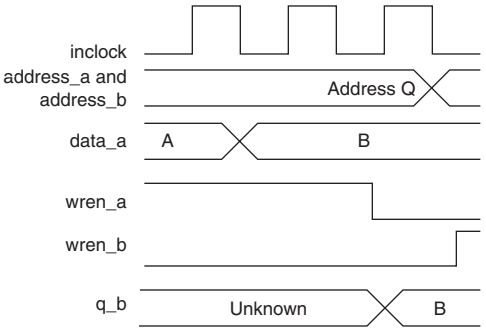
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) *(Part 1 of 2)*

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
LVCMOS	270	310	310	ps
LVTTL	285	305	335	ps
2.5-V	180	180	220	ps
1.8-V	165	175	205	ps

Figure 8–24. Cyclone II Mixed-Port Read-During-Write: Don't Care Mode *Note (1)*



Note to Figure 8–24:
(1) Outputs are not registered.

Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value is unknown during a mixed-port read-during-write operation.

Conclusion

The M4K memory structure of Cyclone II devices provides a flexible memory architecture with high memory bandwidth. It addresses the needs of different memory applications in FPGA designs with features such as different memory modes, byte enables, parity bit storage, address clock enables, mixed clock mode, shift register mode, mixed-port width support, and true dual-port mode.

Referenced Documents

This chapter references the following documents:

- *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*
- *Single- and Dual-Clock FIFO Megafunction User Guide*
- *Using Parity to Detect Errors White Paper*

Cyclone II DDR Memory Support Overview

Table 9–1 shows the external memory interfaces supported in Cyclone II devices.

Table 9–1. External Memory Support in Cyclone II Devices *Note (1)*

Memory Standard	I/O Standard	Maximum Bus Width	Maximum Clock Rate Supported (MHz)	Maximum Data Rate Supported (Mbps)
DDR SDRAM	SSTL-2 class I *(2)*	72	167	333 *(1)*
	SSTL-2 class II *(2)*	72	133	267 *(1)*
DDR2 SDRAM	SSTL-18 class I *(2)*	72	167	333 *(1)*
	SSTL-18 class II *(3)*	72	125	250 *(1)*
QDRII SRAM *(4)*	1.8-V HSTL class I *(2)*	36	167	667 *(1)*
	1.8-V HSTL class II *(3)*	36	100	400 *(1)*

Notes to Table 9–1:

(1) The data rate is for designs using the clock delay control circuitry.
(2) These I/O standards are supported on all the I/O banks of the Cyclone II device.
(3) These I/O standards are supported only on the I/O banks on the top and bottom of the Cyclone II device.
(4) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard because of higher I/O drive strength. QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR SDRAM with the clock delay control circuitry that can shift the incoming DQS signals to center them within the data window. To achieve DDR operation, the DDR input and output registers are implemented using the internal logic element (LE) registers. You should use the `altdqs` and `altdq` megafunctions in the Quartus II software to implement the DDR registers used for DQS and DQ signals, respectively.

DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

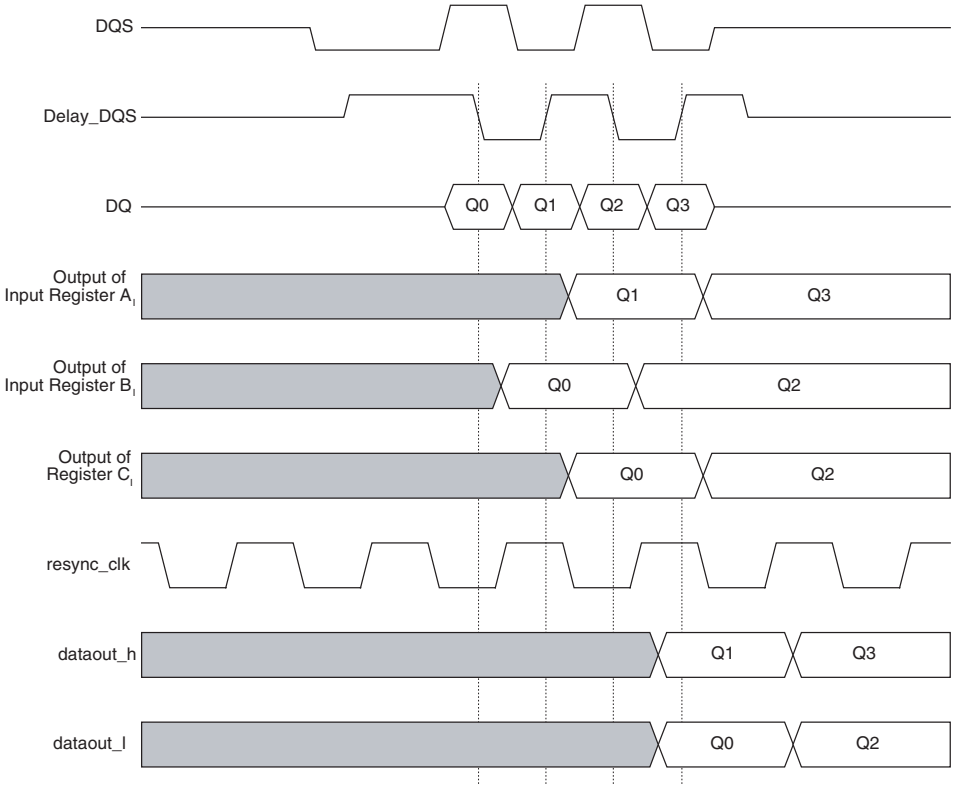
DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see Figure 9–1). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see Figure 9–9). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

Section IV. I/O Standards

This section provides information on Cyclone® II single-ended, voltage referenced, and differential I/O standards.

This section includes the following chapters:

- Chapter 10, Selectable I/O Standards in Cyclone II Devices
- Chapter 11, High-Speed Differential Interfaces in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(3)*	*(4)*	1.5 V	—	—	—	✓ *(6)*	—
		1.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential HSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—	—	✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(7)*	Differential	*(4)*	2.5 V	—	✓	—	✓	✓
LVPECL *(8)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(4)*	✓	—	✓	—	—

Notes to Table 10–1:

(1) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(2) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(3) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(4) This I/O standard is not supported on these I/O pins.
(5) This I/O standard is only supported on the dedicated clock pins.
(6) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(7) mini-LVDS and RSDS are only supported on output pins.
(8) LVPECL is only supported on clock inputs, not DQS and dual-purpose clock pins.

3.3-V LVTTL (EIA/JEDEC Standard JESD8-B)

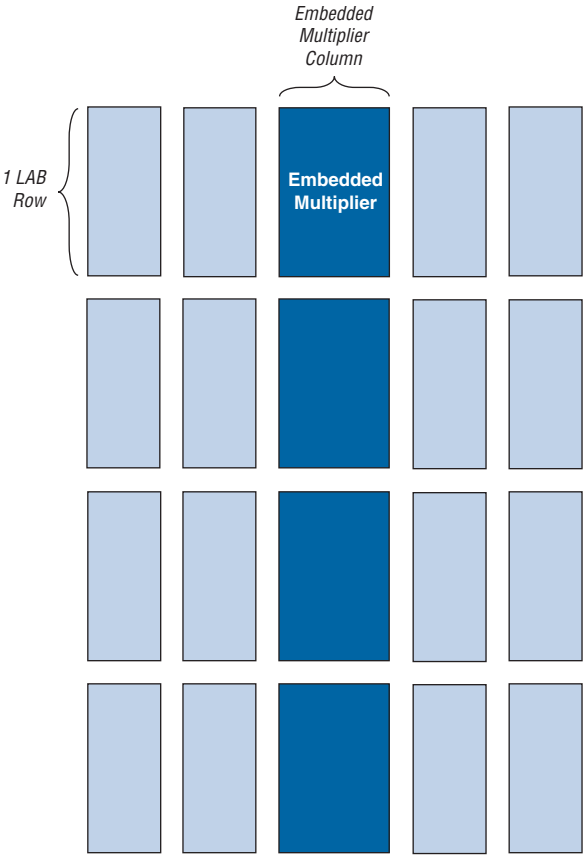
The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-/3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.3\ V \leq V_I \leq 3.9\ V$. Altera recommends an input voltage range of $-0.5\ V \leq V_I \leq 4.1\ V$.

Embedded Multiplier Block Overview

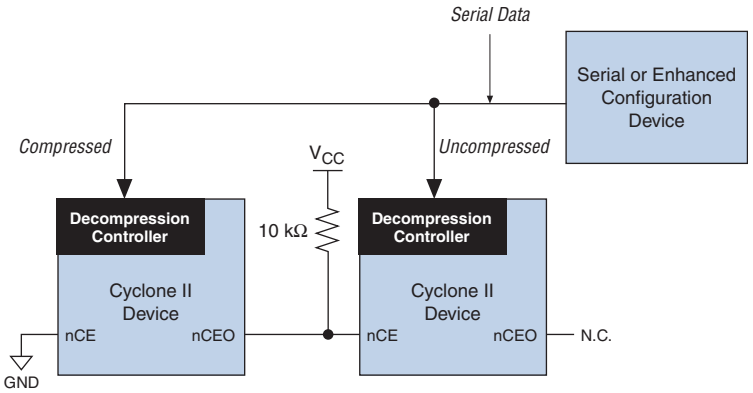
Each Cyclone II device has one to three columns of embedded multipliers that implement multiplication functions. Figure 12–1 shows one of the embedded multiplier columns with the surrounding LABs. Each embedded multiplier can be configured to support one 18 × 18 multiplier or two 9 × 9 multipliers.

Figure 12–1. Embedded Multipliers Arranged in Columns with Adjacent LABs



When multiple Cyclone II devices are cascaded, the compression feature can be selectively enabled for each device in the chain. Figure 13–2 depicts a chain of two Cyclone II devices. The first Cyclone II device has compression enabled and therefore receives a compressed bitstream from the configuration device. The second Cyclone II device has the compression feature disabled and receives uncompressed data.

Figure 13–2. Compressed & Uncompressed Configuration Data in a Programming File



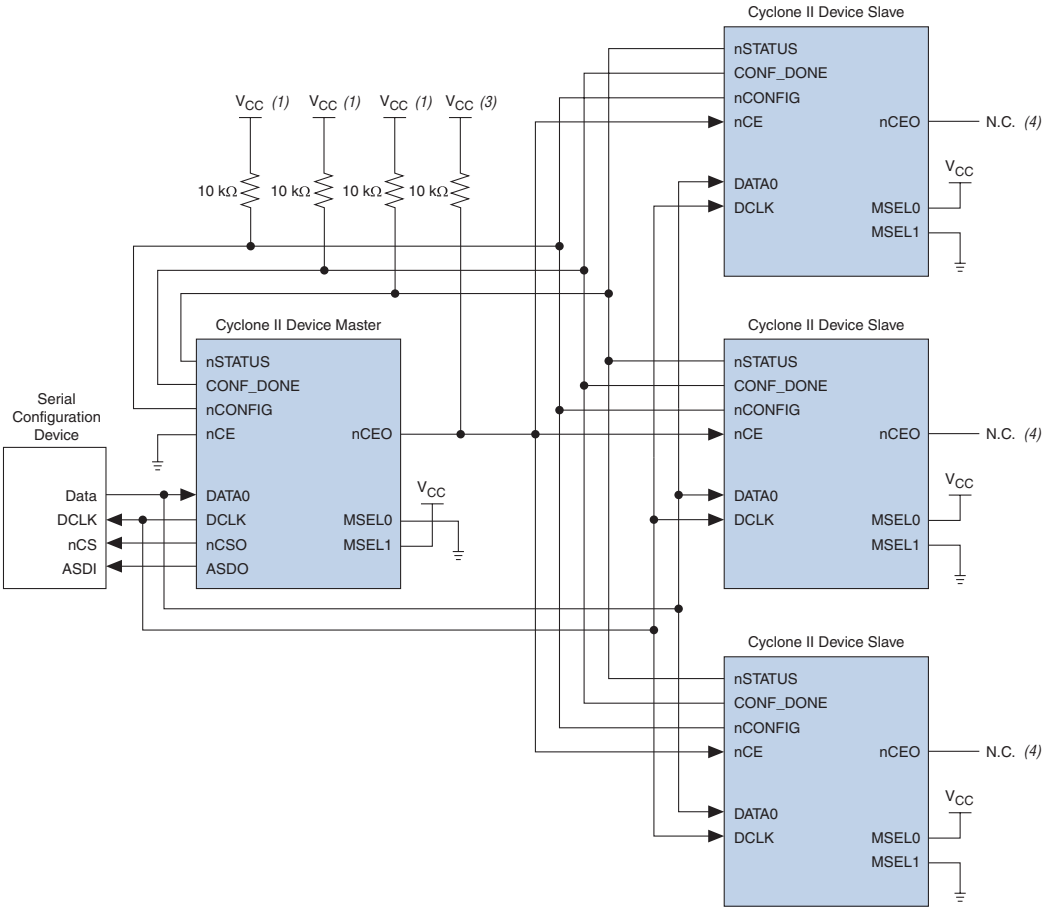
You can generate programming files (for example, POF files) for this setup in the Quartus II software.

Active Serial Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone II devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memory that feature a simple, four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

For more information on serial configuration devices, see the *Serial Configuration Devices Data Sheet* in the Configuration Handbook.

Figure 13–5. Multiple Device AS Configuration When FPGAs Receive the Same Data with Multiple SOFs



Notes to Figure 13–5:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

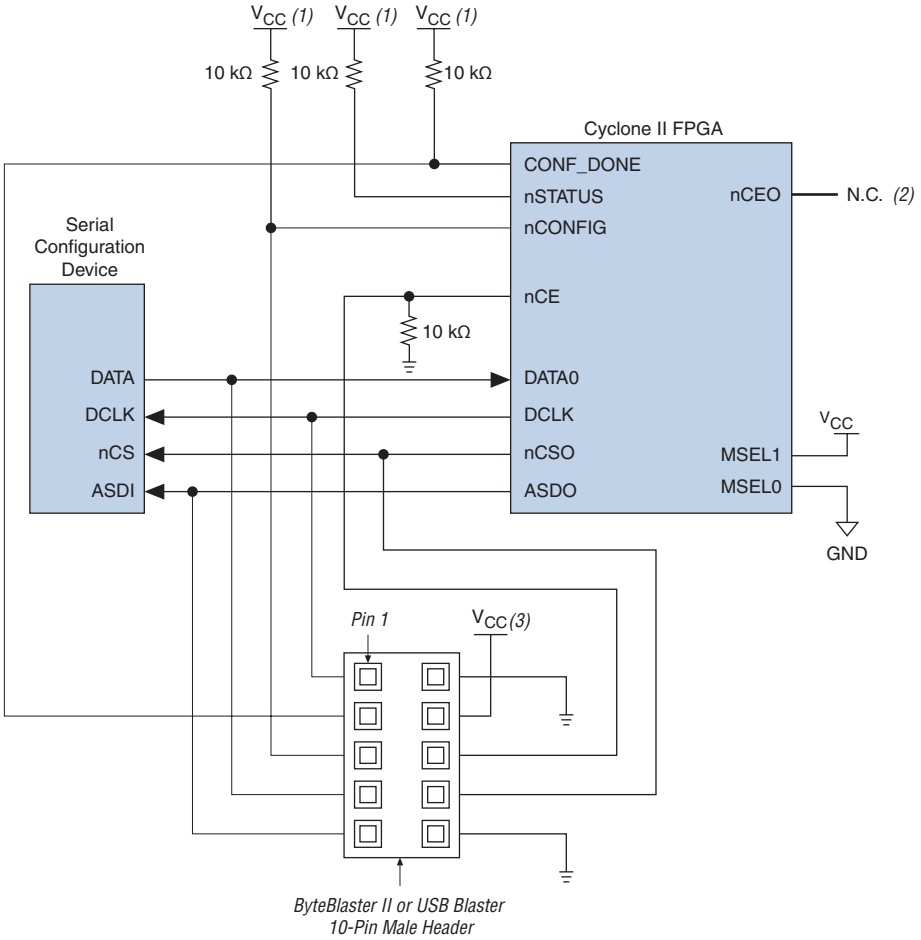
Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™ or ByteBlaster™ II download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can use the AS programming interface to program serial configuration devices in-system. During in-system programming, the download cable disables FPGA access to the AS interface by driving the `nCE` pin high. Cyclone II devices are also held in reset by pulling the `nCONFIG` signal low. After programming is complete, the download cable releases the `nCE` and `nCONFIG` signals, allowing the pull-down and pull-up resistor to drive GND and V_{CC}, respectively. Figure 13–7 shows the download cable connections to the serial configuration device.

For more information on the USB-Blaster download cable, see the *USB-Blaster USB Port Download Cable Data Sheet*. For more information on the ByteBlaster II cable, see the *ByteBlaster II Download Cable Data Sheet*.

Figure 13–7. In-System Programming of Serial Configuration Devices



Notes to Figure 13–7:

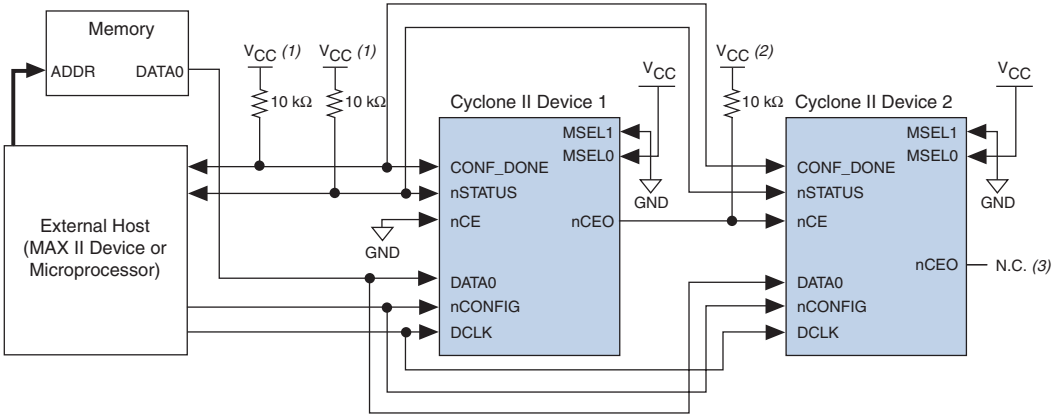
(1) Connect these pull-up resistors to 3.3-V supply.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(3) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with a 3.3-V supply.

You can use the Quartus II software with the APU and the appropriate configuration device programming adapter to program serial configuration devices. All serial configuration devices are offered in an 8-pin or 16-pin small outline integrated circuit (SOIC) package and can be programmed using the PLMSEPC-8 adapter.

Figure 13–10. Multiple Device PS Configuration Using an External Host



Notes to Figure 13–10:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In multiple device PS configuration, connect the first Cyclone II device's nCE pin to GND and connect the nCEO pin to the nCE pin of the next Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin high to its V_{CCIO} level to help the internal weak pull-up resistor when the nCEO pin feeds next Cyclone II device's nCE pin. The input to the nCE pin of the last Cyclone II device in the chain comes from the previous Cyclone II device. After the first device completes configuration in a multiple device configuration chain, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the MAX II device begins to transfer data to the next Cyclone II device without interruption. The nCEO pin is a dual-purpose pin in Cyclone II devices. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

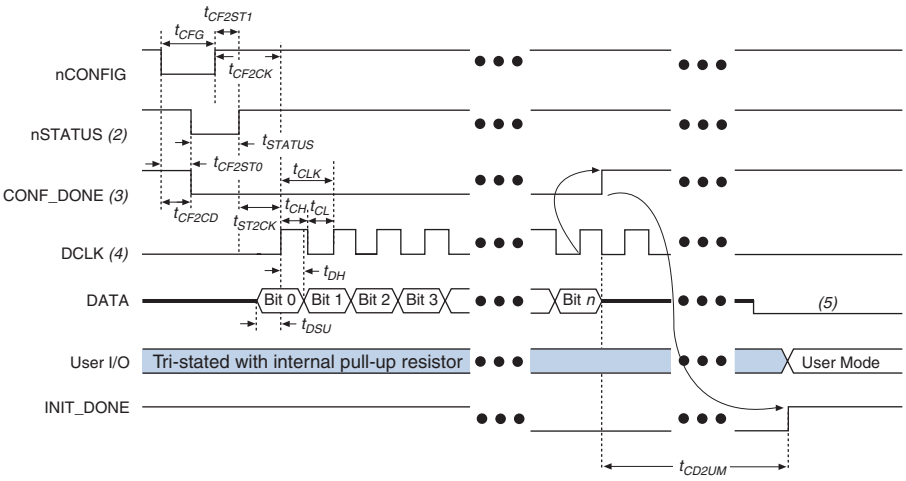
The Quartus II software sets the Cyclone II device nCEO pin as a dedicated output by default. If the nCEO pin feeds the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

PS Configuration Timing

A PS configuration must meet the setup and hold timing parameters and the maximum clock frequency. When using a microprocessor or another intelligent host to control the PS interface, ensure that you meet these timing requirements.

Figure 13–12 shows the timing waveform for PS configuration for Cyclone II devices.

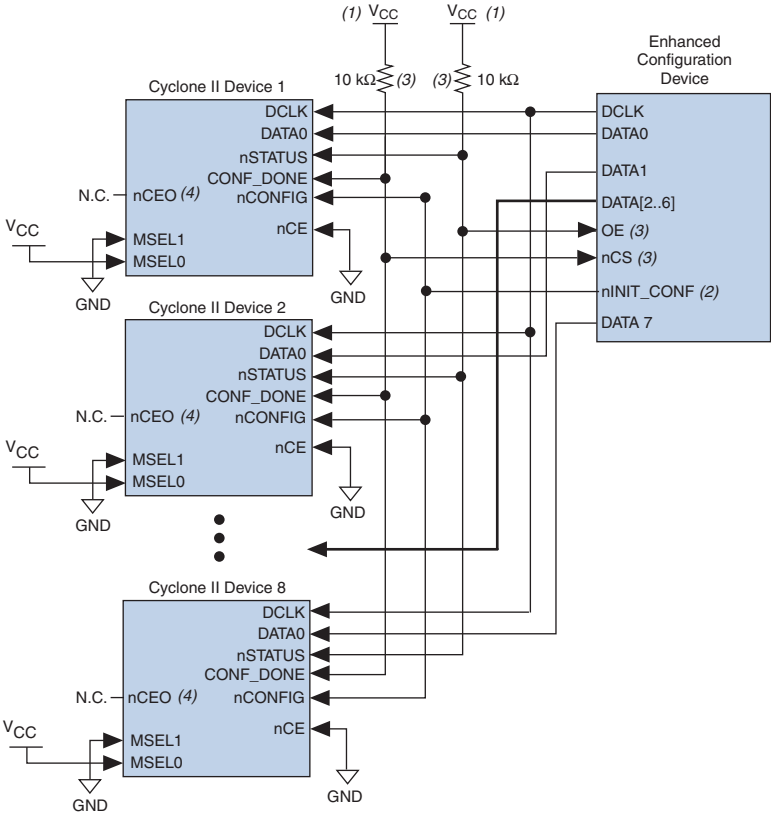
Figure 13–12. PS Configuration Timing Waveform *Note (1)*



Notes to Figure 13–12:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
(2) Upon power-up, the Cyclone II device holds nSTATUS low for the time of the POR delay.
(3) Upon power-up, before and during configuration, CONF_DONE is low.
(4) In user mode, drive DCLK either high or low when using the PS configuration scheme, whichever is more convenient. When using the AS configuration scheme, DCLK is a Cyclone II output pin and should not be driven externally.
(5) Do not leave the DATA pin floating after configuration. Drive it high or low, whichever is more convenient.

Figure 13–15. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device



Notes to Table 13–15:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

The Quartus II software only allows you to set *n* to 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. For example, if you configure three FPGAs, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding SOF data is transmitted from the configuration device to the FPGA. For