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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	516
Number of Logic Elements/Cells	8256
Total RAM Bits	165888
Number of I/O	85
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c8t144i8

A LAB-wide asynchronous load signal to control the logic for the register's preset signal is not available. The register preset is achieved by using a NOT gate push-back technique. Cyclone II devices can only support either a preset or asynchronous clear signal.

In addition to the clear port, Cyclone II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Cyclone II architecture, connections between LEs, M4K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row (direct link, R4, and R24) and column (register chain, C4, and C16) interconnects that span fixed distances. A routing structure with fixed-length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

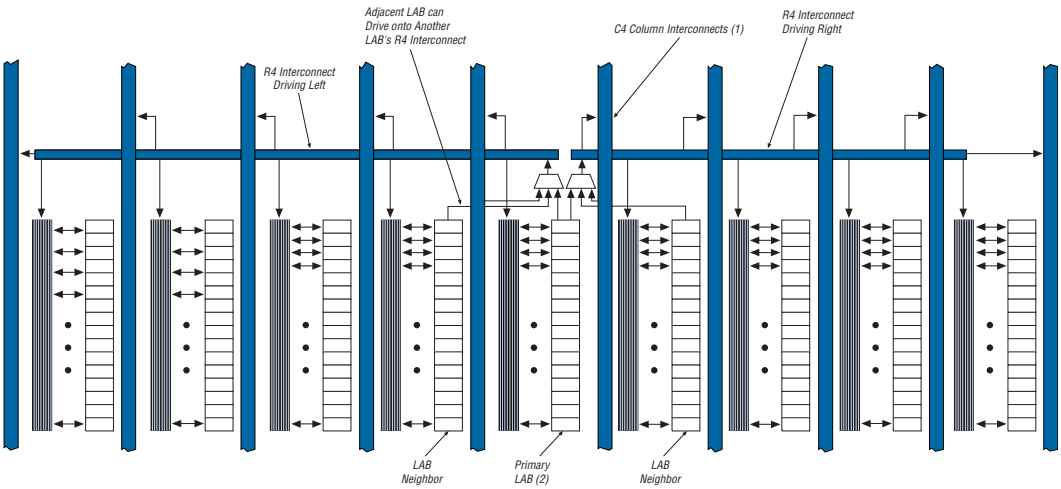
Dedicated row interconnects route signals to and from LABs, PLLs, M4K memory blocks, and embedded multipliers within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 interconnects for high-speed access across the length of the device

The direct link interconnect allows an LAB, M4K memory block, or embedded multiplier block to drive into the local interconnect of its left and right neighbors. Only one side of a PLL block interfaces with direct link and row interconnects. The direct link interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M4K memory block, or three LABs and one embedded multiplier to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–8 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by LABs, M4K memory blocks, embedded multipliers, PLLs, and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor (see Figure 2–8) can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. Additionally, R4 interconnects can drive R24 interconnects, C4, and C16 interconnects for connections from one row to another.

Figure 2–8. R4 Interconnect Connections



Notes to Figure 2–8:

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

Cyclone II devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 Ω When used with the output drivers, on-chip termination sets the output driver impedance to 25 or 50 Ω Cyclone II devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18. Table 2–19 lists the I/O standards that support impedance matching and series termination.

Table 2–19. I/O Standards Supporting Series Termination *Note (1)*

I/O Standards	Target R_S (Ω)	V_{CCIO} (V)
3.3-V LVTTL and LVCMOS	25 *(2)*	3.3
2.5-V LVTTL and LVCMOS	50 *(2)*	2.5
1.8-V LVTTL and LVCMOS	50 *(2)*	1.8
SSTL-2 class I	50 *(2)*	2.5
SSTL-18 class I	50 *(2)*	1.8

Notes to Table 2–19:

(1) Supported conditions are $V_{CCIO} = V_{CCIO} \pm 50$ mV.

(2) These R_S values are nominal values. Actual impedance varies across process, voltage, and temperature conditions.

The recommended frequency range of operation is pending silicon characterization.

On-chip series termination can be supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins in order to enable on-chip series termination in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} are not conflicting.

When using on-chip series termination, programmable drive strength is not available.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage and temperature. The actual tolerance is pending silicon characterization.

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

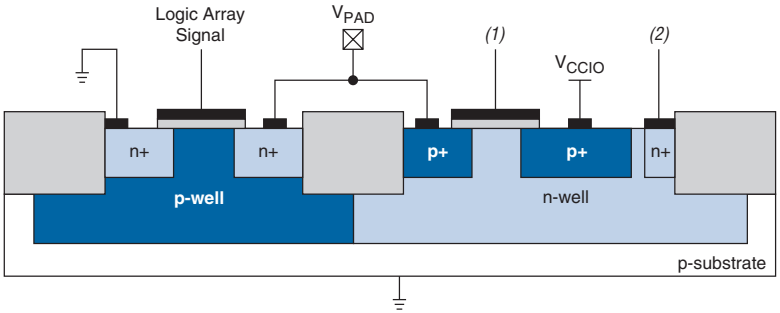
Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:
(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Cyclone II devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT} voltage levels and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels. In addition, the POR circuitry also monitors the V_{CCIO} level of the two I/O banks that contains configuration pins (I/O banks 1 and 3 for EP2C5 and EP2C8, I/O banks 2 and 6 for EP2C15A, EP2C20, EP2C35, EP2C50, and EP2C70) and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels.

After the Cyclone II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If the V_{CCINT} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

"Wake-up" Time for Cyclone II Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone II device family offers the Fast-On feature to support fast wake-up time applications. Devices that support the Fast-On feature are designated with an "A" in the ordering code and have stricter power up requirements compared to non-A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–25:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–26. EP2C15A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–26:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C20/A Clock Timing Parameters

Tables 5–27 and 5–28 show the clock timing parameters for EP2C20/A devices.

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 1 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
LVTTL	4 mA	t_{OP}	1343	1408	2539	2694	2885	2891	ps
		t_{DIP}	1467	1540	2747	2931	3158	3158	ps
	8 mA	t_{OP}	1198	1256	2411	2587	2756	2762	ps
		t_{DIP}	1322	1388	2619	2824	3029	3029	ps
	12 mA	t_{OP}	1156	1212	2282	2452	2614	2620	ps
		t_{DIP}	1280	1344	2490	2689	2887	2887	ps
	16 mA	t_{OP}	1124	1178	2286	2455	2618	2624	ps
		t_{DIP}	1248	1310	2494	2692	2891	2891	ps
	20 mA	t_{OP}	1112	1165	2245	2413	2574	2580	ps
		t_{DIP}	1236	1297	2453	2650	2847	2847	ps
	24 mA (1)	t_{OP}	1105	1158	2253	2422	2583	2589	ps
		t_{DIP}	1229	1290	2461	2659	2856	2856	ps
LVCMOS	4 mA	t_{OP}	1200	1258	2231	2396	2555	2561	ps
		t_{DIP}	1324	1390	2439	2633	2828	2828	ps
	8 mA	t_{OP}	1125	1179	2260	2429	2591	2597	ps
		t_{DIP}	1249	1311	2468	2666	2864	2864	ps
	12 mA (1)	t_{OP}	1106	1159	2217	2383	2543	2549	ps
		t_{DIP}	1230	1291	2425	2620	2816	2816	ps
2.5V	4 mA	t_{OP}	1126	1180	2350	2477	2598	2604	ps
		t_{DIP}	1250	1312	2558	2714	2871	2871	ps
	8 mA (1)	t_{OP}	1105	1158	2177	2296	2409	2415	ps
		t_{DIP}	1229	1290	2385	2533	2682	2682	ps

Figure 5–5. RSDS Transmitter Clock to Data Relationship

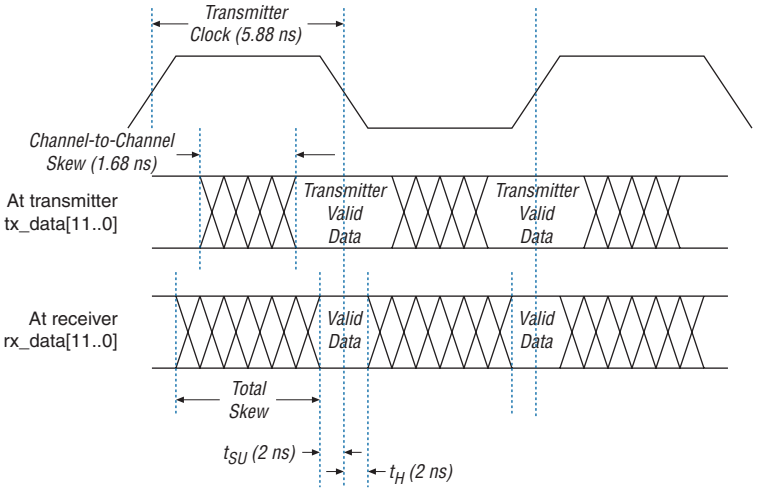
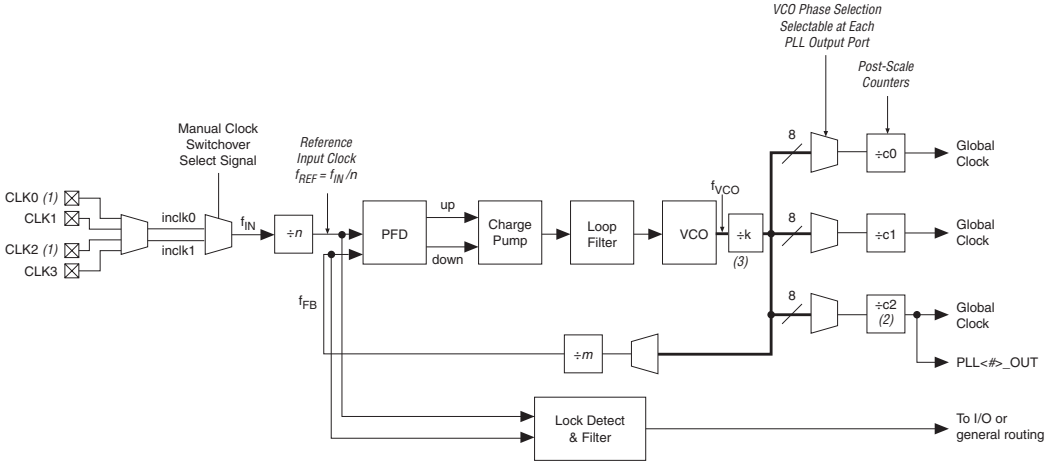


Table 5–49 shows the mini-LVDS transmitter timing budget for Cyclone II devices at 311 Mbps. Cyclone II devices cannot receive mini-LVDS data because the devices are intended for applications where they will be driving display drivers. A maximum mini-LVDS data rate of 311 Mbps is supported for Cyclone II devices using DDIO registers. Cyclone II devices support mini-LVDS only in the commercial temperature range.

Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz

Figure 7–2. Cyclone II PLL Block Diagram



Notes to Figure 7–2:

(1) This input can be single-ended or differential. If you are using a differential I/O standard, then the design uses two clock pins. LVDS input is supported via the secondary function of the dedicated clock pins. For example, the CLK0 pin's secondary function is LVDSCLK1p and the CLK1 pin's secondary function is LVDSCLK1n. Figure 7–2 shows the possible clock input connections to PLL 1.

(2) This counter output is shared between a dedicated external clock output (PLL<#>_OUT) and the global clock network.

(3) If the VCO post scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.

The Cyclone II PLL supports up to three global clock outputs and one dedicated external clock output. The output frequency to the global clock network or dedicated external clock output is determined by using the following equation:

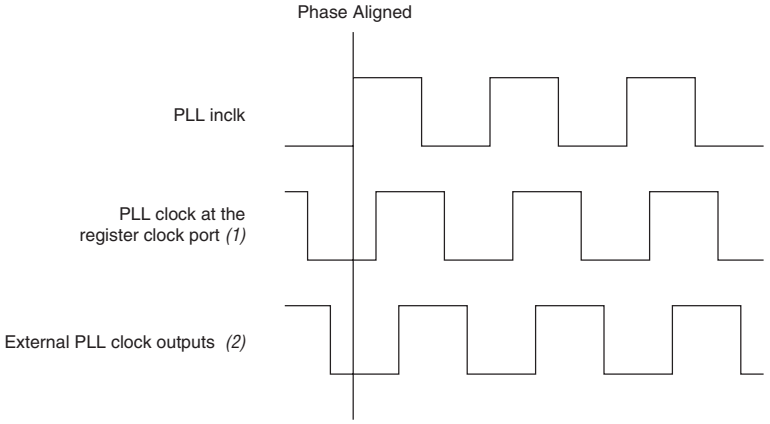
$$f_{global/external} = f_{IN} \frac{m}{n \times C}$$

f_{IN} is the clock input to the PLL and C is the setting on the c0, c1, or c2 counter.

The VCO frequency is determined in all cases by using the following equation:

$$f_{VCO} = f_{IN} \frac{m}{n}$$

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode

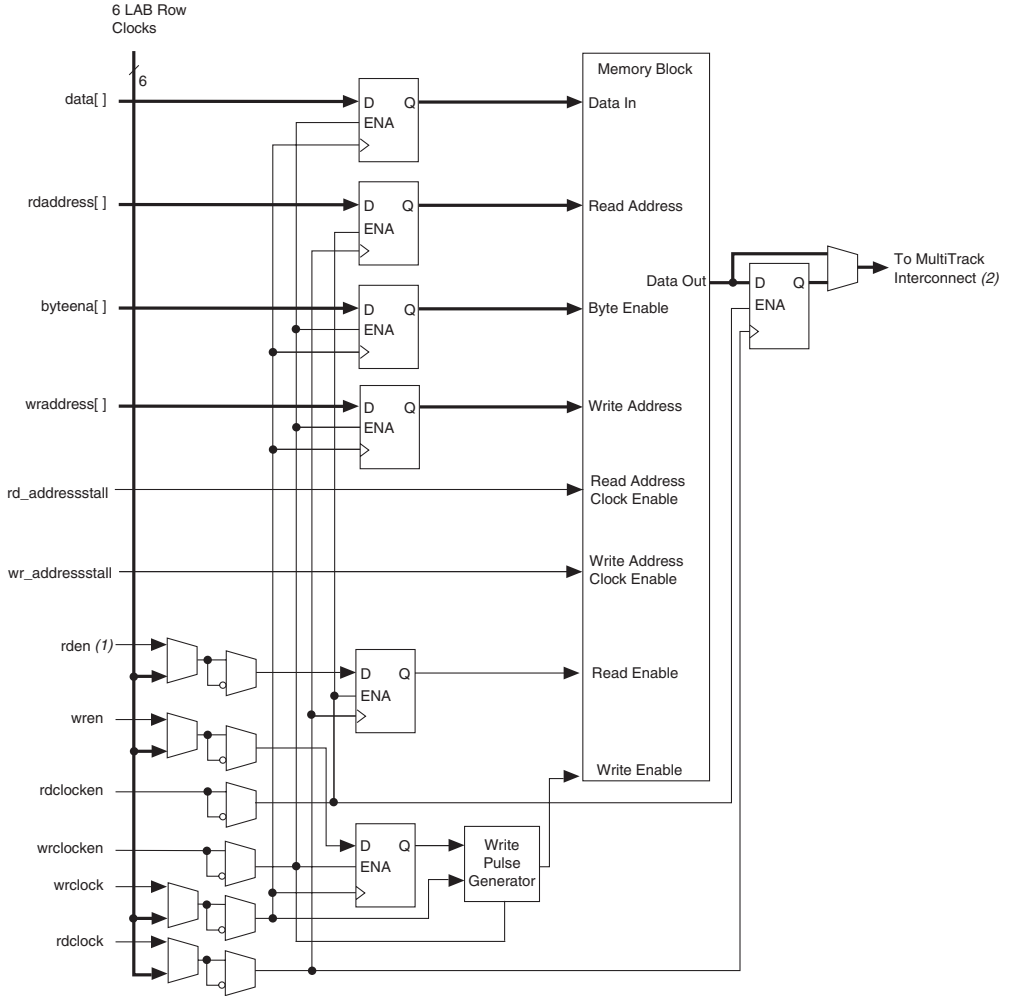


Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Figure 8–17. Cyclone II Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 8–17:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTract interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 9–13 shows waveforms of the circuit shown in Figure 9–11. The first set of waveforms in Figure 9–13 shows the edge-aligned relationship between the DQ and DQS signals at the Cyclone II device pins. The second set of waveforms in Figure 9–13 shows what happens if the shifted DQS signal is not inverted. In this case, the last data, Q_n, does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in Figure 9–13 shows a proper read operation with the DQS signal inverted after the 90° shift. The last data, Q_n, does get latched. In this case the outputs of register A_I and register C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_I, register B_I, and register C_I refer to the nomenclature in Figure 9–11.

Figure 9–13. DQ Captures With Noninverted & Inverted Shifted DQS

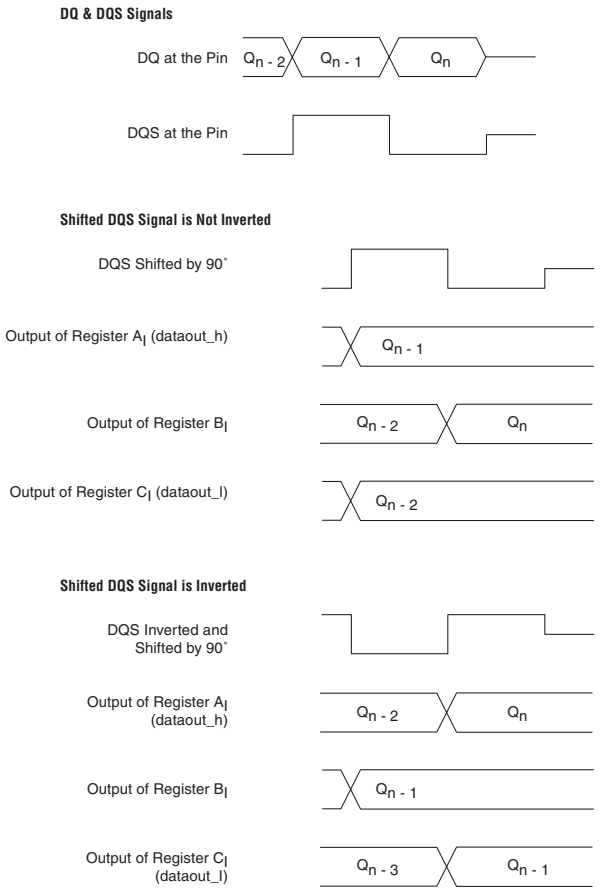


Table 10–6. Programmable Drive Strength (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	—
	24	—
SSTL-18 class I	6	6
	8	8
	10	10
	12	—
SSTL-18 class II	16	—
	18	—
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	N/A
	18	—
	20	—
HSTL-15 class I	8	8
	10	—
	12	—
HSTL-15 class II	16	N/A

These drive-strength settings are programmable on a per-pin basis using the Quartus II software.

After applying the equation above, apply one of the equations in Table 10–11, depending on the package type.

Table 10–11. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤9 (per VCCIO/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤5 (per VCCIO/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (refer to Table 10–4 for more details) and compatible V_{REF} voltage levels.

DDR and QDR Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads have to be on the same power bank as DQS pads. With the DDR and DDR2 memory interfaces, a VCCIO and ground pair can have a maximum of five DQ pads.

For a QDR interface, D is the QDR output and Q is the QDR input. D pads and Q pads have to be on the same power bank as CQ. With the QDR and QDRII memory interfaces, a VCCIO and ground pair can have a maximum of five D and Q pads.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone II QDR and QDRII performance is not guaranteed.

DC Guidelines

There is a current limit of 240 mA per eight consecutive output top and bottom pins per power pair, as shown by the following equation:

$$\sum_{pin}^{pin+7} I_{PIN} < 240mA \text{ per power pair}$$

There is a current limit of 240 mA per 12 consecutive output side (left and right) pins per power pair, as shown by the following equation:

Referenced Documents

This chapter references the following documents:

- *Altera Reliability Report*
- *AN 75: High-Speed Board Designs*
- *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Cyclone II Device Family Data Sheet*, *section 1* of the *Cyclone II Device Handbook*
- *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*
- *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*

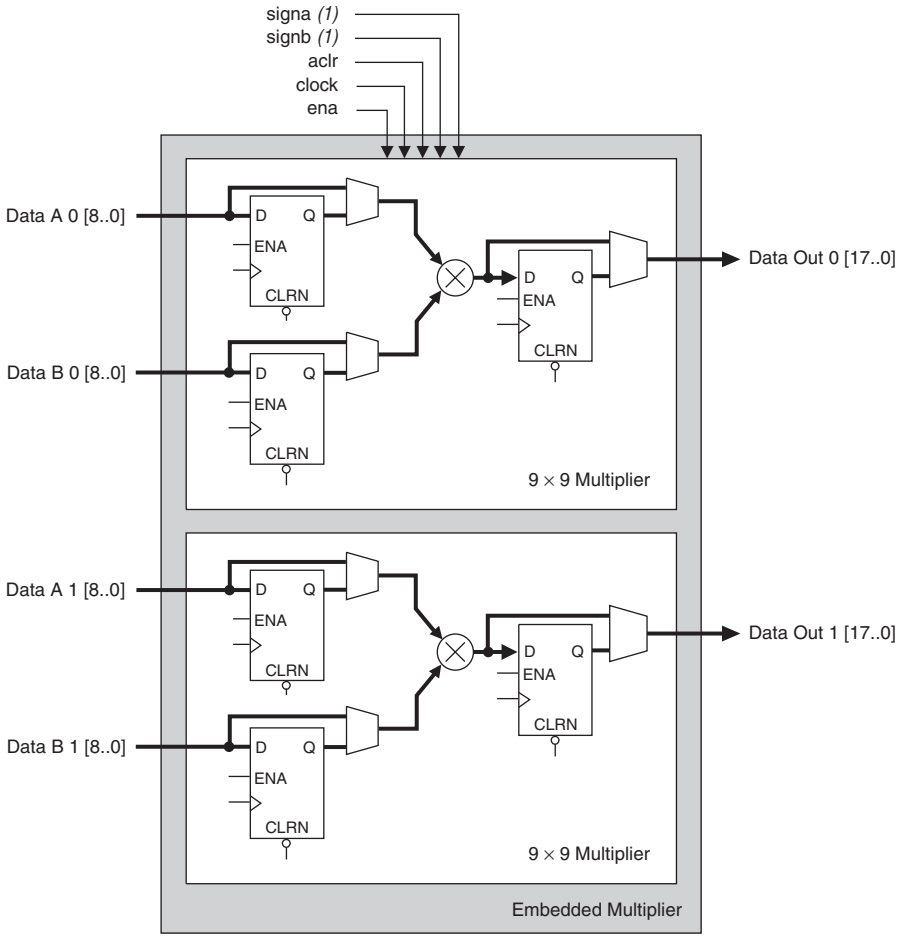
Document Revision History

Table 10–13 shows the revision history for this document.

Table 10–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v2.4	• Added "Referenced Documents" section. • Updated "Differential Pad Placement Guidelines" section.	—
February 2007 v2.3	• Added document revision history. • Updated "Introduction" and its feetpara note. • Updated *Note (2)* in Table 10–4. • Updated "Differential LVPECL" section. • Updated "Differential Pad Placement Guidelines" section. • Updated "Output Pads" section. • Added new section "5.0-V Device Compatibility" with two new figures.	• Added reference detail for ESD specifications. • Added information about differential placement restrictions applying only to pins in the same bank. • Added information that Cyclone II device supports LVDS on clock inputs at 3.3V V_{CCIO}. • Added more information on DC placement guidelines. • Added information stating SSTL and HSTL outputs can be closer than 2 pads from V_{REF}. • Added 5.0 Device tolerence solution.

Figure 12–4. 9-Bit Multiplier Mode



Note to Figure 12–4:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 9-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Each embedded multiplier only has one `signa` signal to control the sign representation of both data A inputs (one for each 9 × 9 multiplier) and one `signb` signal to control the sign representation of both data B inputs. Therefore, all of the data A inputs feeding the same embedded multiplier must have the same sign representation. Similarly, all of the data B inputs feeding the same embedded multiplier must have the same sign representation.

Figure 15–5 shows a 484-pin FineLine BGA package outline.

Figure 15–5. 484-Pin FineLine BGA Package Outline