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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, MI Bus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912d60acfu8

Section 23. Appendix: Information on MC68HC912D60A Mask Set Changes

Technical Data — Glossary

Technical Data — Revision History

1.3 Devices Covered in this Document

The MC68HC912D60C and MC68HC912D60P are devices similar to the MC68HC912D60A, but with different oscillator configurations. Refer to Section 12. Oscillator for more details.

The generic term MC68HC912D60A is used throughout this document to mean all derivatives mentioned above, except in Section 12. Oscillator, where it refers only to the MC68HC912D60A device.

1.4 Features

- 16-bit CPU12
  - Upward compatible with M68HC11 instruction set
  - Interrupt stacking and programmer's model identical to M68HC11
  - 20-bit ALU
  - Instruction queue
  - Enhanced indexed addressing
- Multiplexed bus
  - Single chip or expanded
  - 16 address/16 data wide or 16 address/8 data narrow mode
- Two 8-bit ports with key wake-up interrupt (2 pins only are available on 80QFP) and one I^2C start bit detector (112TQFP only)
- Memory
  - 60K byte flash EEPROM, made of a 28K module and a 32K module with 8K bytes protected BOOT section in each module (MC68HC912D60A)
  - 1K byte EEPROM
  - 2K byte RAM

1.6 Block Diagrams

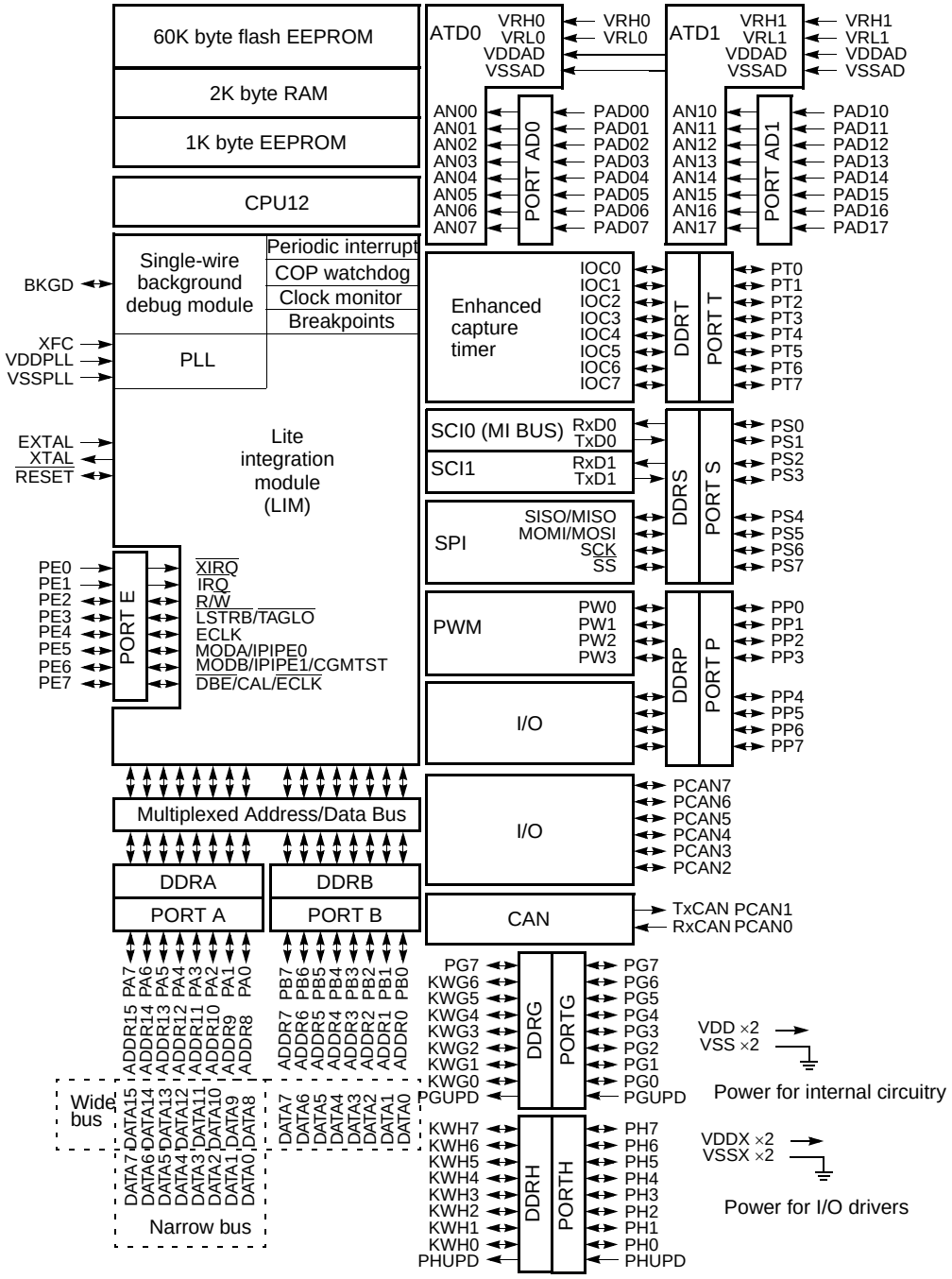

Figure 1-1. MC68HC912D60A 112-pin QFP Block Diagram

Table 3-2. MC68HC912D60A Signal Description Summary

Pin Name	Pin Number		Description
	80-pin	112-pin	
ADDR[7:0] DATA[7:0]	23–16	31–24	External bus pins share function with general-purpose I/O ports A and B. In single chip modes, the pins can be used for I/O. In expanded modes, the pins are used for the external buses.
ADDR[15:8] DATA[15:8]	48–41	64–57	
$\overline{\text{DBE}}$	25	36	Data bus control and, in expanded mode, enables the drive control of external buses during external reads.
$\overline{\text{ECLK}}$	25	36	Inverted ECLK used to latch the address.
CAL	25	36	CAL is the output of the Slow Mode programmable clock divider, SLWCLK, and is used as a calibration reference for functions such as time of day. It is overridden when DBE function is enabled. It always has a 50% duty cycle.
CGMTST	26	37	Clock generation module test output.
MODB/ IPIPE1, MODA/ IPIPE0	26, 27	37, 38	State of mode select pins during reset determine the initial operating mode of the MCU. After reset, MODB and MODA can be configured as instruction queue tracking signals IPIPE1 and IPIPE0 or as general-purpose I/O pins.
ECLK	28	39	E Clock is the output connection for the external bus clock. ECLK is used as a timing reference and for address demultiplexing.
$\overline{\text{LSTRB}}$/ $\overline{\text{TAGLO}}$	37	53	Low byte strobe (0 = low byte valid), in all modes this pin can be used as I/O. The low strobe function is the exclusive-NOR of A0 and the internal $\overline{\text{SZ8}}$ signal. (The $\overline{\text{SZ8}}$ internal signal indicates the size 16/8 access.) Pin function $\overline{\text{TAGLO}}$ used in instruction tagging. See Development Support.
R/$\overline{\text{W}}$	38	54	Indicates direction of data on expansion bus. Shares function with general-purpose I/O. Read/write in expanded modes.
$\overline{\text{IRQ}}$	39	55	Maskable interrupt request input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register).
$\overline{\text{XIRQ}}$	40	56	Provides a means of requesting asynchronous nonmaskable interrupt requests after reset initialization
SMODN/BKGD/$\overline{\text{TAGHI}}$	15	23	Single-wire background interface pin is dedicated to the background debug function. During reset, this pin determines special or normal operating mode. Pin function $\overline{\text{TAGHI}}$ used in instruction tagging. See Development Support.
PW[3:0]	80, 1–3	112, 1–3	Pulse Width Modulator channel outputs.
$\overline{\text{SS}}$	70	96	Slave select output for SPI master mode, input for slave mode or master mode.
SCK	69	95	Serial clock for SPI system.

5.5.4 Miscellaneous System Control Register

Additional mapping and external resource controls are available. To use external resources the part must be operated in one of the expanded modes.

	Bit 7	6	5	4	3	2	1	Bit 0	
	MAPROM	NDRF	RFSTR1	RFSTR0	EXSTR1	EXSTR0	ROMON28	ROMON32	
RESET:	0	0	0	0	1	1	0	0	Exp Modes
RESET:	0	0	0	0	1	1	1	1	SC Modes

MISC — Miscellaneous Mapping Control Register **$0013**

Normal modes: write once; Special modes: write anytime. Read anytime.

MAPROM — Map Location of ROM

This bit is used to swap the location of the on-chip Flash EEPROM.

0 = 28K byte array is mapped from $1000 to $7FFF, 32K byte array is mapped from $8000 to $FFFF.

1 = 28K byte is mapped from $9000 to $FFFF, 32K byte array is mapped from $0000 to $7FFF.

NDRF — Narrow Data Bus for Register-Following Map Space

This bit enables a narrow bus feature for the 512 byte Register-Following Map. This is useful for accessing 8-bit peripherals and allows 8-bit and 16-bit external memory devices to be mixed in a system. In Expanded Narrow (eight bit) modes, Single Chip Modes, and Peripheral mode, this bit has no effect.

0 = Makes Register-Following MAP space act as a full 16 bit data bus.

1 = Makes the Register-Following MAP space act the same as an 8 bit only external data bus (data only goes through port A externally).

The Register-Following space is mapped from $0200 to $03FF after reset, which is next to the register map. If the registers are moved this space follows.

8.6 Program/Erase Operation

A program or erase operation should follow the sequence below if AUTO bit is clear:

1. Write BYTE, ROW and ERASE to desired value, write EELAT = 1
2. Write a byte or an aligned word to an EEPROM address
3. Write EEPGM = 1
4. Wait for programming, t_{PROG} or erase, t_{ERASE} delay time (10ms)
5. Write EEPGM = 0
6. Write EELAT = 0

If the AUTO bit is set, steps 4 and 5 can be replaced by a step to poll the EEPGM bit until it is cleared.

It is possible to program/erase more bytes or words without intermediate EEPROM reads, by jumping from step 5 to step 2.

8.7 Shadow Word Mapping

The shadow word is mapped to location $_FC0 and $_FC1 when the NOSHW bit in EEMCR register is zero. The value in the shadow word is loaded to the EEMCR, EEDIVH and EEDIVL after reset. Table 8-4 shows the mapping of each bit from shadow word to the registers

Table 8-4. Shadow word mapping

Shadow word location	Register / Bit
$_FC0 bit 7	EEMCR / NOBDML
$_FC0, bit 6	EEMCR / NOSHW
$_FC0, bit 5	EEMCR / bit 5(1)
$_FC0, bit 4	EEMCR / FPOPEN
$_FC0, bit 3:2	not mapped(2)
$_FC0, bit 1:0	EEDIVH / bit 1:0
$_FC1, bit 7:0	EEDIVCLK / bit 7:0

1. Reserved for testing. Must be set to one in user application.
2. Reserved. Must be set to one in user application for future compatibility.

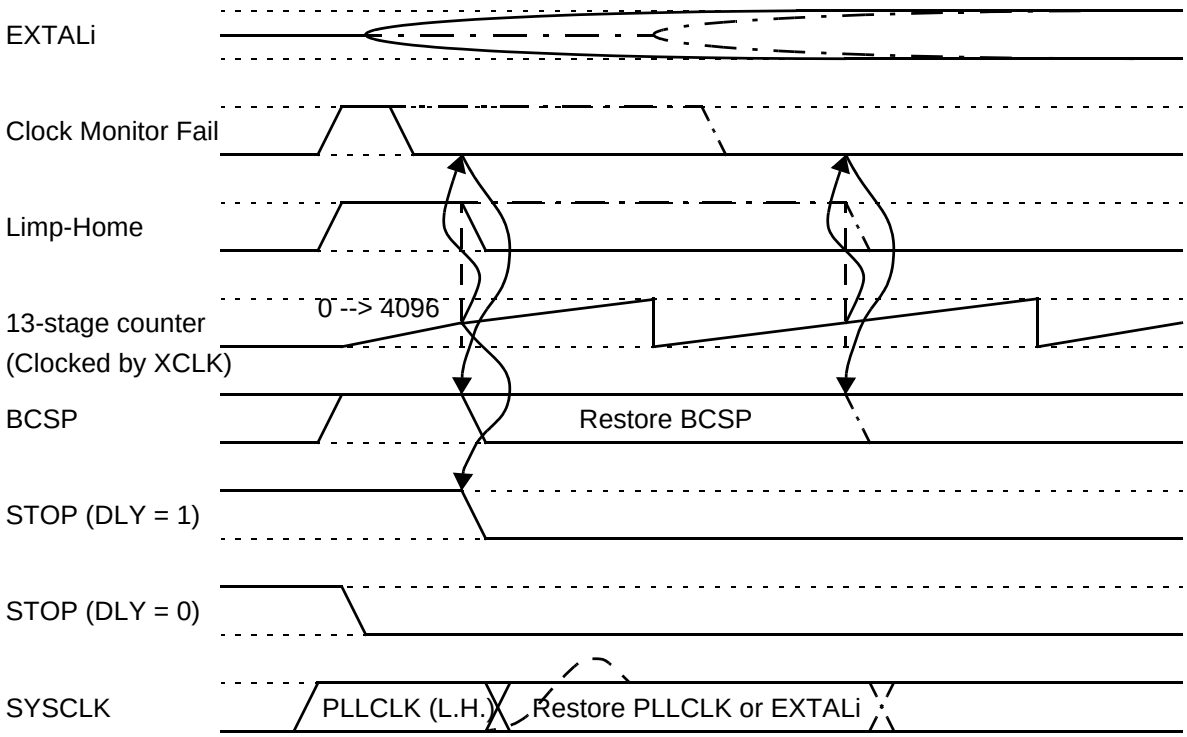

Figure 11-5. STOP Exit and Fast STOP Recovery

11.6.4 STOP exit without Limp Home mode, clock monitor disabled

(NOLHM=1, CME=0, DLY=X)

If Limp home mode is disabled (V_{DDPLL}=V_{SS} or NOLHM bit set) and the CME (or FCME) bit is cleared, the MCU goes into STOP mode when a STOP instruction is executed.

If EXTALi clock is present then exit from STOP will occur normally using this clock. Under this condition, DLY should always be set to allow the crystal to stabilise and minimise the risk of code runaway. With DLY=1 execution resumes after a delay of 4096 XCLK cycles.

NOTE: *The external clock signal should stabilise within the 4096 reset counter cycles.* ***Use of DLY=0 is not recommended due to this requirement.***

	Bit 7	6	5	4	3	2	1	Bit 0
	0	BCSP	BCSS	0	0	MCS	0	0
RESET:	0	0	0	0	0	0	0	0

CLKSEL — Clock Generator Clock select Register **$003D**

Read and write anytime. Exceptions are listed below for each bit.

BCSP and BCSS bits determine the clock used by the main system including the CPU and buses.

BCSP — Bus Clock Select PLL

0 = SYSCLK is derived from the crystal clock or from SLWCLK.
1 = SYSCLK source is the PLL.

Cannot be set when PLLON = 0. In limp-home mode, the output of BCSP is forced to 1, but the BCSP bit reads the latched value.

BCSS — Bus Clock Select Slow

0 = SYSCLK is derived from the crystal clock EXTALi.
1 = SYSCLK source is the Slow clock SLWCLK.

This bit has no effect when BCSP is set.

MCS — Module Clock Select

0 = M clock is the same as PCLK.
1 = M clock is derived from Slow clock SLWCLK.

This bit determines the clock used by the ECT module and the baud rate generators of the SCIs. In limp-home mode, the output of MCS is forced to 0, but the MCS bit reads the latched value.

12.4.4 MC68HC912D60C DC Blocking Capacitor Guidelines

Due to the placement of the resonator from EXTAL to VSS and the nature of the microcontroller's inputs, there will be a DC bias voltage of approximately (VDD–2V) across the pins of the resonator. For some resonators, this can have long-term reliability issues. To remedy this situation, a DC-blocking capacitor can be placed in series with the crystal, as shown in Figure 12-3.

The value of the DC-blocking capacitor should be between 0.1 and 10nF, with a preferred value of 1nF. This capacitor must be connected as shown in Figure 12-3. If connected thus, all other oscillator specifications and guidelines continue to apply.

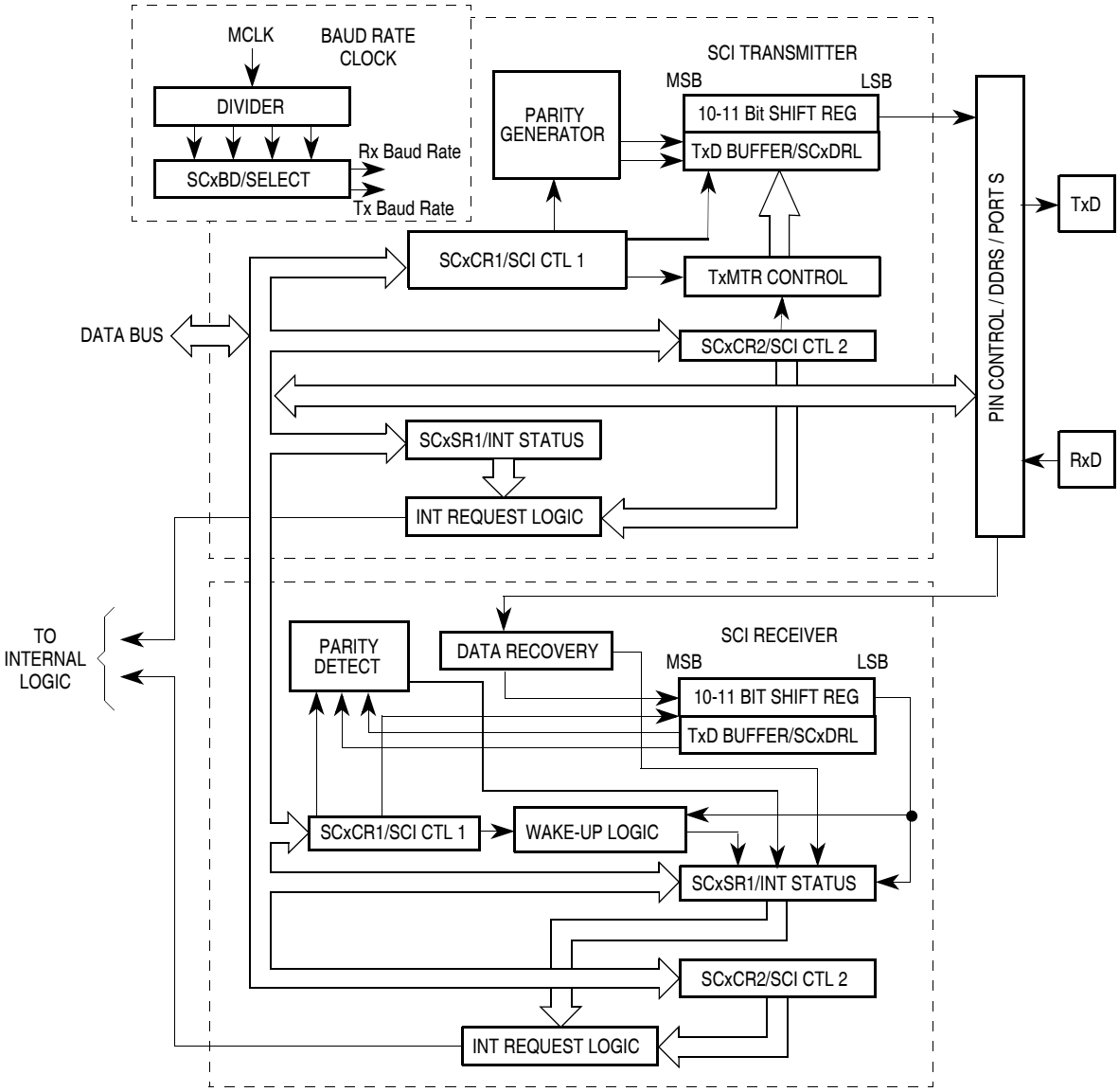

Figure 15-2. Serial Communications Interface Block Diagram

PT — MI Bus TxD0 polarity

If parity is enabled, this bit determines even or odd parity for both the receiver and the transmitter.

0 = MI Bus transmit pin functions normally.

1 = MI Bus transmit pin will send inverted data.

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	RIE	—	TE	RE	—	SBK
RESET:	0	0	0	0	0	0	0	0

SC0CR2 — MI Bus Control Register 2 **$00C3**

Read or write anytime.

RIE — Receiver Interrupt Enable

0 = RDRF interrupt disabled.

1 = MI Bus interrupt will be requested whenever the RDRF status flag is set.

OR does not generate an interrupt request in MI Bus mode.

TE — Transmitter Enable

0 = Transmitter disabled.

1 = MI Bus transmit logic is enabled and the TxD0 pin (Port S bit 1) is dedicated to the transmitter.

RE — Receiver Enable

0 = Receiver disabled.

1 = Port pin dedicated to the MI Bus; the receiver is enabled by a pull sync and is inhibited during a push field.

SBK — Send Break

0 = No action.

1 = MI transmit line is set low for 20 time slots.

When an MI Bus wire is held low for eight or more time slots an internal circuit on any slave device connected to the bus may reset or preset the device with default values.

17.6 Interrupts

The msCAN12 supports four interrupt vectors mapped onto eleven different interrupt sources, any of which can be individually masked (for details see msCAN12 Receiver Flag Register (CRFLG) to msCAN12 Transmitter Control Register (CTCR)):

- *Transmit interrupt*: At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXE flags of the empty message buffers are set.
- *Receive interrupt*: A message has been successfully received and loaded into the foreground receive buffer. This interrupt is generated immediately after receiving the EOF symbol. The RXF flag is set.
- *Wake-up interrupt*: An activity on the CAN bus occurred during msCAN12 internal SLEEP mode.
- *Error interrupt*: An overrun, error or warning condition occurred. The receiver flag register (CRFLG) indicates one of the following conditions:
  - *Overrun:* an overrun condition as described in Receive Structures has occurred.
  - *Receiver warning*: the receive error counter has reached the CPU warning limit of 96.
  - *Transmitter warning*: the transmit error counter has reached the CPU warning limit of 96.
  - *Receiver error passive*: the receive error counter has exceeded the error passive limit of 127 and msCAN12 has gone to error passive state.
  - *Transmitter error passive*: the transmit error counter has exceeded the error passive limit of 127 and msCAN12 has gone to error passive state.
  - *Bus off*: the transmit error counter has exceeded 255 and msCAN12 has gone to BUSOFF state.

mode is required, the existing continuous sequence must be interrupted, the control registers modified, and a new conversion sequence initiated.

MULT — Multi-Channel Sample Mode

0 = Sample only the specified channel

1 = Sample across many channels

When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CC/CB/CA located in ATDCTL5).

When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S1C control bits). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code.

SC — Special Channel Conversion Mode

0 = Perform A/D conversion on an analog input channel

1 = Perform special channel A/D conversion

SC determines if the ATD module performs A/D conversions on any of the analog input channels (normal operation) or whether it performs a conversion on one of the defined, special channels. The special channels are normally used to test the A/D machine and include converting the high and low reference potentials for the module. The control bits CC/CB/CA are used to indicate which special channel is to be converted.

Table 18-8. Special Channel Conversion Select Coding

CC	CB	CA	Special	Expected
			Channel	Digital Result Code
0	X	X	reserved	–
1	0	0	VRH	$FF
1	0	1	VRL	$00
1	1	0	(VRH + VRL)/2	$7F
1	1	1	reserved	–

18.9.6 ATDTEST Module Test Register (ATDTEST)

The test registers implement various special (test) modes used to test the ATD module. The reset bit in ATDTEST1 is always read/write. The SAR (successive approximation register) can always be read but only written in special (test) mode.

The functions implemented by the test registers are reserved for factory test.

ATD0TESTH/ATD1TESTH — ATD Test Register **$0068/$01E8**

	Bit 7	6	5	4	3	2	1	Bit 0
	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
RESET:	0	0	0	0	0	0	0	0

ATD0TESTL/ATD1TESTL — ATD Test Register **$0069/$01E9**

	Bit 7	6	5	4	3	2	1	Bit 0
	SAR1	SAR0	RST	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SAR[9:0] — Successive Approximation Register

This ten bit value represents the contents of the AD machine's successive approximation register. This value can always be read. It can only be written in special (test) mode. Note that ATDTEST0 acts as a ten bit register since the entire SAR is read/written when accessing this address.

RST — Test Mode Reset Bit

0 = No reset

1 = Reset the ATD module

When set, this bit causes the ATD module to reset itself. This sets all registers to their reset state (note the reset state of the reset bit is zero), the current conversion and conversion sequence are aborted, pending interrupts are cleared, and the module is placed in an idle mode.

19.4 Background Debug Mode

Background debug mode (BDM) is used for system development, in-circuit testing, field testing, and programming. BDM is implemented in on-chip hardware and provides a full set of debug options.

Because BDM control logic does not reside in the CPU, BDM hardware commands can be executed while the CPU is operating normally. The control logic generally uses free CPU cycles to execute these commands, but can steal cycles from the CPU when necessary. Other BDM commands are firmware based, and require the CPU to be in active background mode for execution. While BDM is active, the CPU executes a firmware program located in a small on-chip ROM that is available in the standard 64-Kbyte memory map only while BDM is active.

The BDM control logic communicates with an external host development system serially, via the BKGD pin. This single-wire approach minimizes the number of pins needed for development support.

19.4.1 Enabling BDM Firmware Commands

BDM is available in all operating modes, but must be made active before firmware commands can be executed. BDM is enabled by setting the ENBDM bit in the BDM STATUS register via the single wire interface (using a hardware command; WRITE_BD_BYTE at $FF01). BDM must then be activated to map BDM registers and ROM to addresses $FF00 to $FFFF and to put the MCU in active background mode.

After the firmware is enabled, BDM can be activated by the hardware BACKGROUND command, by the BDM tagging mechanism, or by the CPU BGND instruction. An attempt to activate BDM before firmware has been enabled causes the MCU to resume normal instruction execution after a brief delay.

BDM becomes active at the next instruction boundary following execution of the BDM BACKGROUND command, but tags activate BDM before a tagged instruction is executed.

Table 20-15. SPI Timing

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H , 200 pF load on all SPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	f_{op}	$f_{eclk}/256$ $f_{eclk}/256$	4 4	MHz
1	SCK Period Master Slave	t_{sck}	2 2	256 —	t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	1/2 1	— —	t_{sck} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	1/2 1	— —	t_{sck} t_{cyc}
4	Clock (SCK) High or Low Time Master Slave	t_{wsck}	t_{cyc} – 30 t_{cyc} – 30	128 t_{cyc} —	ns ns
5	Sequential Transfer Delay Master Slave	t_{td}	1/2 1	— —	t_{sck} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	30 30	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	0 30	— —	ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	1	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	— —	50 50	ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	0 0	— —	ns ns
12	Rise Time Input Output	t_{ri} t_{ro}	— —	t_{cyc} – 30 30	ns ns
13	Fall Time Input Output	t_{fi} t_{fo}	— —	t_{cyc} – 30 30	ns ns

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

Glossary

binary-coded decimal (BCD) — A notation that uses 4-bit binary numbers to represent the 10 decimal digits and that retains the same positional structure of a decimal number. For example,

234 (decimal) = 0010 0011 0100 (BCD)

bit — A binary digit. A bit has a value of either logic 0 or logic 1.

branch instruction — An instruction that causes the CPU to continue processing at a memory location other than the next sequential address.

break module — The break module allows software to halt program execution at a programmable point in order to enter a background routine.

breakpoint — A number written into the break address registers of the break module. When a number appears on the internal address bus that is the same as the number in the break address registers, the CPU executes the software interrupt instruction (SWI).

break interrupt — A software interrupt caused by the appearance on the internal address bus of the same value that is written in the break address registers.

bus — A set of wires that transfers logic signals.

bus clock — See "CPU clock".

byte — A set of eight bits.

CAN — See "Scalable CAN."

CCR — See “condition code register.”

central processor unit (CPU) — The primary functioning unit of any computer system. The CPU controls the execution of instructions.

CGM — See “clock generator module (CGM).”

clear — To change a bit from logic 1 to logic 0; the opposite of set.

clock — A square wave signal used to synchronize events in a computer.

clock generator module (CGM) — The CGM module generates a base clock signal from which the system clocks are derived. The CGM may include a crystal oscillator circuit and/or phase-locked loop (PLL) circuit.

comparator — A device that compares the magnitude of two inputs. A digital comparator defines the equality or relative differences between two binary numbers.

two’s complement — A means of performing binary subtraction using addition techniques. The most significant bit of a two’s complement number indicates the sign of the number (1 indicates negative). The two’s complement negative of a number is obtained by inverting each bit in the number and then adding 1 to the result.

unbuffered — Utilizes only one register for data; new data overwrites current data.

unimplemented memory location — A memory location that is not used. Writing to an unimplemented location has no effect. Reading an unimplemented location returns an unpredictable value.

variable — A value that changes during the course of program execution.

VCO — See "voltage-controlled oscillator."

vector — A memory location that contains the address of the beginning of a subroutine written to service an interrupt or reset.

voltage-controlled oscillator (VCO) — A circuit that produces an oscillating output signal of a frequency that is controlled by a dc voltage applied to a control input.

waveform — A graphical representation in which the amplitude of a wave is plotted against time.

wired-OR — Connection of circuit outputs so that if any output is high, the connection point is high.

word — A set of two bytes (16 bits).

write — The transfer of a byte of data from the CPU to a memory location.

Section	Page (in Rev 2.0)	Description of change
EEPROM Memory	110, 111	FPOPEN bit added to EEMCR register
Clock Functions	139	Note added about consideration of crystal selection due to EMC emissions
Oscillator	New section	
MSCAN Controller	317	First two bullets of sleep mode description updated
	331	SLPRQ = 1 description updated
Analog-to-Digital Converter	350	*signed/unsigned* removed from result data bullet
	352	*signed/unsigned* reference removed from note
	359, 361	DSGN bit removed from ATD0CTL2/ATD1CTL2 register diagram and bit descriptions. Table 18-1 and Table 18-2 updated accordingly
	376	DSGN bit references removed from ADR0-15 description
Electrical Specifications	411	Reference to supply differential voltage values updated. V_{REF} differential voltage row removed Analog input differential voltage row added
	413	f_{XTAL} removed
	413	Footnote added restricting external oscillator operating frequency to 8MHz when using a quartz crystal
	425	Table footnote removed from Table 20-16 regarding V_{DDPLL}
Appendix: Changes from MC68HC912D60	438	Sentence removed from end of paragraph in Flash External Programming Voltage.
	441	DSGN reference removed from Additional Features.
Appendix: CGM Practical Aspects	427	Section 21.3 A Few Hints For The CGM Crystal Oscillator Application removed. All points are covered in new Oscillator section.
	435	Extra bullets added
Appendix: Information on MC68HC912D60A Mask Set Changes	New Section	

23.11 Major Changes From Rev 0.0 to Rev 1.0

The Advance Information data book was converted to Technical Data book status. This constituted only a change of cover.