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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, MI Bus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912d60acfue8

List of Tables

RFSTR1, RFSTR0 — Register Following Stretch

This two bit field determines the amount of clock stretch on accesses to the 512 byte Register Following Map. It is valid regardless of the state of the NDRF bit. In Single Chip and Peripheral Modes this bit has no meaning or effect.

Table 5-3. RFSTR Stretch Bit Definition

RFSTR1	RFSTR0	Number of E Clocks Stretched
0	0	0
0	1	1
1	0	2
1	1	3

EXSTR1, EXSTR0 — External Access Stretch

This two bit field determines the amount of clock stretch on accesses to the External Address Space. In Single Chip and Peripheral Modes this bit has no meaning or effect.

Table 5-4. EXSTR Stretch Bit Definition

EXSTR1	EXSTR0	Number of E Clocks Stretched
0	0	0
0	1	1
1	0	2
1	1	3

ROMON28, ROMON32 — Enable bits for ROM

These bits are used to enable the Flash EEPROM arrays FEE28 and FEE32 respectively.

0 = Corresponding Flash EEPROM array disabled from the memory map.

1 = Corresponding Flash EEPROM array enabled in the memory map.

FEESWAI — Flash EEPROM Stop in Wait Control

0 = Do not halt Flash EEPROM clock when the part is in wait mode.
0 = Halt Flash EEPROM clock when the part is in wait mode.

HVEN — High-Voltage Enable

This bit enables the charge pump to supply high voltages for program and erase operations in the array. HVEN can only be set if either PGM or ERAS are set and the proper sequence for program or erase is followed.

0 = Disables high voltage to array and charge pump off
1 = Enables high voltage to array and charge pump on

ERAS — Erase Control

This bit configures the memory for erase operation. ERAS is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to1 at the same time.

0 = Erase operation is not selected.
1 = Erase operation selected.

PGM — Program Control

This bit configures the memory for program operation. PGM is interlocked with the ERAS bit such that both bits cannot be equal to 1 or set to1 at the same time.

0 = Program operation is not selected.
1 = Program operation selected.

7.7 Operation

The Flash EEPROM can contain program and data. On reset, it can operate as a bootstrap memory to provide the CPU with internal initialization information during the reset sequence.

7.7.1 Bootstrap Operation Single-Chip Mode

After reset, the CPU controlling the system will begin booting up by fetching the first program address from address $FFFE.

EEPROT — EEPROM Block Protect **$00F1**

	Bit 7	6	5	4	3	2	1	Bit 0
	SHPROT	1	1	BPROT4	BPROT3	BPROT2	BPROT1	BPROT0
RESET:	1	1	1	1	1	1	1	1

Prevents accidental writes to EEPROM. Read anytime. Write anytime if EEPGM = 0 and PROTLCK = 0.

SHPROT — SHADOW Word Protection

0 = The SHADOW word can be programmed and erased.

1 = The SHADOW word is protected from being programmed and erased.

BPROT[4:0] — EEPROM Block Protection

0 = Associated EEPROM block can be programmed and erased.

1 = Associated EEPROM block is protected from being programmed and erased.

Table 8-2. 1K byte EEPROM Block Protection

Bit Name	Block Protected	Block Size
BPROT4	$0C00 to $0DFF	512 Bytes
BPROT3	$0E00 to $0EFF	256 Bytes
BPROT2	$0F00 to $0F7F	128 Bytes
BPROT1	$0F80 to $0FBF	64 Bytes
BPROT0	$0FC0 to $0FFF	64 Bytes

EEPROM location at address $0FC0 and $0FC1. Do not program other bits of the high byte of the SHADOW word (location $0FC0); otherwise some regular EEPROM array locations will not be visible. At the next reset, the SHADOW values are loaded into the EEDIVH and EEDIVL registers. They do not require further initialization as long as the oscillator frequency of the target application is not changed.

5. Protect the SHADOW word by setting SHPROT bit in EEPROT register.

Section 9. Resets and Interrupts

9.1 Contents

9.2 Introduction

CPU12 exceptions include resets and interrupts. Each exception has an associated 16-bit vector, which points to the memory location where the routine that handles the exception is located. Vectors are stored in the upper 128 bytes of the standard 64K byte address map.

The six highest vector addresses are used for resets and non-maskable interrupt sources. The remainder of the vectors are used for maskable interrupts, and all must be initialized to point to the address of the appropriate service routine.

9.2.1 Exception Priority

A hardware priority hierarchy determines which reset or interrupt is serviced first when simultaneous requests are made. Six sources are not

	Bit 7	6	5	4	3	2	1	Bit 0
	KWIFH7	KWIFH6	KWIFH5	KWIFH4	KWIFH3	KWIFH2	KWIFH1	KWIFH0
RESET:	0	0	0	0	0	0	0	0

KWIFH — Key Wake-up Port H Flag Register **$002F**

Read and write anytime.

Each flag is set by a falling edge on its associated input pin. To clear the flag, write one to the corresponding bit in KWIFH.

KWIFH[7:0] — Key Wake-up Port H Flags

0 = Falling edge on the associated bit has not occurred

1 = Falling edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set)

10.4 Key Wake-Up Input Filter

The KWU input signals are filtered by a digital filter which is active only during STOP mode. The purpose of the filter is to prevent single pulses shorter than a specified value from waking the part from STOP.

The filter is composed of an internal oscillator and a majority voting logic. The filter oscillator starts the oscillation by detecting a triggering edge on an input if the corresponding interrupt enable bit is set. The majority voting logic takes three samples of an asserted input pin at each filter oscillator period and if two samples are taken at the triggering level, the filter recognizes a valid triggering level and sets the corresponding interrupt flag. In this way the majority voting logic rejects the short non-triggering state between two incoming triggering pulses. As the filter is shared with all KWU inputs, the filter considers any pulse coming from any input pin for which the corresponding interrupt enable bit is set.

The timing specification is given for a single pulse. The time interval between the triggering edges of two following pulses should be greater than the t_{KWSP} in order to be considered as a single pulse by the filter. If

the transition, the clock select output will be held low and all CPU activity will cease until the transition is complete.

The Module Clock Select bit MCS determines the clock used by the ECT module and the baud rate generators of the SCIs. In limp-home mode, the output of MCS is forced to 0, but the MCS bit reads the latched value. It allows normal operation of the serial and timer subsystems at a fixed reference frequency while allowing the CPU to operate at a higher, variable frequency.

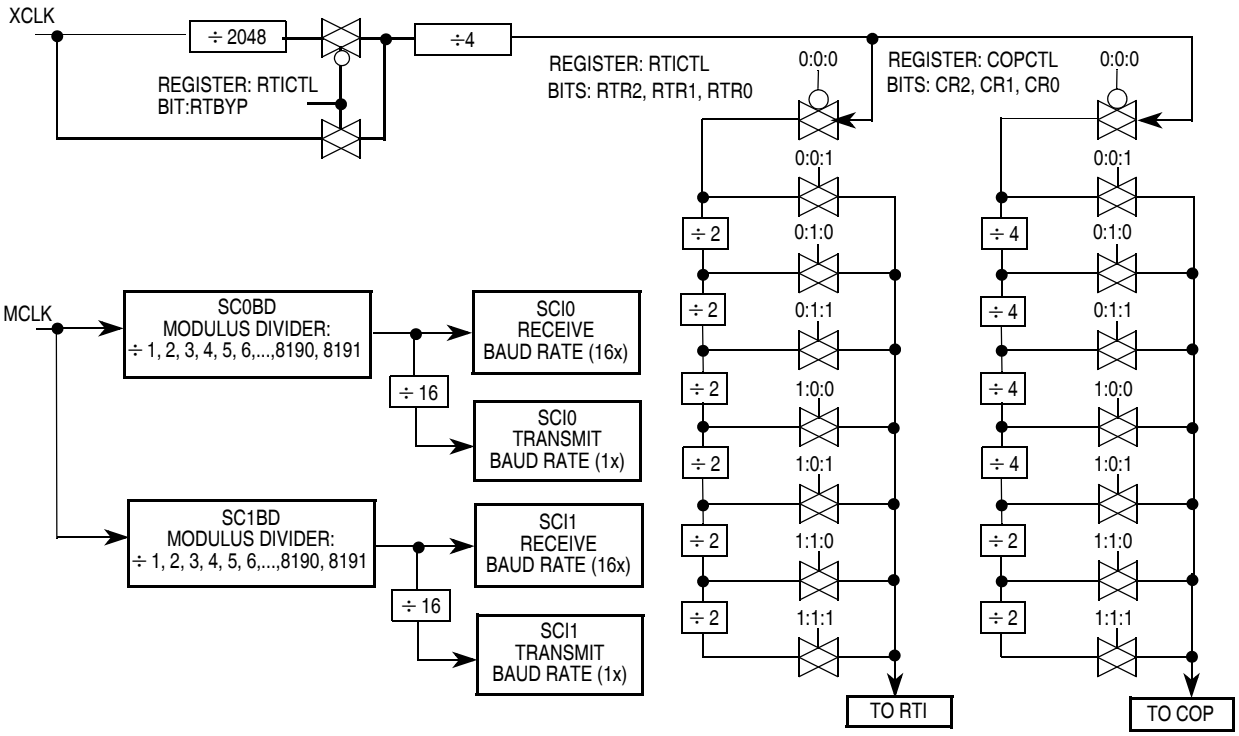

Figure 11-7. Clock Chain for SCI0, SCI1, RTI, COP

Table 12-1. MC68HC912D60C EXTAL–XTAL Capacitor Values vs. Maximum ESR, Shunt Capacitance, and VDDPLL setting

Maximum ESR vs. EXTAL–XTAL capacitor value, 1MHz resonators

Shunt Capacitance (pF) (VDDPLL=VDD)	**3**	1570	2080	2620	2700	1870	1140	630	170		
	5	1460	1890	2340	2010	1370	830	460	120		
	7	1350	1730	2100	1550	1050	630	350	90		
	10	1210	1520	1600	1100	740	440	240	60		
$C_{EXTAL-XTAL}$ (pF)		100pF	82pF	68pF	56pF	47pF	39pF	33pF	27pF	22pF	18pF

Maximum ESR vs. EXTAL–XTAL capacitor value, 2MHz resonators

Shunt Capacitance (pF) (VDDPLL=VDD)	**3**	360	480	620	780	940	1100	1080	730	440	240
	5	340	450	570	700	830	950	800	530	320	170
	7	320	410	520	630	740	830	620	410	250	130
	10	290	370	450	550	620	600	440	290	170	90
$C_{EXTAL-XTAL}$ (pF)		100pF	82pF	68pF	56pF	47pF	39pF	33pF	27pF	22pF	18pF

Maximum ESR vs. EXTAL–XTAL capacitor value, 4MHz resonators

Shunt Capacitance (pF) (VDDPLL=VDD)	**3**	210	255	290	335	370	340	175	80
	5	190	225	254	290	310	255	130	60
	7	170	200	227	250	270	200	100	45
	10	145	170	190	205	205	140	70	25
Shunt Capacitance (pF) (VDDPLL=0)	**3**	250	300	350	400	440	325	165	75
	5	225	265	305	340	345	245	120	55
	7	200	235	265	295	270	190	90	40
	10	175	200	220	240	195	135	65	20
$C_{EXTAL-XTAL}$ (pF)		47pF	39pF	33pF	27pF	22pF	18pF	13pF	10pF

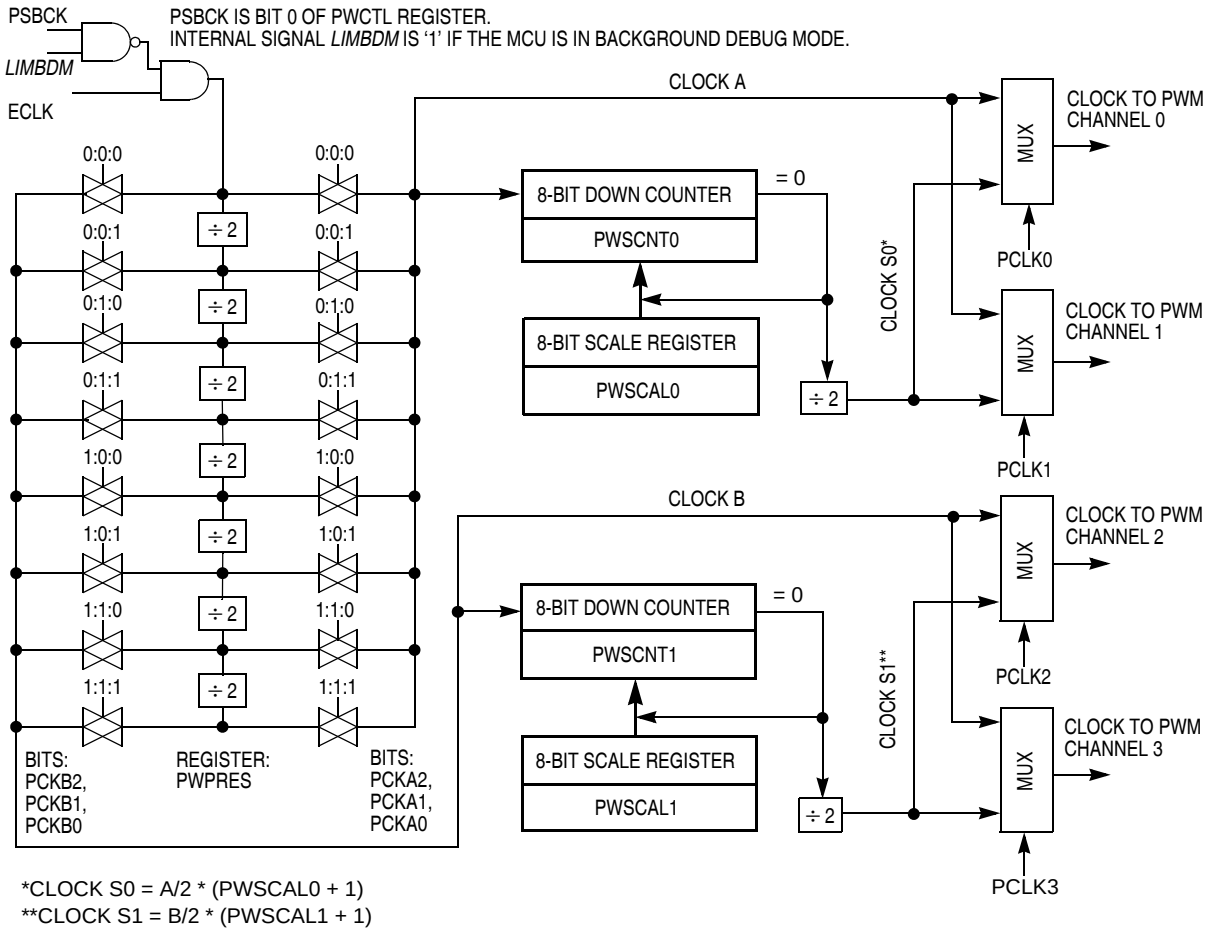

Figure 13-3. PWM Clock Sources

13.3 PWM Register Description

	Bit 7	6	5	4	3	2	1	Bit 0
	CON23	CON01	PCKA2	PCKA1	PCKA0	PCKB2	PCKB1	PCKB0
RESET:	0	0	0	0	0	0	0	0

PWCLK — PWM Clocks and Concatenate **$0040**

Read and write anytime.

At the same time the pulse accumulator is cleared.

14.3.3 Modulus Down-Counter

The modulus down-counter can be used as a time base to generate a periodic interrupt. It can also be used to latch the values of the IC registers and the pulse accumulators to their holding registers.

The action of latching can be programmed to be periodic or only once.

14.4 Timer Registers

Input/output pins default to general-purpose I/O lines until an internal function which uses that pin is specifically enabled. The timer overrides the state of the DDR to force the I/O state of each associated port line when an output compare using a port line is enabled. In these cases the data direction bits will have no affect on these lines.

When a pin is assigned to output an on-chip peripheral function, writing to this PORTT bit does not affect the pin but the data is stored in an internal latch such that if the pin becomes available for general-purpose output the driven level will be the last value written to the PORTT bit.

	Bit 7	6	5	4	3	2	1	Bit 0
	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
RESET:	0	0	0	0	0	0	0	0

TIOS — Timer Input Capture/Output Compare Select **$0080**

Read or write anytime.

IOS[7:0] — Input Capture or Output Compare Channel Configuration
0 = The corresponding channel acts as an input capture
1 = The corresponding channel acts as an output compare.

Table 14-1. Compare Result Output Action

OMn	OLn	Action
0	0	Timer disconnected from output pin logic
0	1	Toggle OCn output line
1	0	Clear OCn output line to zero
1	1	Set OCn output line to one

To operate the 16-bit pulse accumulators A and B (PACA and PACB) independently of input capture or output compare 7 and 0 respectively the user must set the corresponding bits IOSn = 1, OMn = 0 and OLn = 0. OC7M7 or OC7M0 in the OC7M register must also be cleared.

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
RESET:	0	0	0	0	0	0	0	0

TCTL3 — Timer Control Register 3 **$008A**

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
RESET:	0	0	0	0	0	0	0	0

TCTL4 — Timer Control Register 4 **$008B**

Read or write anytime.

EDGnB, EDGnA — Input Capture Edge Control

These eight pairs of control bits configure the input capture edge detector circuits.

Table 14-2. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

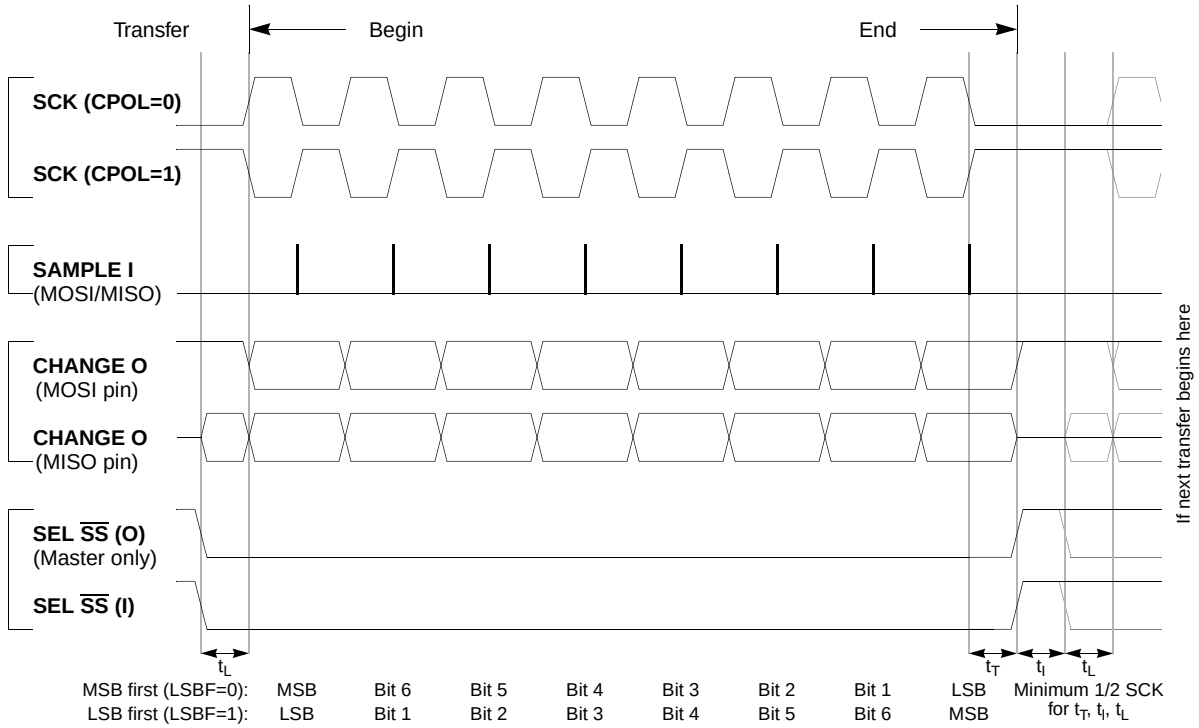

Figure 15-5. SPI Clock Format 1 (CPHA = 1)

15.5.3 $\overline{SS}$ Output

Available in master mode only, $\overline{SS}$ output is enabled with the SSOE bit in the SP0CR1 register if the corresponding DDRS is set. The $\overline{SS}$ output pin will be connected to the $\overline{SS}$ input pin of the external slave device. The $\overline{SS}$ output automatically goes low for each transmission to select the external device and it goes high during each idling state to deselect external devices.

Table 15-3. $\overline{SS}$ Output Selection

DDS7	SSOE	Master Mode	Slave Mode
0	0	SS Input with MODF Feature	SS Input
0	1	Reserved	SS Input
1	0	General-Purpose Output	SS Input
1	1	SS Output	SS Input

	Bit 7	6	5	4	3	2	1	Bit 0
	0	RDPS2	RDPS1	RDPS0	0	PUPS2	PUPS1	PUPS0
RESET:	0	0	0	0	0	0	0	0

PURDS — Pull-Up Register for Port S **$00D9**

RDPS2 — Reduce Drive of Port S[7:4]
0 = Port S[7:4] output drivers operate normally
1 = Port S[7:4] output pins have reduced drive capability for lower power and less noise

RDPS1 — Reduce Drive of Port S[3:2]
0 = Port S[3:2] output drivers operate normally
1 = Port S[3:2] output pins have reduced drive capability for lower power and less noise

RDPS0 — Reduce Drive of Port S[1:0]
0 = Port S[1:0] output drivers operate normally
1 = Port S[1:0] output pins have reduced drive capability for lower power and less noise

PUPS2 — Pull-up Port S[7:4] Enable
0 = No internal pull-ups on port S[7:4]
1 = Port S[7:4] input pins have an active pull-up device. If a pin is programmed as output, the pull-up device becomes inactive.

PUPS1 — Pull-up Port S[3:2] Enable
0 = No internal pull-ups on port S[3:2]
1 = Port S[3:2] input pins have an active pull-up device. If a pin is programmed as output, the pull-up device becomes inactive.

PUPS0 — Pull-up Port S[1:0] Enable
0 = No internal pull-ups on port S[1:0]
1 = Port S[1:0] input pins have an active pull-up device. If a pin is programmed as output, the pull-up device becomes inactive.

16.7 MI Bus clock rate

The MI Bus clock rate is set via the SCI baud registers. To use the MI Bus, the MCLK clock frequency that drives the SCI clock generator must be selected to match the minimum resolution of the MI Bus logic. This is expressed by the following formula:

MCLK = 16 • n • (2 • Push_field_bit_rate) = 16 • n • 40kHz = n • 640kHz

where ‘n’ is an integer and 20kHz is the minimum Push field bit rate for the MI Bus. Values for MCLK could be 640kHz,1280kHz, 1920kHz, …, n • 640kHz. The value ‘n’ is the modulus for the MI Bus baud register. MCLK may be the output of the PLL circuit or it may be the EXTAL/2 input of the MCU. Refer to Clock Divider Chains.

16.8 SCI0/MI Bus registers

MI Bus operation is controlled by the same group of registers as is used for the SCI. However the functions of some of the bits are modified when in MI Bus mode. A description of the registers, as applicable to the MI Bus function, is given here.

In MI Bus mode, bits that have no meaning are reserved by Freescale, and are not described.

	Bit 7	6	5	4	3	2	1	Bit 0	
	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	High
RESET:	0	0	0	0	0	0	0	0	

SC0BDH — MI Bus Clock Rate Control Register **$00C0**

	Bit 7	6	5	4	3	2	1	Bit 0	
	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	Low
RESET:	0	0	0	0	0	1	0	0	

SC0BDL — MI Bus Clock Rate Control Register **$00C1**

real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

msCAN12 utilises an advanced buffer arrangement resulting in a predictable real-time behaviour and simplifies the application software.

17.3 External Pins

The msCAN12 uses 2 external pins, 1 input (RxCAN) and 1 output (TxCAN). The TxCAN output pin represents the logic level on the CAN: 0 is for a dominant state, and 1 is for a recessive state.

RxCAN is on bit 0 of Port CAN, TxCAN is on bit 1. The remaining six pins of Port CAN (112TQFP version only) are controlled by registers in the msCAN12 address space (see msCAN12 Port CAN Control Register (PCTLCAN) and msCAN12 Port CAN Data Direction Register (DDRCAN)).

A typical CAN system with msCAN12 is shown in Figure 17-1.

Each CAN station is connected physically to the CAN bus lines through a transceiver chip. The transceiver is capable of driving the large current needed for the CAN and has current protection, against defective CAN or defective stations.

exited, the ATD module powers up and continues operation. The module is not reset; the register file is not reinitialized; the conversion sequence is not restarted.

When the module comes out of wait, it is recommended that a stabilization delay (t_{SR}) is allowed before new conversions are started.

DJM — Result Register Data Justification Mode

0 = Left justified mode

1 = Right justified mode

For 10-bit resolution, left justified mode maps a result register into data bus bits 6 through 15; bit 15 is the MSB. In right justified mode, the result registers maps onto data bus bits 0 through 9; bit 9 is the MSB.

For 8-bit resolution, left justified mode maps a result into the high byte (bits 8 though 15; bit 15 is the MSB). Right justified maps a result into the low byte (bits 0 through 7; bit 7 is the MSB).

Table 18-1 summarizes the result data formats available and how they are set up using the control bits.

Table 18-2 illustrates left justified output codes for an input signal range between 0 and 5.1 Volts.

RES10	DJM	Result Data Formats Description and Bus Bit Mapping
0	0	8-bit/left justified - bits 8-15
0	1	8-bit/right justified - bits 0-7
1	0	10-bit/left justified - bits 6-15
1	1	10-bit/right justified - bits 0-9

Table 18-1. Result Data Formats Available

Table 20-4. Supply Current

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Frequency of Operation (E-clock)			Unit
		2 MHz[1]	4 MHz[1]	8 MHz	
Maximum total supply current					
RUN:					
Single-chip mode	I_{DD}	18	30	50	mA
Expanded mode		30	50	85	
WAIT: (All peripheral functions shut down)[2]					
Single-chip mode	W_{IDD}	4	6	8	mA
Expanded mode		5	9	12	
STOP:[2]					
Single-chip mode, no clocks					
–40 to +85	S_{IDD}	10	10	10	µA
+85 to +105		50	50	50	µA
+105 to +125		50	50	50	µA
Maximum power dissipation[3]					
Single-chip mode	P_D	**100**	**165**	275	mW
Expanded mode		**165**	**275**	467	

1. For information only. Supply current guaranteed at 8MHz only.
2. On the 80 QFP package option, unbonded pins must be made outputs or have pullups enabled.
3. Includes I_{DD} and I_{DDA}.

Table 20-5. ATD DC Electrical Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, **ATD Clock** = **2 MHz**, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Analog supply voltage	V_{DDA}	4.5	5.5	V
Analog supply current, normal operation[1]	I_{DDA}		1.0	mA
Reference voltage, low	V_{RL}	V_{SSA}	$V_{DDA}/2$	V
Reference voltage, high	V_{RH}	$V_{DDA}/2$	V_{DDA}	V
V_{REF} differential reference voltage	$V_{RH}–V_{RL}$	4.5	5.5	V
Input voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
Input current, off channel[3]	I_{OFF}		100	nA
Reference supply current	I_{REF}		250	µA
Input capacitanceNot Sampling	C_{INN}		10	pF
Sampling	C_{INS}		15	pF

1. For **each** ATD module.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10°C decrease from maximum temperature.

Section 22. Appendix: Changes from MC68HC912D60

22.1 Contents

22.2 Significant changes from the MC68HC912D60 (non-suffix device)

22.2.1 Flash

22.2.1.1 Flash Architecture

The flash arrays are made from a new non-volatile memory (NVM) technology. An external VFP is no longer used. Programming is now carried out on a whole row (64 bytes) at a time. Erasing is still a bulk erase of the entire array.

22.2.1.2 Flash Control Register

The Flash Control Register (FEECTL) is in the same location. However, the individual bit functions have changed significantly to support the new technology.

memory location — Each M68HC12 memory location holds one byte of data and has a unique address. To store information in a memory location, the CPU places the address of the location on the address bus, the data information on the data bus, and asserts the write signal. To read information from a memory location, the CPU places the address of the location on the address bus and asserts the read signal. In response to the read signal, the selected memory location places its data onto the data bus.

memory map — A pictorial representation of all memory locations in a computer system.

MI-Bus — See "Freescale interconnect bus".

microcontroller — Microcontroller unit (MCU). A complete computer system, including a CPU, memory, a clock oscillator, and input/output (I/O) on a single integrated circuit.

modulo counter — A counter that can be programmed to count to any number from zero to its maximum possible modulus.

most significant bit (MSB) — The leftmost digit of a binary number.

Freescale interconnect bus (MI-Bus) — The Freescale Interconnect Bus (MI Bus) is a serial communications protocol which supports distributed real-time control efficiently and with a high degree of noise immunity.

Freescale scalable CAN (msCAN) — The Scalable controller area network is a serial communications protocol that efficiently supports distributed real-time control with a very high level of data integrity.

msCAN — See "Scalable CAN".

MSI — See "multiple serial interface".

multiple serial interface — A module consisting of multiple independent serial I/O sub-systems, e.g. two SCI and one SPI.

multiplexer — A device that can select one of a number of inputs and pass the logic level of that input on to the output.

nibble — A set of four bits (half of a byte).

object code — The output from an assembler or compiler that is itself executable machine code, or is suitable for processing to produce executable machine code.

opcode — A binary code that instructs the CPU to perform an operation.

open-drain — An output that has no pullup transistor. An external pullup device can be connected to the power supply to provide the logic 1 output voltage.