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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, MI Bus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	68
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912d60ampve8

3.5.6 Mode Select (SMODN, MODA, and MODB)

The state of these pins during reset determine the MCU operating mode. After reset, MODA and MODB can be configured as instruction queue tracking signals IPIPE0 and IPIPE1. MODA and MODB have active pull-downs during reset.

The SMODN pin has an active pull-up when configured as input. This pin can be used as BKGD or $\overline{\text{TAGHI}}$ after reset.

3.5.7 Single-Wire Background Mode Pin (BKGD)

The BKGD pin receives and transmits serial background debugging commands. A special self-timing protocol is used. The BKGD pin has an active pull-up when configured as input; BKGD has no pull-up control. Refer to Development Support.

3.5.8 External Address and Data Buses (ADDR[15:0] and DATA[15:0])

External bus pins share function with general-purpose I/O ports A and B. In single-chip operating modes, the pins can be used for I/O; in expanded modes, the pins are used for the external buses.

In expanded wide mode, ports A and B are used for multiplexed 16-bit data and address buses. PA[7:0] correspond to ADDR[15:8]/DATA[15:8]; PB[7:0] correspond to ADDR[7:0]/DATA[7:0].

In expanded narrow mode, ports A and B are used for the16-bit address bus, and an 8-bit data bus is multiplexed with the most significant half of the address bus on port A. In this mode, 16-bit data is handled as two back-to-back bus cycles, one for the high byte followed by one for the low byte. PA[7:0] correspond to ADDR[15:8] and to DATA[15:8] or DATA[7:0], depending on the bus cycle. The state of the address pin should be latched at the rising edge of E. To allow for maximum address setup time at external devices, a transparent latch should be used.

Setting the RDPT bit in the TMSK2 register configures all port T outputs to have reduced drive levels. Levels are at normal drive capability after reset. The TMSK2 register can be read or written anytime after reset Refer to Enhanced Capture Timer.

Table 3-3. MC68HC912D60A Port Description Summary

Port Name	Pin Numbers		Data Direction Register (Address)	Description
	80-pin	112-pin		
Port A PA[7:0]	48–41	64–57	In/Out DDRA ($0002)	Port A and port B pins are used for address and data in expanded modes. The port data registers are not in the address map during expanded and peripheral mode operation. When in the map, port A and port B can be read or written any time. DDRA and DDRB are not in the address map in expanded or peripheral modes.
Port B PB[7:0]	23–16	31–24	In/Out DDRB ($0003)	
Port AD1 PAD1[7:0]	N/A	84/82/80/78/76/74/72/70	In	Analog-to-digital converter 1 and general-purpose I/O.
Port AD0 PAD0[7:0]	60–53	83/81/79/77/75/73/71/69	In	Analog-to-digital converter 0 and general-purpose I/O.
Port CAN PCAN[7:0]	72, 73(1)	98–105	In/Out	General purpose I/O. PCAN[1:0] are used with the MSCAN12 module and cannot be used as I/O.
Port E PE[7:0]	25–28, 37–40	36–39, 53–56	PE[1:0] In PE[7:2] In/Out DDRE ($0009)	Mode selection, bus control signals and interrupt service request signals; or general-purpose I/O.
Port P PP[7:0]	76–80, 1–3	108–112, 1–3	In/Out DDRP ($0057)	General-purpose I/O. PP[3:0] are used with the pulse-width modulator when enabled.
Port S PS[7:0]	70–63	96–89	In/Out DDRS ($00D7)	Serial communications interfaces 1 and 0 and serial peripheral interface subsystems and general-purpose I/O.
Port T PT[7:0]	14–11, 7–4	18–15, 7–4	In/Out DDRT ($00AF)	General-purpose I/O when not enabled for input capture and output compare in the timer and pulse accumulator subsystem.

1. In 80-pin QFP package only TxCAN and RxCAN are available. PortCAN[2:7] pins should either be defined as outputs or have their pull-ups enabled.

	BIT 7	6	5	4	3	2	1	BIT 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	—	—	—	—	—	—	—	—
Alt. Pin Function	$\overline{\text{DBE}}$ or $\overline{\text{ECLK}}$ or CAL	MODB or IPIPE1 or CGMTST	MODA or IPIPE0	ECLK	$\overline{\text{LSTRB}}$ or BDTAGL or $\overline{\text{TAGLO}}$	R/$\overline{\text{W}}$	$\overline{\text{IRQ}}$	$\overline{\text{XIRQ}}$

PORTE — Port E Register **$0008**

This register is associated with external bus control signals and interrupt inputs, including data bus enable ($\overline{\text{DBE}}$), mode select (MODB/IPIPE1, MODA/IPIPE0), ECLK, size ($\overline{\text{LSTRB}}$), read/write (R/$\overline{\text{W}}$), $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$. When the associated pin is not used for one of these specific functions, the pin can be used as general-purpose I/O. The port E assignment register (PEAR) selects the function of each pin. DDRE determines the primary direction of each port E pin when configured to be general-purpose I/O.

Some of these pins have software selectable pull-ups ($\overline{\text{DBE}}$, $\overline{\text{LSTRB}}$, R/$\overline{\text{W}}$, $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$). A single control bit enables the pull-ups for all these pins which are configured as inputs.

This register is not in the map in peripheral mode or expanded modes when the EME bit is set.

Read and write anytime.

	Bit 7	6	5	4	3	2	1	Bit 0
	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	0	0
RESET:	0	0	0	0	0	0	0	0

DDRE — Port E Data Direction Register **$0009**

This register determines the primary direction for each port E pin configured as general-purpose I/O.

Use this step-by-step procedure to program a row of Flash memory.

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Write to any aligned word Flash address within the row address range desired (with any data) to select the row.
3. Wait for a time, t_{NVS} (min. 10μs).
4. Set the HVEN bit.
5. Wait for a time, t_{PGS} (min. 5μs).
6. Write one data word (two bytes) to the next aligned word Flash address to be programmed. If BOOTP is asserted, an attempt to program an address in the boot block will be ignored.
7. Wait for a time, t_{FPGM} (min. 30μs – max. 40μs).
8. Repeat steps 6 and 7 until all the words within the row are programmed.
9. Clear the PGM bit.
10. Wait for a time, t_{NVH} (min. 5μs).
11. Clear the HVEN bit.
12. After time, t_{RCV} (min 1μs), the memory can be accessed in read mode again.

This program sequence is repeated throughout the memory until all data is programmed. For minimum overall programming time and least program disturb effect, the sequence should be part of an intelligent operation which iterates per row.

9.6.2 External Reset

The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic one in less than eight ECLK cycles after an internal device releases reset. When a reset condition is sensed, the $\overline{\text{RESET}}$ pin is driven low by an internal device for about 16 ECLK cycles, then released. Eight ECLK cycles later it is sampled. If the pin is still held low, the CPU assumes that an external reset has occurred. If the pin is high, it indicates that the reset was initiated internally by either the COP system or the clock monitor.

To prevent a COP or clock monitor reset from being detected during an external reset, hold the reset pin low for at least 32 cycles. An external RC power-up delay circuit on the reset pin is not recommended as circuit charge time can cause the MCU to misinterpret the type of reset that has occurred.

9.6.3 COP Reset

The MCU includes a computer operating properly (COP) system to help protect against software failures. When COP is enabled, software must write $55 and $AA (in this order) to the COPRST register in order to keep a watchdog timer from timing out. Other instructions may be executed between these writes. A write of any value other than $55 or $AA or software failing to execute the sequence properly causes a COP reset to occur. In addition, windowed COP operation can be selected. In this mode, a write to the COPRST register must occur in the last 25% of the selected period. A premature write will also reset the part.

9.6.4 Clock Monitor Reset

If clock frequency falls below a predetermined limit when the clock monitor is enabled, a reset occurs.

Section 10. I/O Ports with Key Wake-up

10.1 Contents

10.2 Introduction

The 112QFP MC68HC912D60A offers 16 additional I/O port pins with key wake-up capability on 15 of them (KWG7 is used for I^2C start detect). Only two (KWG4 and KWH4) are available on the 80QFP package. All Port G and Port H pins should either be defined as outputs or have their pull-ups/downs enabled.

The key wake-up feature of the MC68HC912D60A issues an interrupt that will wake up the CPU when it is in the STOP or WAIT mode. Two ports are associated with the key wake-up function: port G and port H. Port G and port H wake-ups are triggered with a falling signal edge. For each pin which has an interrupt enabled, there is a path to the interrupt request signal which has no clocked devices when the part is in stop mode. This allows an active edge to bring the part out of stop.

Digital filtering is included to prevent pulses shorter than a specified value from waking the part from STOP.

An interrupt is generated when a bit in the KWIFG or KWIFH register and its corresponding KWIEG or KWIEH bit are both set. All 15 bits/pins share the same interrupt vector. Key wake-ups can be used with the pins configured as inputs or outputs.

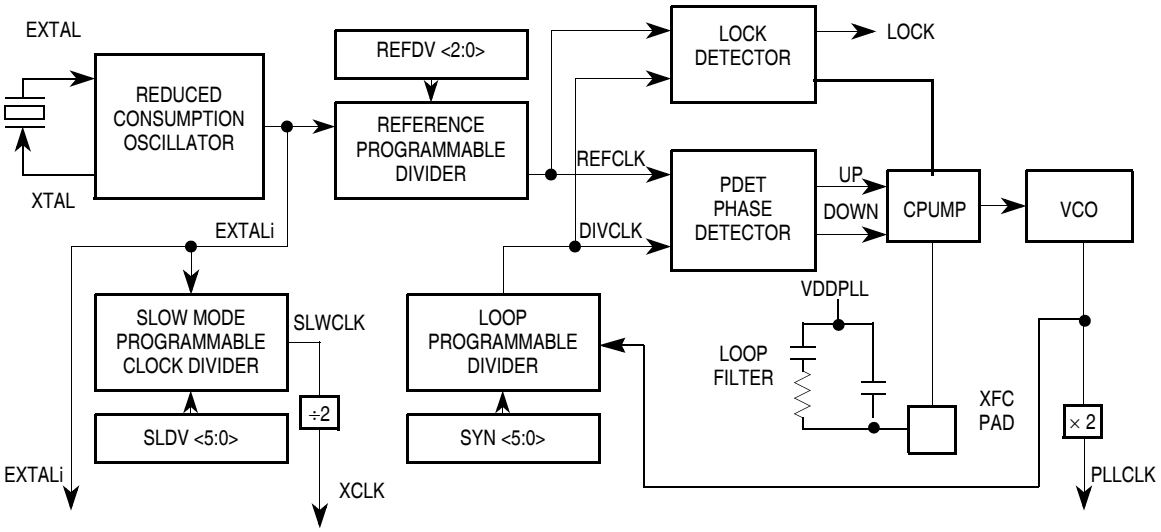

Figure 11-2. PLL Functional Diagram

The PLL may be used to run the MCU from a different time base than the incoming crystal value. It creates an integer multiple of a reference frequency. For increased flexibility, the crystal clock can be divided by values in a range of 1 – 8 (in unit steps) to generate the reference frequency. The PLL can multiply this reference clock in a range of 1 to 64. Although it is possible to set the divider to command a very high clock frequency, do not exceed the specified bus frequency limit for the MCU.

If the PLL is selected, it will continue to run when in WAIT mode resulting in more power consumption than normal. To take full advantage of the reduced power consumption of WAIT mode, turn off the PLL before going into WAIT. Please note that in this case the PLL stabilization time applies.

The PLL operation is suspended in STOP mode. After STOP exit followed by the stabilization time, it resumes operation at the same frequency, provided the AUTO bit is set.

A passive external loop filter must be placed on the control line (XFC pad). The filter is a second-order, low-pass filter to eliminate the VCO input ripple. Values of components in the diagram are dependent upon the desired VCO operation. See XFC description.

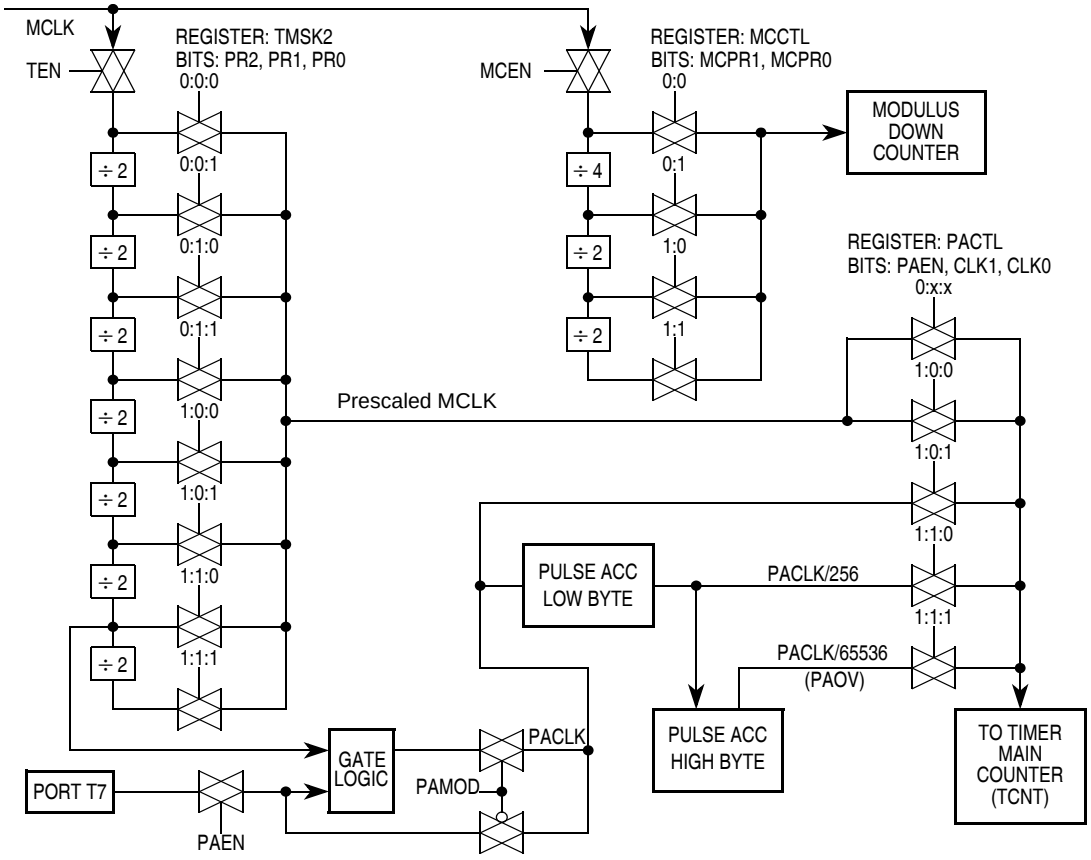

Figure 11-8. Clock Chain for ECT

Section 15. Multiple Serial Interface

15.1 Contents

15.2 Introduction

The multiple serial interface (MSI) module consists of three independent serial I/O sub-systems: two serial communication interfaces (SCI0 and SCI1) and the serial peripheral interface (SPI). Each serial pin shares function with the general-purpose port pins of port S. The SCI subsystems are NRZ type systems that are compatible with standard RS-232 systems. These SCI systems have a new single wire operation mode which allows the unused pin to be available as general-purpose I/O. The SPI subsystem, which is compatible with the M68HC11 SPI, includes new features such as $\overline{SS}$ output and bidirectional mode.

15.4.3 SCI Register Descriptions

Control and data registers for the SCI subsystem are described below. The memory address indicated for each register is the default address that is in use after reset. Both SCI have identical control registers mapped in two blocks of eight bytes.

	Bit 7	6	5	4	3	2	1	Bit 0	
	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	High
RESET:	0	0	0	0	0	0	0	0	

SC0BDH/SC1BDH — SCI Baud Rate Control Register **$00C0/$00C8**

	Bit 7	6	5	4	3	2	1	Bit 0	
	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	Low
RESET:	0	0	0	0	0	1	0	0	

SC0BDL/SC1BDL — SCI Baud Rate Control Register **$00C1/$00C9**

SCxBDH and SCxBDL are considered together as a 16-bit baud rate control register.

Read any time. Write SBR[12:0] anytime. Low order byte must be written for change to take effect. Write SBR[15:13] only in special modes. The value in SBR[12:0] determines the baud rate of the SCI. The desired baud rate is determined by the following formula:

$$\text{SCI Baud Rate} = \frac{\text{MCLK}}{16 \times \text{BR}}$$

which is equivalent to:

$$\text{BR} = \frac{\text{MCLK}}{16 \times \text{SCI Baud Rate}}$$

BR is the value written to bits SBR[12:0] to establish baud rate.

NOTE: *The baud rate generator is disabled until TE or RE bit in SCxCR2 register is set for the first time after reset, and/or the baud rate generator is disabled when SBR[12:0] = 0.*

17.13.12 msCAN12 Transmit Error Counter (CTXERR)

		Bit 7	6	5	4	3	2	1	Bit 0
CTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
$010F	W								
RESET		0	0	0	0	0	0	0	0

This register reflects the status of the msCAN12 transmit error counter. The register is read only.

NOTE: *Both error counters must only be read when in SLEEP or SOFT_RESET mode.*

17.13.13 msCAN12 Identifier Acceptance Registers (CIDAR0–7)

On reception each message is written into the background receive buffer. The CPU is only signalled to read the message however, if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the msCAN12 are applied on the IDR0 to IDR3 registers of incoming messages in a bit by bit manner.

For extended identifiers all four acceptance and mask registers are applied. For standard identifiers only the first two (CIDMR0/1 and CIDAR0/1) are applied.

AM7 – AM0 — Acceptance Mask Bits

If a particular bit in this register is cleared this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit, before a match is detected. The messageis accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted.

Bit description:

0 = Match corresponding acceptance code register and identifier bits.

1 = Ignore corresponding acceptance code register bit.

NOTE: *The CIDMR0–7 registers can only be written if the SFTRES bit in CMCR0 is set.*

17.13.15 msCAN12 Port CAN Control Register (PCTLCAN)

		Bit 7	6	5	4	3	2	1	Bit 0
PCTLCAN	R	0	0	0	0	0	0	PUPCAN	RDPCAN
$013D	W								
RESET		0	0	0	0	0	0	0	0

The following bits control pins 7 through 2 of Port CAN. Pins 1 and 0 are reserved for the RxCan (input only) and TxCan (output only) pins.

PUPCAN — Pull-Up Enable Port CAN

0 = Pull mode disabled for Port CAN.

1 = Pull mode enabled for Port CAN.

In 80QFP all PortCAN[2:7] pins should either be defined as outputs or have their pull-ups enabled.

RDPCAN — Reduced Drive Port CAN

0 = Reduced drive disabled for Port CAN.

1 = Reduced drive enabled for Port CAN.

Section 18. Analog-to-Digital Converter

18.1 Contents

18.2 Introduction

The 112TQFP version of the MC68HC912D60A has two identical ATD modules identified as ATD0 and ATD1. Except for the V_{DDA} and V_{SSA} Analog supply voltage, all pins are duplicated and indexed with ‘0’ or ‘1’ in the following description. An ‘x’ indicates either ‘0’ or ‘1’.

The 80QFP version has only one ATD available, ATD0. ATD1 is not bonded out. As this module defaults to disabled on reset and it's I/O are inputs by default it requires no configuration.

The ATD module is an 8-channel, 10-bit or 8-bit, multiplexed-input, successive-approximation analog-to-digital converter. It does not require external sample and hold circuits because of the type of charge redistribution technique used. The ATD converter timing can be synchronized to the system PCLK. The ATD module consists of a 16-word (32-byte) memory-mapped control register block used for control, testing and configuration.

can be performed. Note that powering up the module does not reset the module since the register file is not initialized.

In power down mode, the control and result registers are still accessible.

18.5.2 IDLE Mode

IDLE mode for the ATD module is defined as the state where the ATD module is powered up and ready to perform an A/D conversion, but not actually performing a conversion at the present time. Access to all control, status, and result registers is available. The module is consuming near maximum power.

NOTE: *When not active, the sample-and-hold and analog-to-digital sub-modules disable the clocks at their inputs to conserve power. The analog electronics still draw quiescent current.*

18.5.3 RUN Mode

RUN mode for the ATD module is defined as the state where the ATD module is powered up and currently performing an A/D conversion. Complete assess to all control, status and result registers is available. The module is consuming maximum power.

18.6 ATD Operation In Different MCU Modes

18.6.1 STOP Mode

Asserting Stop causes the ATD module to power down. The digital clocks are disabled and the analog quiescent current draw is turned off; this places the module into its power down state and is equivalent to clearing the ADPU control bit in ATDCTL2.

Table 18-8 lists the special channels. The last column in the table denote the expected digital code that should be generated by the special conversion for 8-bit resolution.

CC, CB, CA — Analog Input Channel Select Code

These bits select the analog input channel(s). Table 18-9 lists the coding used to select the various analog input channels. In the case of single channel scans (MULT=0), this selection code specifies the channel for conversion. In the case of multi-channel scans (MULT=1), this selection code represents the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing the channel selection code; selection codes that reach the maximum value wrap around to the minimum value.

Note that for special conversion mode, bits CC/CB/CA have a different function. Instead of specifying the analog input channel, they identify which special channel conversion is to take place. (See Table 18-8.) A summart of the channels converted and the associated result locations for multiple channel scans can be found in Table 18-10.

Table 18-9. Analog Input Channel Select Coding

CC	CB	CA	Analog Input Channel
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	AD6
1	1	1	AD7

the result is available in result register ADR0; CCF1 is set when the second conversion in a sequence is complete and the result is available in ADR1, and so forth.

The conversion complete flags are cleared depending on the setting of the fast flag clear bit (AFFC in ATDCTL2). When AFFC=0, the status register containing the conversion complete flag must be read as a precondition before the flag can be cleared. The flag is actually cleared during a subsequent access to the result register. This provides a convenient method for clearing the conversion complete flag when the user is polling the ATD module; it ensures the user is signaled as to the availability of new data and avoids having to have the user clear the flag explicitly.

When AFFC=1, the conversion complete flags are cleared when their associated result registers are read; reading the status register is not a necessary condition in order to clear them. This is the easiest method for clearing the conversion complete flags which is useful when the ATD module signals conversion completion with an interrupt.

The conversion complete flags are normally read only; in special (test) mode they can be written.

NOTE: *When ATDCTL4/5 register is written, the SCF flags and all CCFx flags are cleared; any pending interrupt request is canceled.*

BKMBL — Breakpoint Mask Low

Disables the matching of the low byte of data when in full breakpoint mode. Used in conjunction with the BKDBE bit (which should be set)

0 = Low byte of data bus (bits 7:0) are compared to BRKDL

1 = Low byte is not used in comparisons.

BK1RWE — R/$\overline{W}$ Compare Enable

Enables the comparison of the R/$\overline{W}$ signal to further specify what causes a match. This bit is NOT useful in program breakpoints or in full breakpoint mode. This bit is used in conjunction with a second address in dual address mode when BKDBE=1.

0 = R/W is not used in comparisons

1 = R/W is used in comparisons

BK1RW — R/$\overline{W}$ Compare Value

When BK1RWE = 1, this bit determines the type of bus cycle to match.

0 = A write cycle will be matched

1 = A read cycle will be matched

BK0RWE — R/$\overline{W}$ Compare Enable

Enables the comparison of the R/$\overline{W}$ signal to further specify what causes a match. This bit is not useful in program breakpoints.

0 = R/$\overline{W}$ is not used in the comparisons

1 = R/$\overline{W}$ is used in comparisons

BK0RW — R/$\overline{W}$ Compare Value

When BK0RWE = 1, this bit determines the type of bus cycle to match on.

0 = Write cycle will be matched

1 = Read cycle will be matched

Table 20-10. Flash EEPROM Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Units
Bytes per row	—	64	64	Bytes
Read bus clock frequency	f_{READ}	32K	8M	Hz
Erase time	t_{ERAS}	8	8	ms
PGM/ERAS to HVEN set up time	t_{NVS}	10	—	µs
High voltage hold time	t_{NVL}	5	—	µs
High voltage hold time (erase)	t_{NVHL}	100	—	µs
Program hold time	t_{PGS}	5	—	µs
Program time	t_{FPGM}	30	40	µs
Return to read time	t_{RCV}	1	—	µs
Cumulative program hv period	t_{HV}	—	8	ms
Row program/erase endurance	—	100		cycles
Data retention	—	10(1)		years

1. Based on the average life time operating temperature of 70°C.

Table 20-11. Pulse Width Modulator Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
ECLK frequency	f_{eclk}	0.004	8.0	MHz
A-clock frequency Selectable	f_{aclk}	$f_{eclk}/128$	f_{eclk}	Hz
BCLK frequency Selectable	f_{bclk}	$f_{eclk}/128$	f_{eclk}	Hz
Left-aligned PWM frequency 8-bit 16-bit	f_{lpwm}	 $f_{eclk}/1M$ $f_{eclk}/256M$	 $f_{eclk}/2$ $f_{eclk}/2$	 Hz Hz
Left-aligned PWM resolution	r_{lpwm}	$f_{eclk}/4K$	f_{eclk}	Hz
Center-aligned PWM frequency 8-bit 16-bit	f_{cpwm}	 $f_{eclk}/2M$ $f_{eclk}/512M$	 f_{eclk} f_{eclk}	 Hz Hz
Center-aligned PWM resolution	r_{cpwm}	$f_{eclk}/4K$	f_{eclk}	Hz

Table 20-14. Multiplexed Expansion Bus Timing

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Num	Characteristic[1], [2], [3], [4]	Delay	Symbol	8 MHz		Unit
				Min	Max	
	Frequency of operation (ECLK frequency)		f_o	0.004	8.0	MHz
1	Cycle time $t_{cyc} = 1/f_o$	—	t_{cyc}	0.125	250	µs
2	Pulse width, E low $PW_{EL} = t_{cyc}/2 + \text{delay}$	–4	PW_{EL}	58		ns
3	Pulse width, E high[5] $PW_{EH} = t_{cyc}/2 + \text{delay}$	–2	PW_{EH}	60		ns
5	Address delay time $t_{AD} = t_{cyc}/4 + \text{delay}$	27	t_{AD}		50	ns
7	Address valid time to ECLK rise $t_{AV} = PW_{EL} - t_{AD}$	—	t_{AV}	8		ns
8	Multiplexed address hold time $t_{MAH} = t_{cyc}/4 + \text{delay}$	–18	t_{MAH}	13		ns
9	Address Hold to Data Valid	—	t_{AHDS}	20		ns
10	Data Hold to High Z $t_{DHZ} = t_{AD} - 20$	—	t_{DHZ}		30	ns
11	Read data setup time	—	t_{DSR}	25		ns
12	Read data hold time	—	t_{DHR}	0		ns
13	Write data delay time	—	t_{DDW}		47	ns
14	Write data hold time	—	t_{DHW}	20		ns
15	Write data setup time[5] $t_{DSW} = PW_{EH} - t_{DDW}$	—	t_{DSW}	13		ns
16	Read/write delay time $t_{RWD} = t_{cyc}/4 + \text{delay}$	18	t_{RWD}		49	ns
17	Read/write valid time to E rise $t_{RWV} = PW_{EL} - t_{RWD}$	—	t_{RWV}	9		ns
18	Read/write hold time	—	t_{RWH}	20		ns
19	Low strobe[6] delay time $t_{LSD} = t_{cyc}/4 + \text{delay}$	18	t_{LSD}		49	ns
20	Low strobe[6] valid time to E rise $t_{LSV} = PW_{EL} - t_{LSD}$	—	t_{LSV}	9		ns
21	Low strobe[6] hold time	—	t_{LSH}	20		ns
22	Address access time[5] $t_{ACCA} = t_{cyc} - t_{AD} - t_{DSR}$	—	t_{ACCA}		50	ns
23	Access time from E rise[5] $t_{ACCE} = PW_{EH} - t_{DSR}$	—	t_{ACCE}		35	ns
24	$\overline{DBE}$ delay from ECLK rise[5] $t_{DBED} = t_{cyc}/4 + \text{delay}$	8	t_{DBED}		39	ns
25	$\overline{DBE}$ valid time $t_{DBE} = PW_{EH} - t_{DBED}$	—	t_{DBE}	21		ns
26	$\overline{DBE}$ hold time from ECLK fall		t_{DBEH}	0	10	ns

1. All timings are calculated for normal port drives.
2. Crystal input is required to be within 45% to 55% duty.
3. Reduced drive must be off to meet these timings.
4. Unequalled loading of pins will affect relative timing numbers.
5. This characteristic is affected by clock stretch.
   Add $N \times t_{cyc}$ where N = 0, 1, 2, or 3, depending on the number of clock stretches.
6. Without TAG enabled.

The filter components values are chosen from standard series (e.g. E12 for resistors). The operating voltage is assumed to be 5V (although there is only a minor difference between 3V and 5V operation). The smoothing capacitor Cp in parallel with R and C is set to be 1/10 of the value of C. The reference frequencies mentioned in this table correspond to the output of the fine granularity divider controlled by the REFDV register. This means that the calculations are irrespective of the way the reference frequency is generated (directly for the crystal oscillator or after division). The target frequency value also has an influence on the calculations of the filter components because the VCO gain is NOT constant over its operating range.

The bandwidth limit corresponds to the so-called Gardner's criteria. It corresponds to the maximum value that can be chosen before the continuous time approximation ceases to be justified. It is of course advisable to stay far away from this limit.