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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, MI Bus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	68
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912d60avpve8

Table 1-2. Development Tools Ordering Information

Description	Name	Order Number
MCUez		Free from World Wide Web
Serial Debug Interface	SDI	M68SDIL (3–5V), M68DIL12 (SDIL + MCUez + SDBUG12)
Evaluation board	EVB	M68EVB912D60 (EVB only) M68KIT912D60 (EVB + SDIL12)

NOTE: *SDBUG12 is a P & E Micro Product. It can be obtained from P & E from their web site (http://www.pemicro.com) for approximately $100.*

Third party tools: http://www.mcu.motsps.com/dev_tools/3rd/index.html

RDWE — Read/Write Enable

Normal: write once; Special: write anytime EXCEPT the first time. Read anytime. This bit has no effect in single-chip modes.

0 = PE2 is a general-purpose I/O pin.

1 = PE2 is configured as the R/$\overline{W}$ pin. In single chip modes, RDWE has no effect and PE2 is a general-purpose I/O pin.

R/$\overline{W}$ is used for external writes. After reset in normal expanded mode, it is disabled. If needed it should be enabled before any external writes.

CALE — Calibration Reference Enable

Read and write anytime.

0 = Calibration reference is disabled and PE7 is general-purpose I/O in single chip or peripheral modes or if the NDBE bit is set.

1 = Calibration reference is enabled on PE7 in single chip and peripheral modes or if the NDBE bit is set.

DBENE — $\overline{DBE}$ or Inverted E Clock on Port E[7]

Normal modes: write once. Special modes: write anytime EXCEPT the first; read anytime.

DBENE controls which signal is output on PE7 when NDBE control bit is cleared. The inverted ECLK output can be used to latch the address for demultiplexing. It has the same behaviour as the ECLK, except it is inverted. Please note that in the case of idle expansion bus, the ‘not ECLK’ signal could stay high for many cycles.

The DBNE bit has no effect in single chip or peripheral modes and PE7 is defaulted to the CAL function if the CALE bit is set in the PEAR register or to an I/O otherwise.

0 = PE7 pin used for $\overline{DBE}$ external control of data enable on memories in expanded modes when NDBE = 0

1 = PE7 pin used for inverted ECLK output in expanded modes when NDBE = 0

7.11 Flash protection bit FPOPEN

The FPOPEN bit is located in EEMCR – EEPROM Module Configuration Register, bit 4.

FPOPEN – Opens the Flash array for program or erase

0 = The whole Flash array (32-Kbyte and 28-Kbyte) is protected.

1 = The whole Flash array (32-Kbyte and 28-Kbyte) is enabled for program or erase

FPOPEN can be read at anytime.

FPOPEN can be written only to ’0’ for protection but not to ’1’ for un-protect in normal mode.

FPOPEN can be written ’0’ and ’1’ in special mode only.

FPOPEN is loaded at reset from EEPROM SHADOW word bit 4.

When FPOPEN is cleared to ’0’, the Flash array cannot be reprogrammed in normal modes.

CAUTION: *Programming the NVM FPOPEN bit in the SHADOW word ($_FC0, bit 4) means that the FPOPEN bit in the EEMCR register will always be ’0’ in normal modes. The flash array can no longer be modified in normal modes.*

Section 10. I/O Ports with Key Wake-up

10.1 Contents

10.2 Introduction

The 112QFP MC68HC912D60A offers 16 additional I/O port pins with key wake-up capability on 15 of them (KWG7 is used for I^2C start detect). Only two (KWG4 and KWH4) are available on the 80QFP package. All Port G and Port H pins should either be defined as outputs or have their pull-ups/downs enabled.

The key wake-up feature of the MC68HC912D60A issues an interrupt that will wake up the CPU when it is in the STOP or WAIT mode. Two ports are associated with the key wake-up function: port G and port H. Port G and port H wake-ups are triggered with a falling signal edge. For each pin which has an interrupt enabled, there is a path to the interrupt request signal which has no clocked devices when the part is in stop mode. This allows an active edge to bring the part out of stop.

Digital filtering is included to prevent pulses shorter than a specified value from waking the part from STOP.

An interrupt is generated when a bit in the KWIFG or KWIFH register and its corresponding KWIEG or KWIEH bit are both set. All 15 bits/pins share the same interrupt vector. Key wake-ups can be used with the pins configured as inputs or outputs.

	Bit 7	6	5	4	3	2	1	Bit 0
	0	KWIFG6	KWIFG5	KWIFG4	KWIFG3	KWIFG2	KWIFG1	KWIFG0
RESET:	0	0	0	0	0	0	0	0

KWIFG — Key Wake-up Port G Flag Register **$002E**

Each flag, except bit 6, is set by a falling edge on its associated input pin. To clear the flag, write one to the corresponding bit in KWIFG.

Read and write anytime

Bit 7 always reads zero.

KWIFG6 — Key Wake-up Port G Flag 6

0 = Falling edge on the associated bit or I2C Start condition has not occurred

1 = Falling edge on the associated bit or I2C Start condition has occurred (an interrupt will occur if the associated enable bit is set)

Depending on WI2CE bit in KWIEG register, KWIFG6 flags either falling edge or I2C Start condition.

KWIFG[5:0] — Key Wake-up Port G Flags

0 = Falling edge on the associated bit has not occurred

1 = Falling edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).

Therefore, if the MCU is powered up without an external clock, limp-home mode is entered provided the MCU is in a normal mode of operation.

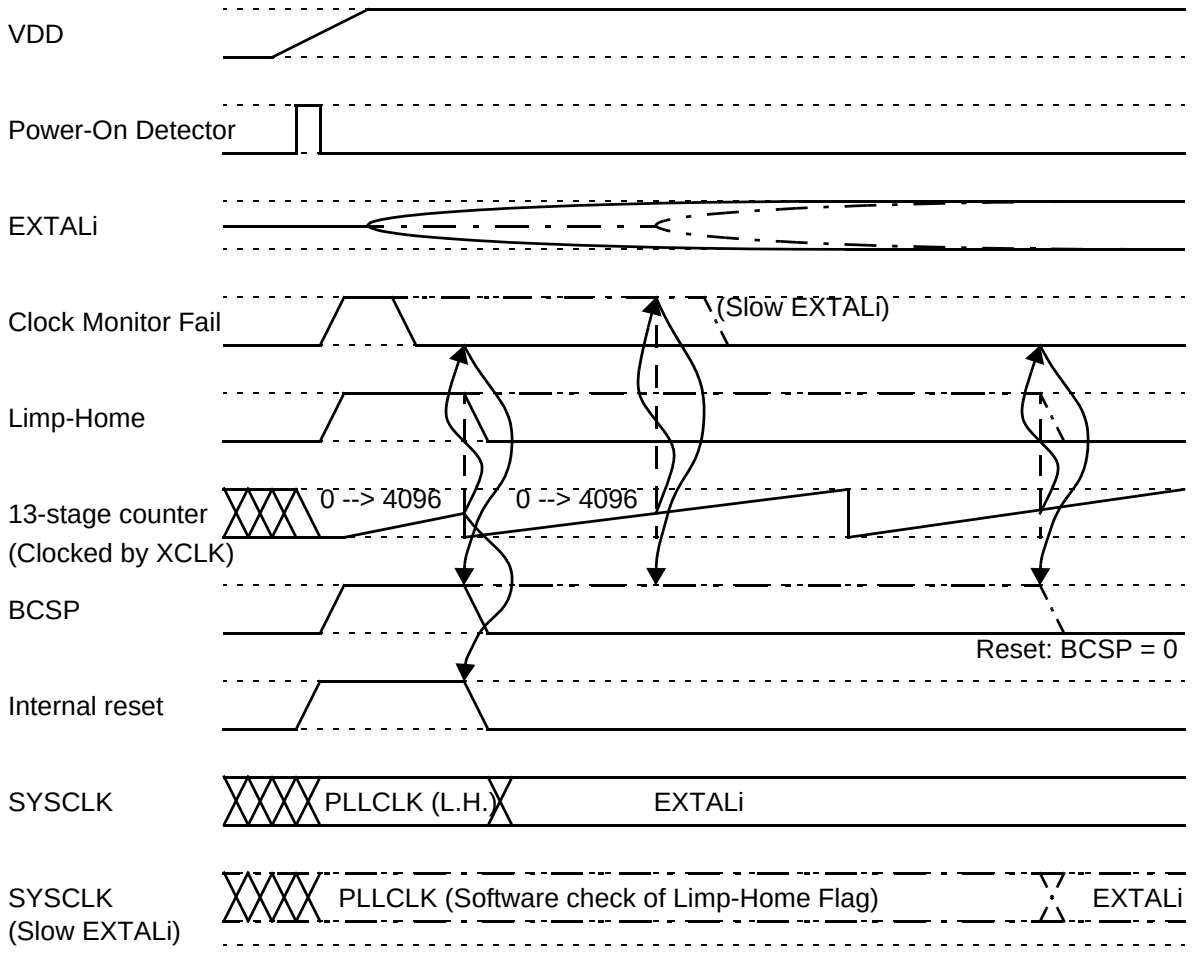

Figure 11-4. No Clock at Power-On Reset

- **Minimize XTAL and EXTAL routing lengths** to reduce EMC issues.

NOTE: *EXTAL and XTAL routing resistances are less important than capacitances. Using minimum width traces is an acceptable trade-off to reduce capacitance.*

12.5 MC68HC912D60P Pierce Oscillator Specification

This section applies to the 3L02H mask set, which refers to the newest set of CGM improvements (to the MC68HC912D60A) with the Pierce oscillator configuration enabled. The name for these devices is MC68HC912D60P.

12.5.1 MC68HC912D60P Oscillator Design Architecture

The Pierce oscillator architecture is shown in Figure 12-4. The component configuration for this oscillator is different to all previous MC68HC912D60A configurations and the recommended components may be different.

Please note carefully the connection of external capacitors and the resonator in this diagram.

Section 13. Pulse Width Modulator

13.1 Contents

13.2 Introduction

The pulse-width modulator (PWM) subsystem provides four independent 8-bit PWM waveforms or two 16-bit PWM waveforms or a combination of one 16-bit and two 8-bit PWM waveforms. Each waveform channel has a programmable period and a programmable duty-cycle as well as a dedicated counter. A flexible clock select scheme allows four different clock sources to be used with the counters. Each of the modulators can create independent, continuous waveforms with software-selectable duty rates from 0 percent to 100 percent. The PWM outputs can be programmed as left-aligned outputs or center-aligned outputs.

The period and duty registers are double buffered so that if they change while the channel is enabled, the change will not take effect until the counter rolls over or the channel is disabled. If the channel is not enabled, then writes to the period and/or duty register will go directly to the latches as well as the buffer, thus ensuring that the PWM output will always be either the old waveform or the new waveform, not some variation in between.

A change in duty or period can be forced into immediate effect by writing the new value to the duty and/or period registers and then writing to the counter. This causes the counter to reset and the new duty and/or period values to be latched. In addition, since the counter is readable it is

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
RESET:	0	0	0	0	0	0	0	0

CFORC — Timer Compare Force Register **$0081**

Read anytime but will always return $00 (1 state is transient). Write anytime.

FOC[7:0] — Force Output Compare Action for Channel 7-0

A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “n” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCn register except the interrupt flag does not get set.

	Bit 7	6	5	4	3	2	1	Bit 0
	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
RESET:	0	0	0	0	0	0	0	0

OC7M — Output Compare 7 Mask Register **$0082**

Read or write anytime.

The bits of OC7M correspond bit-for-bit with the bits of timer port (PORTT). Setting the OC7Mn will set the corresponding port to be an output port regardless of the state of the DDRTn bit when the corresponding IOSn bit is set to be an output compare. This does not change the state of the DDRT bits. At successful OC7, for each bit that is set in OC7M, the corresponding data bit OC7D is stored to the corresponding bit of the timer port.

NOTE: *OC7M has priority over output action on the timer port enabled by OMn and OLn bits in TCTL1 and TCTL2. If an OC7M bit is set, it prevents the action of corresponding OM and OL bits on the selected timer port.*

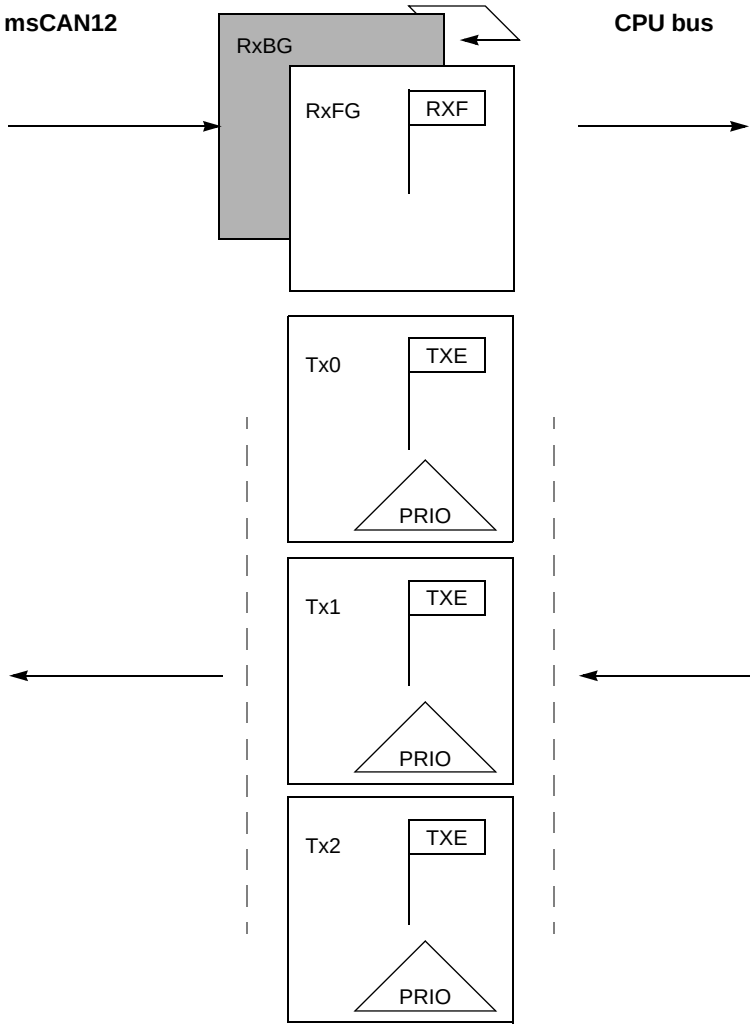

Figure 17-2. User Model for Message Buffer Organization

When the msCAN12 module is transmitting, the msCAN12 receives its own messages into the background receive buffer, RxBG, but does NOT overwrite RxFG, generate a receive interrupt or acknowledge its own messages on the CAN bus. The exception to this rule is in loop-back mode (see msCAN12 Module Control Register 1 (CMCR1).) where the msCAN12 treats its own messages exactly like all other incoming messages. The msCAN12 receives its own transmitted messages in the event that it loses arbitration. If arbitration is lost, the msCAN12 must be prepared to become receiver.

cause of the receiver interrupt. When more than one hit occurs (two or more filters match) the lower hit has priority.

A very flexible programmable generic identifier acceptance filter has been introduced in order to reduce the CPU interrupt loading. The filter is programmable to operate in four different modes:

- Two identifier acceptance filters, each to be applied to a) the full 29 bits of the extended identifier and to the following bits of the CAN frame: RTR, IDE, SRR or b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. This mode implements two filters for a full length CAN 2.0B compliant extended identifier. Figure 17-3 shows how the first 32-bit filter bank (CIDAR0–3, CIDMR0–3) produces a filter 0 hit. Similarly, the second filter bank (CIDAR4–7, CIDMR4–7) produces a filter 1 hit.
- Four identifier acceptance filters, each to be applied to a) the 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages or b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B mesages. Figure 17-4 shows how the first 32-bit filter bank (CIDAR0–3, CIDMR0–3) produces filter 0 and 1 hits. Similarly, the second filter bank (CIDAR4–7, CIDMR4–7) produces filter 2 and 3 hits.
- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or of a CAN 2.0B compliant extended identifier. Figure 17-5 shows how the first 32-bit filter bank (CIDAR0–3, CIDMR0–3) produces filter 0 to 3 hits. Similarly, the second filter bank (CIDAR4–7, CIDMR4–7) produces filter 4 to 7 hits.
- Closed filter. No CAN message will be copied into the foreground buffer RxFG, and the RXF flag will never be set.

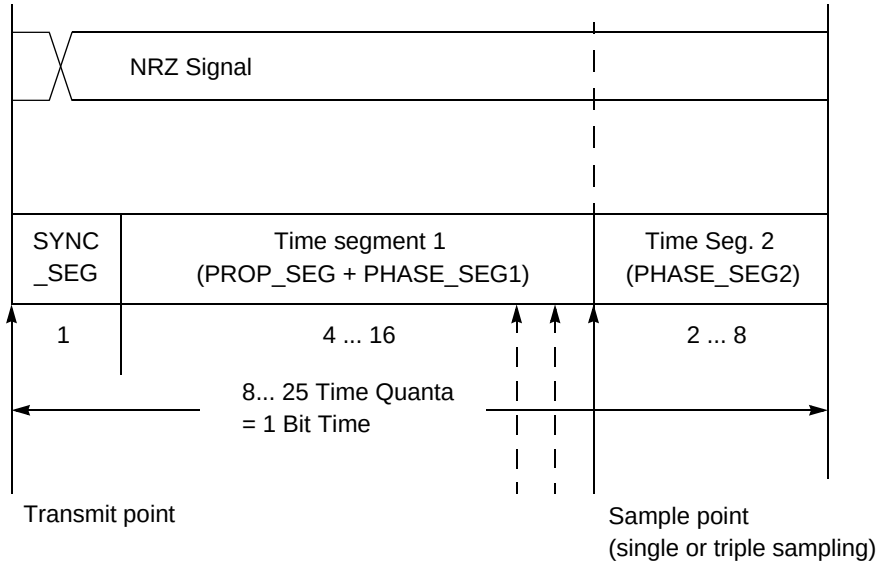

Figure 17-8. Segments within the Bit Time

Table 17-3. CAN Standard Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchron. Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

TXEIE2 – TXEIE0 — Transmitter Empty Interrupt Enable

0 = No interrupt will be generated from this event.

1 = A transmitter empty (transmit buffer available for transmission) event will result in a transmitter empty interrupt.

NOTE: *The CTCR register is held in the reset state when the SFTRES bit in CMCR0 is set.*

17.13.10 msCAN12 Identifier Acceptance Control Register (CIDAC)

		Bit 7	6	5	4	3	2	1	Bit 0
CIDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
$0108	W								
RESET		0	0	0	0	0	0	0	0

IDAM1 – IDAM0 — Identifier Acceptance Mode

The CPU sets these flags to define the identifier acceptance filter organisation (see Identifier Acceptance Filter). Table 17-8 summarizes the different settings. In Filter Closed mode no messages are accepted such that the foreground buffer is never reloaded.

Table 17-9. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32 bit Acceptance Filters
0	1	Four 16 bit Acceptance Filters
1	0	Eight 8 bit Acceptance Filters
1	1	Filter Closed

17.13.12 msCAN12 Transmit Error Counter (CTXERR)

		Bit 7	6	5	4	3	2	1	Bit 0
CTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
$010F	W								
RESET		0	0	0	0	0	0	0	0

This register reflects the status of the msCAN12 transmit error counter. The register is read only.

NOTE: *Both error counters must only be read when in SLEEP or SOFT_RESET mode.*

17.13.13 msCAN12 Identifier Acceptance Registers (CIDAR0–7)

On reception each message is written into the background receive buffer. The CPU is only signalled to read the message however, if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the msCAN12 are applied on the IDR0 to IDR3 registers of incoming messages in a bit by bit manner.

For extended identifiers all four acceptance and mask registers are applied. For standard identifiers only the first two (CIDMR0/1 and CIDAR0/1) are applied.

- WAIT is executed (if the ASWAI bit is activated)
- STOP is executed.

The MCU can discover when result data is available in the result registers with an interrupt on sequence complete or by polling the conversion complete flags

- The SCF bit is set after the completion of each sequence.
- The CCF bit associated with each result register is set when that register is loaded with result data.

NOTE: ***ATD conversion modes*** *should not be confused with* ***MCU operating modes*** *such as STOP, WAIT, IDLE, RUN, DEBUG, and SPECIAL (test) modes or with* ***module defined operating modes*** *such as power down, fast flag clear, 8-bit resolution, 10-bit resolution, interrupt enable, clock prescaler setting, and freeze modes; and finally do not confuse with* ***module result data formats*** *such as right justify mode and left justify mode.*

18.4 Functional Description

18.4.1 Analog Input Multiplexer

The analog input multiplexer selects one of the 8 external analog input channels to generate an analog sample. The input analog signals are unipolar and must fall within the potential range of VSSA to VDDA (analog electronics supply potentials).

18.4.2 Sample Buffer Amplifier

A sample amplifier is used to buffer the input analog signal so that a storage node can be quickly charged to the sample potential.

18.9.1 ATD Control Registers 0 &1 (ATDCTL0, ATDCTL1)

ATD0CTL0/ATD1CTL0 — Reserved **$0060/$01E0**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	0	0	0	0	0	0	0	0

Writes to this register will abort current conversion sequence.
Read or write any time.

ATD0CTL1/ATD1CTL1 — Reserved **$0061/$01E1**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	0	0	0	0	0	0	0	0

WRITE: Write to this register has no meaning.
READ: Special Mode only.

18.9.2 ATD Control Registers 2 & 3 (ATDCTL2, ATDCTL3)

The ATD control registers 2 & 3 are used to select the power up mode, fast flag clear mode, wait mode, 16 channel mode, interrupt control, and freeze control. Writes to these registers will not abort the current conversion sequence nor start a new sequence.

ATD0CTL2/ATD1CTL2 — ATD Control Register 2 **$0062/$01E2**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	AFFC	ASWAI	DJM	Reserved	Reserved	ASCIE	ASCIF
RESET:	0	0	0	0	0	0	0	0

READ: any time
WRITE: any time
(except for Bit 0 – ASCIF, READ: any time, WRITE: not allowed)

ADPU — ATD Disable / Power Down
0 = Disable and power down the ATD
1 = Normal ATD functionality

$\overline{\text{TAGHI}}$ signal shares a pin with the BKGD signal. Tagging information is latched on the falling edge of ECLK.

Table 19-12 shows the functions of the two tagging pins. The pins operate independently - the state of one pin does not affect the function of the other. The presence of logic level zero on either pin at the fall of ECLK performs the indicated function. Tagging is allowed in all modes. Tagging is disabled when BDM becomes active and BDM serial commands are not processed while tagging is active.

Table 19-12. Tag Pin Function

TAGHI	TAGLO	Tag
1	1	no tag
1	0	low byte
0	1	high byte
0	0	both bytes

The tag follows program information as it advances through the queue. When a tagged instruction reaches the head of the queue, the CPU enters active background debugging mode rather than execute the instruction.

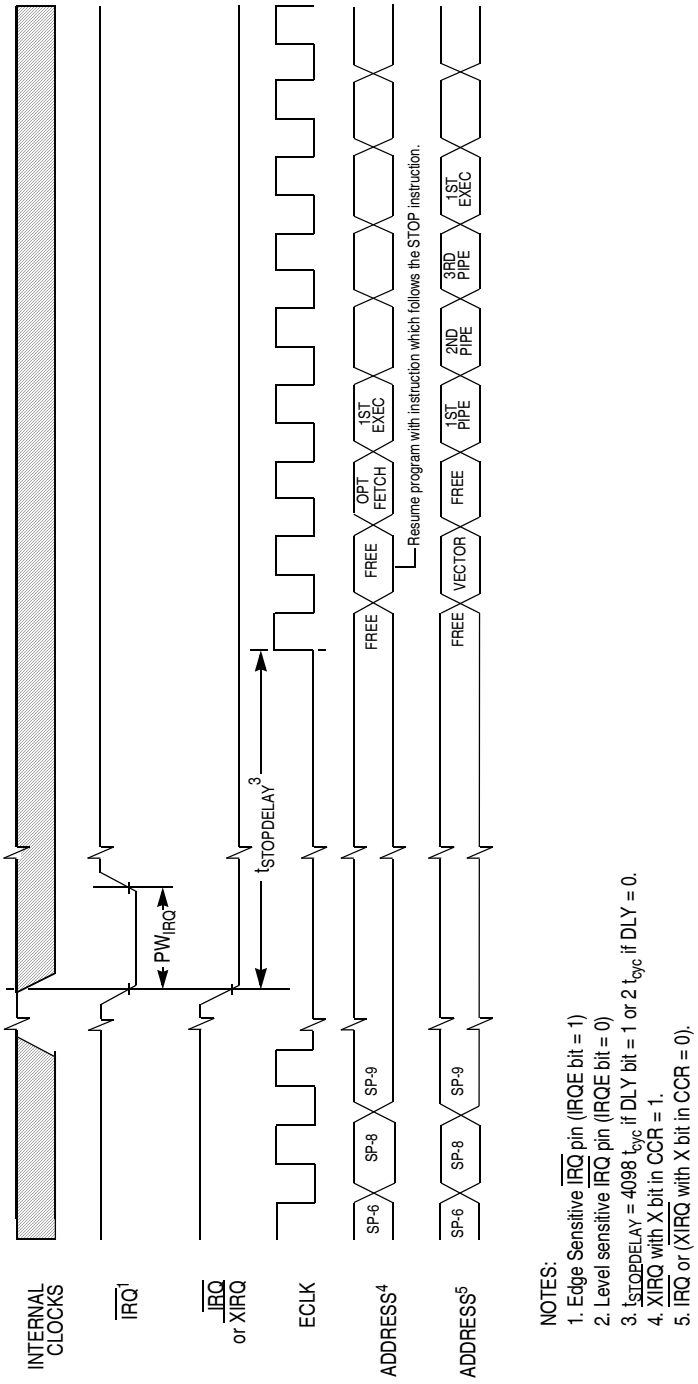

Figure 20-3. STOP Recovery Timing Diagram

spectrum. This is especially the case for the power supply pins close to the E port, when the ECLK and/or the calibration clock are used.

- On the general VDD power supply input, a ‘T’ low pass filter LCL can be used (e.g. 10μH-47μF-10μH). The ‘T’ is preferable to the ‘Π’ version as the exhibited impedance is more constant with respect to the VDD current. Like many modular micro controllers, HC12 devices have a power consumption which not only varies with clock edges but also with the functioning modes.
- Keep high speed clock and bus trace length to a minimum. The higher the clock speed, the shorter the trace length. If noisy signals are sent over long tracks, impedance adjustments should be considered at both ends of the line (generally, simple resistors suffice).
- Bus drivers like the CAN physical interface should be installed close to their connector, with dedicated filtering on their power supply.
- Mount components as close to the board as possible. Snip excess lead length as close to the board as possible. Preferably use Surface Mount Devices (SMDs).
- Mount discrete components as close to the chip that uses them as possible.
- Do not cross sensitive signals ON ANY LAYER. If a sensitive signal must be crossed by another signal, do it as many layers away as possible and at right angles.
- Always keep PCBs clean. Solder flux, oils from fingerprints, humidity and general dirt can conduct electricity. Sensitive circuits can easily be disrupted by small amounts of leakage.
- Choose PCB coatings with care. Certain epoxies, paints, gelatins, plastics and waxes can conduct electricity. If the manufacturer cannot provide the electrical characteristics of the substance, do not use it.

Appendix: Information on MC68HC912D60A Mask