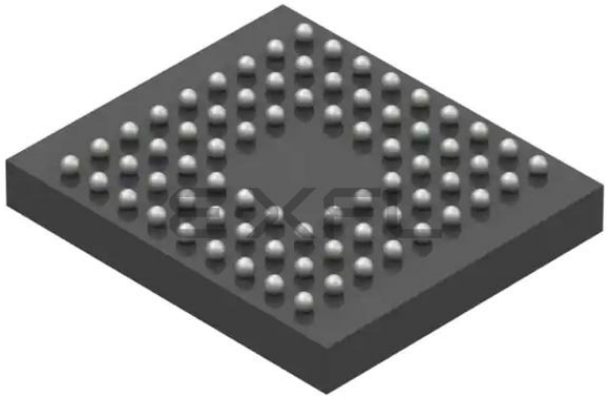

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	57
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	72-UFBGA, WLCSP
Supplier Device Package	72-WLCSP (4.41x3.76)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476jgy6ptr

3.4 Embedded Flash memory

STM32L476xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

Table 13. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.31 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.32 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

3.36 Quad SPI memory interface (QUADSPI)

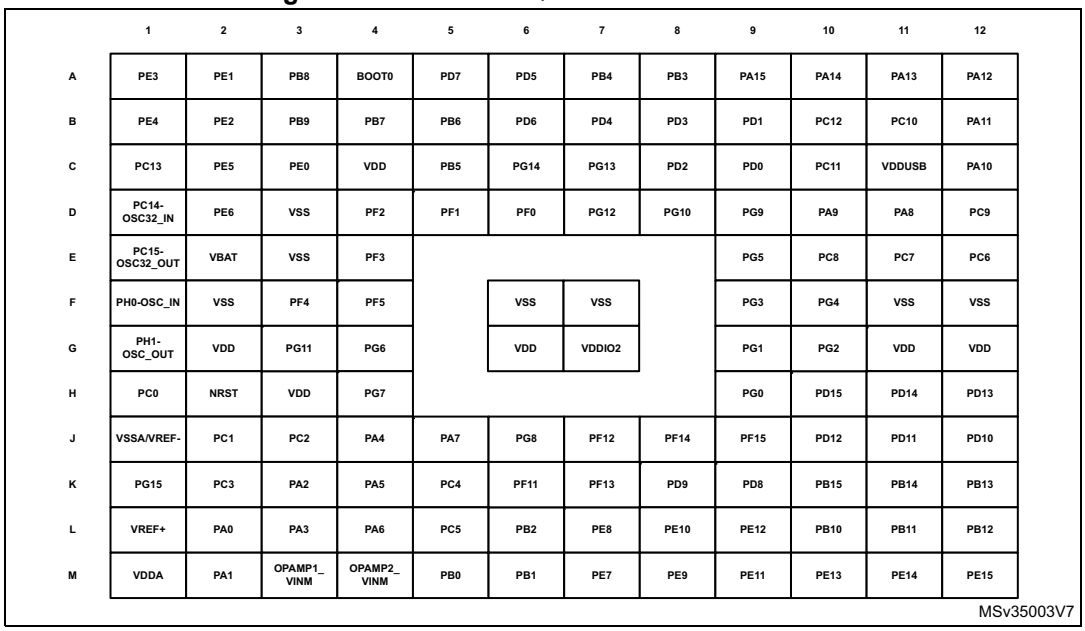
The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external flash is memory mapped and is seen by the system as if it were an internal memory

The Quad SPI interface supports:

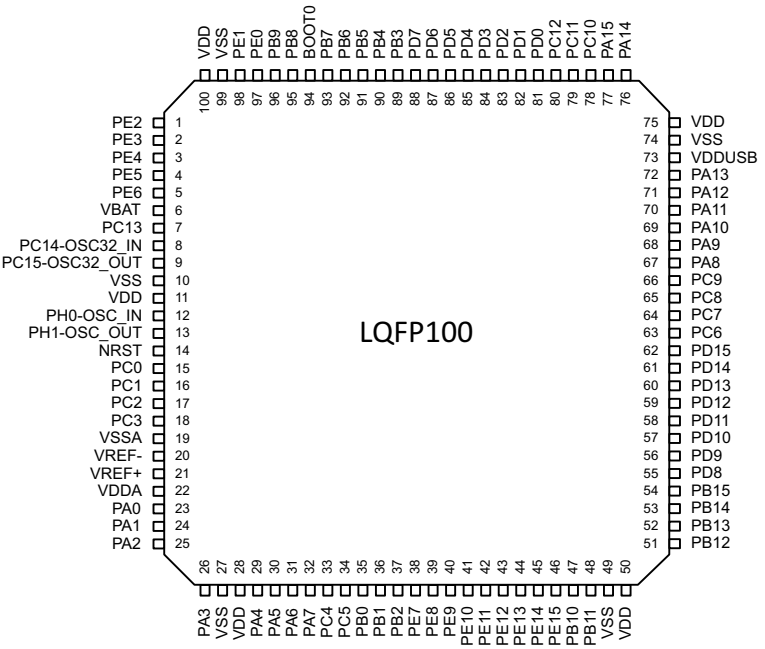
- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

Figure 5. STM32L476Qx UFBGA132 ballout(1)



1. The above figure shows the package top view.

Figure 6. STM32L476Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	45	M11	67	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	-	-	46	M12	68	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-
29	H3	H3	47	L10	69	PB10	I/O	FT_fl	-	TIM2_CH3, I2C2_SCL, SPI2_SCK, DFSDM_DATIN7, USART3_TX, LPUART1_RX, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	G3	G3	48	L11	70	PB11	I/O	FT_fl	-	TIM2_CH4, I2C2_SDA, DFSDM_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
31	J2	J2	49	F12	71	VSS	S	-	-	-	-
32	J1	J1	50	G12	72	VDD	S	-	-	-	-
33	H1	H1	51	L12	73	PB12	I/O	FT_l	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-

Table 18. STM32L476xx memory map and peripheral register boundary addresses (1)

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI
	0xA000 0000 - 0xA000 0FFF	4 KB	FMC
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5004 0400 - 0x5006 07FF	129 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.15	3.19	3.31	3.50	3.85	3.47	3.70	3.84	4.26	4.88	mA
				16 MHz	2.24	2.28	2.39	2.57	2.90	2.46	2.60	2.74	3.16	3.78	
				8 MHz	1.26	1.29	1.40	1.57	1.89	1.40	1.50	1.64	2.06	2.68	
				4 MHz	0.71	0.75	0.85	1.02	1.34	0.79	0.88	1.06	1.38	2.21	
				2 MHz	0.42	0.45	0.55	0.72	1.04	0.46	0.55	0.73	1.09	1.88	
				1 MHz	0.27	0.30	0.40	0.57	0.89	0.30	0.38	0.57	0.90	1.61	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.22	0.40	0.74	1.44	
			Range 1	80 MHz	10.0	10.1	10.3	10.6	11.0	11.00	11.35	11.64	12.26	13.10	
				72 MHz	9.06	9.13	9.28	9.51	9.92	9.97	10.36	10.65	11.06	11.69	
				64 MHz	8.96	9.04	9.22	9.48	9.92	9.86	10.25	10.54	10.95	11.79	
				48 MHz	7.64	7.72	7.91	8.17	8.62	8.40	8.76	8.90	9.52	10.36	
				32 MHz	5.49	5.57	5.74	5.98	6.40	6.04	6.40	6.69	7.10	7.94	
				24 MHz	4.16	4.22	4.36	4.57	4.96	4.60	4.86	5.15	5.56	6.19	
				16 MHz	2.93	2.99	3.13	3.35	3.75	3.22	3.43	3.72	4.13	4.97	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	358	392	503	683	1050	435	501	694	1069	1819	µA
				1 MHz	197	230	340	519	880	245	312	512	887	1637	
				400 kHz	97	126	235	414	778	130	202	402	777	1527	
				100 kHz	47	77	186	365	726	85	147	347	711	1472	

1. Guaranteed by characterization results, unless otherwise specified.

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 41* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 41. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		6	9.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	5.6	10.9	µs
			Wakeup clock HSI16 = 16 MHz	4.7	10.4	
		Range 2	Wakeup clock MSI = 24 MHz	5.7	11.1	
			Wakeup clock HSI16 = 16 MHz	4.5	10.5	
			Wakeup clock MSI = 4 MHz	6.6	14.2	
	Wake up time from Stop 0 mode to Low-power run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	0.7	2.05	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
		Range 2	Wakeup clock MSI = 24 MHz	0.8	2.72	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
			Wakeup clock MSI = 4 MHz	2.4	11.32	

Table 50. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 66. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 85. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{sf(IN)}$;$t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2	3.5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time		6.5	-	-	
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Data output valid time	Voltage Range 1	-	11	12	
		Voltage Range 2		15	19	
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Data output hold time	Voltage Range 1	6	-	-	
		Voltage Range 2	8	-		

1. Guaranteed by characterization results.

Figure 31. Quad SPI timing diagram - SDR mode

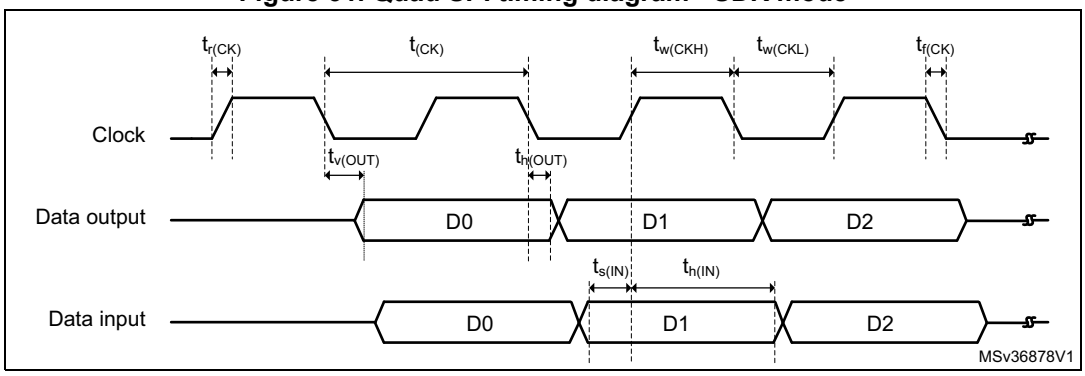


Figure 32. Quad SPI timing diagram - DDR mode

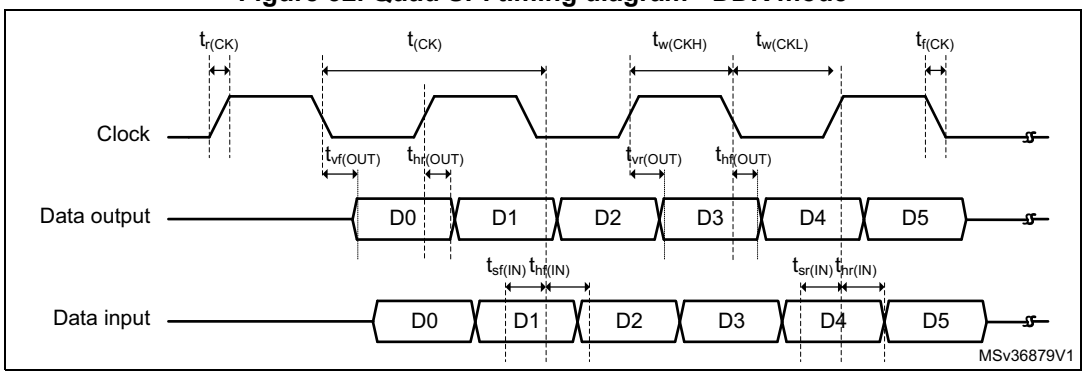


Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-1	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	T_{HCLK}-0.5	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+0.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}$-0.5	$7T_{HCLK}$+0.5	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-0.5	$5T_{HCLK}$+0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}-0.5	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 43. Synchronous non-multiplexed NOR/PSRAM read timings

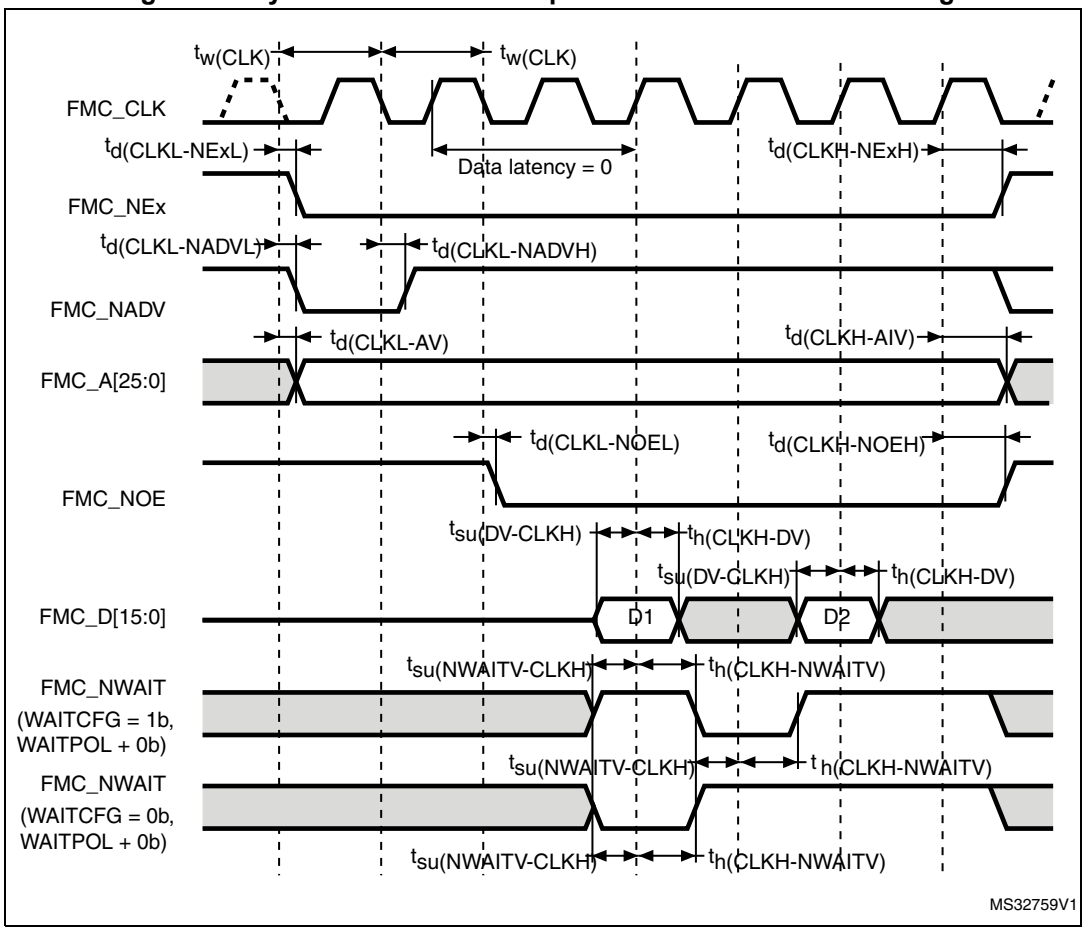
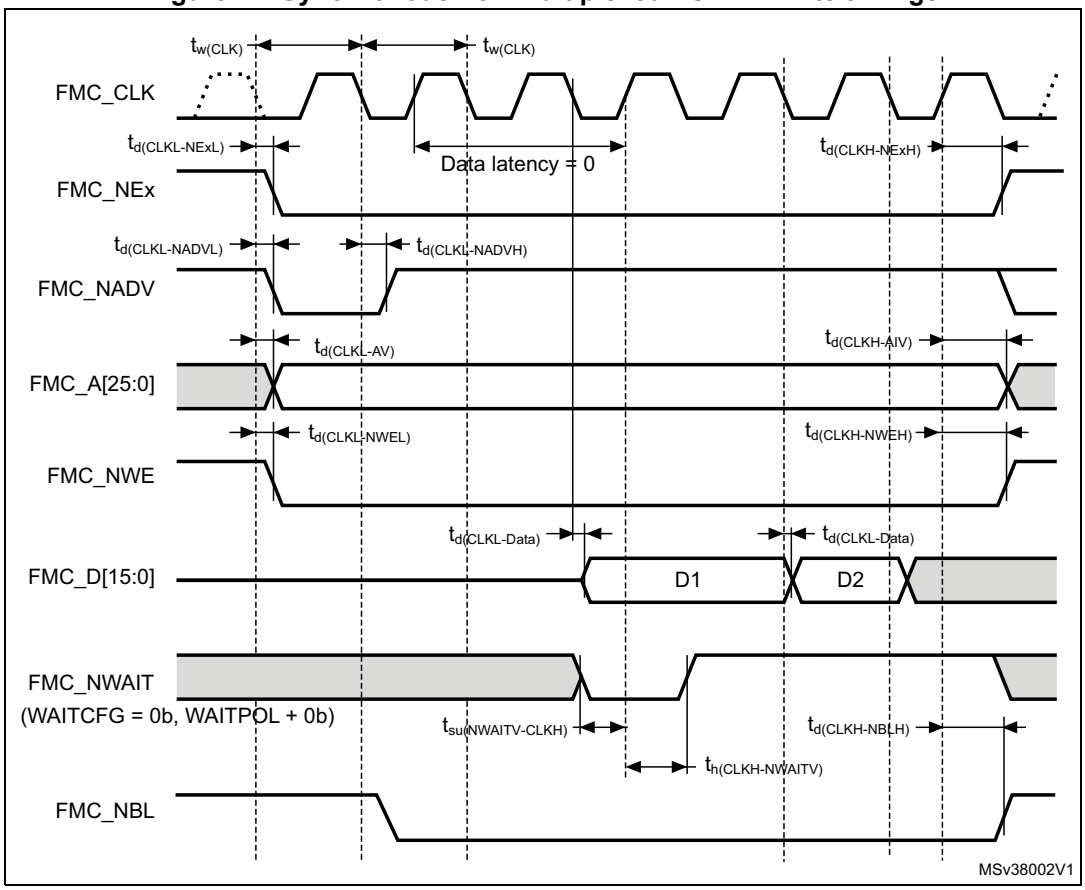


Table 100. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}-0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}-0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

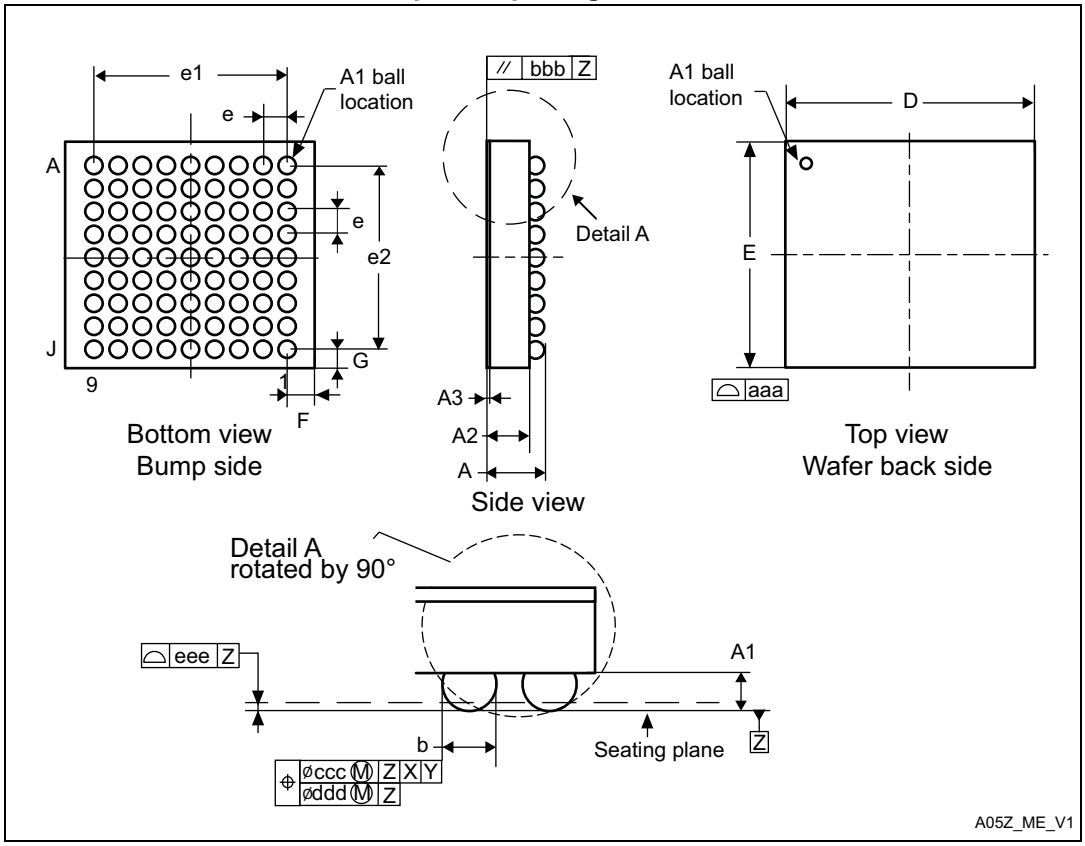
1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 44. Synchronous non-multiplexed PSRAM write timings



7.4 WLCSP81 package information

Figure 58. WLCSP81 - 81-ball, 4.4084 x 3.7594 mm, 0.4 mm pitch wafer level chip scale package outline



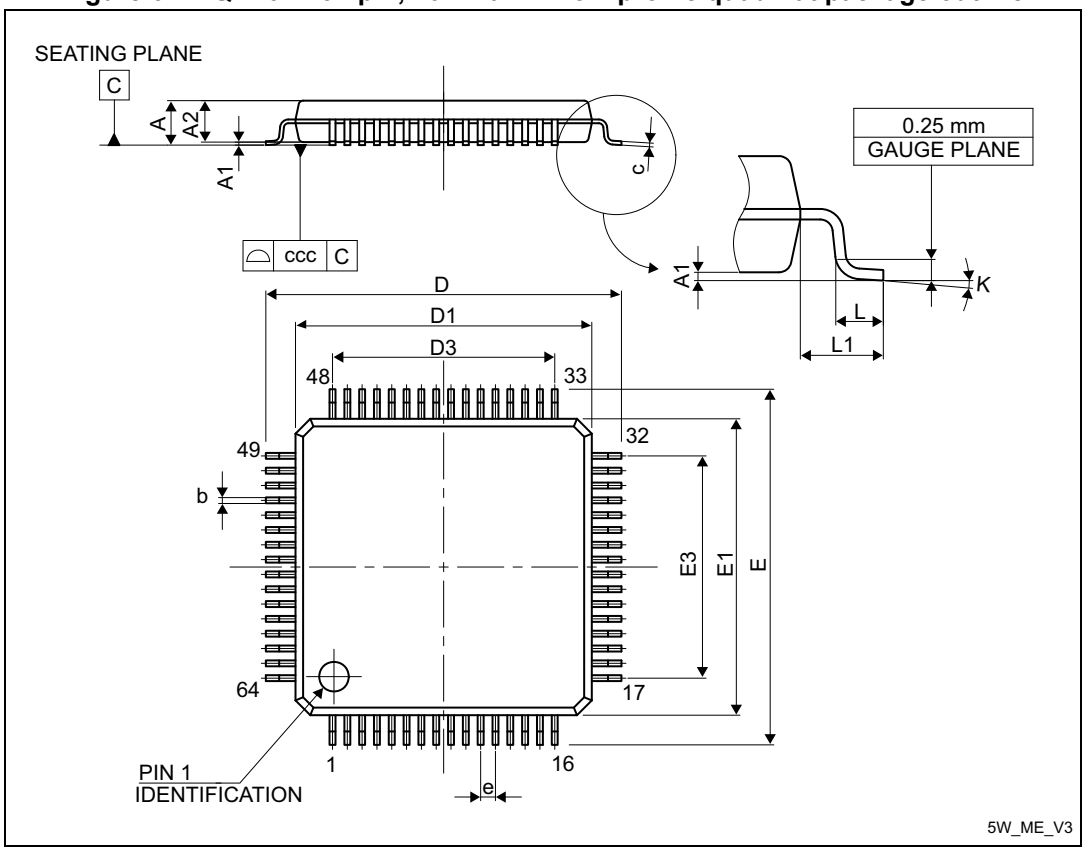
1. Drawing is not to scale.

Table 108. WLCSP81- 81-ball, 4.4084 x 3.7594 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.3734	4.4084	4.4434	0.1722	0.1736	0.1749
E	3.7244	3.7594	3.7944	0.1466	0.1480	0.1494
e	-	0.400	-	-	0.0157	-
e1	-	3.200	-	-	0.1260	-
e2	-	3.200	-	-	0.1260	-

7.6 LQFP64 package information

Figure 64. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 112. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-