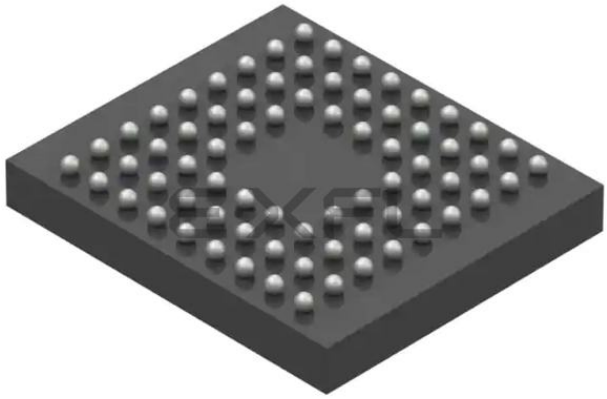

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	57
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	72-UFBGA, WLCSP
Supplier Device Package	72-WLCSP (4.41x3.76)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476jgy6vtr

3.25 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	20	-	31	VREF-	S	-	-	-	-
12	G9	G9	-	J1	-	VSSA/VREF-	-	-	-	-	-
-	G8	G8	21	L1	32	VREF+	S	-	-	-	VREFBUF_OUT
-	H9	H9	22	M1	33	VDDA	S	-	-	-	-
13	-	-	-	-	-	VDDA/VREF+	S	-	-	-	-
14	H8	H8	23	L2	34	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, RTC_TAMP2/WKUP1
-	-	-	-	M3	-	OPAMP1_VINM	I	TT	-	-	-
15	G4	G4	24	M2	35	PA1	I/O	FT_la	-	TIM2_CH2, TIM5_CH2, USART2_RTS_DE, UART4_RX, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6
16	G6	G6	25	K3	36	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LCD_SEG1, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO
17	H7	H7	26	L3	37	PA3	I/O	TT	-	TIM2_CH4, TIM5_CH4, USART2_RX, LCD_SEG2, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC12_IN8
18	J9	J9	27	E3	38	VSS	S	-	-	-	-
19	J8	J8	28	H3	39	VDD	S	-	-	-	-
20	G5	G5	29	J4	40	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_IN9, DAC1_OUT1
21	H6	H6	30	K4	41	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC12_IN10, DAC1_OUT2
22	H5	H5	31	L4	42	PA6	I/O	FT_la	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, USART3_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11

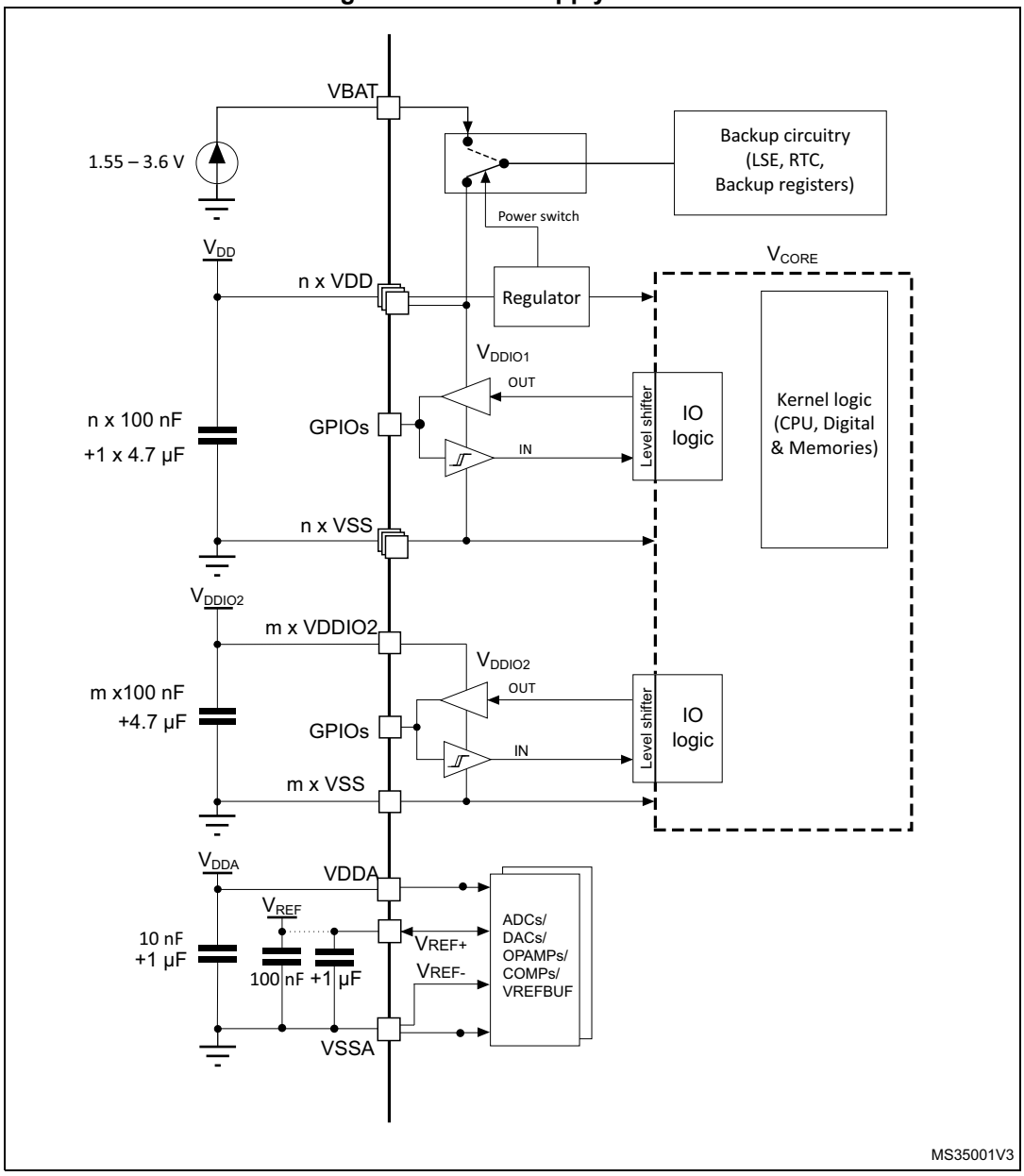
Table 18. STM32L476xx memory map and peripheral register boundary addresses (continued)[1]

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 1800 - 0x4000 23FF	3 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

6.1.6 Power supply scheme

Figure 13. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.93	3.05	3.23	3.58	3.20	3.37	3.51	3.93	4.76	mA
				16 MHz	1.83	1.87	1.98	2.16	2.49	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.98	1.02	1.12	1.29	1.62	1.10	1.17	1.31	1.73	2.56	
				4 MHz	0.55	0.59	0.69	0.85	1.18	0.61	0.70	0.89	1.24	1.95	
				2 MHz	0.34	0.37	0.47	0.64	0.96	0.37	0.46	0.64	0.98	1.71	
				1 MHz	0.23	0.26	0.36	0.53	0.85	0.27	0.33	0.50	0.86	1.57	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.21	0.38	0.74	1.44	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.8	12.1	12.5	13.3	
				72 MHz	9.24	9.31	9.47	9.69	10.1	10.16	10.7	11.0	11.4	12.2	
				64 MHz	8.25	8.32	8.46	8.68	9.09	9.08	9.6	9.9	10.3	11.1	
				48 MHz	6.28	6.35	6.5	6.72	7.11	6.91	7.3	7.6	8.0	8.8	
				32 MHz	4.24	4.30	4.44	4.65	5.04	4.66	4.97	5.26	5.67	6.51	
				24 MHz	3.21	3.27	3.4	3.61	3.98	3.53	3.76	4.05	4.46	5.30	
				16 MHz	2.19	2.24	2.36	2.56	2.94	2.41	2.66	2.95	3.16	3.99	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	272	303	413	592	958	330	393	579	954	1704	µA
				1 MHz	154	184	293	473	835	195	265	457	822	1572	
				400 kHz	78	108	217	396	758	110	180	380	755	1505	
				100 kHz	42	73	182	360	723	75	138	331	706	1456	

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.94	3.05	3.23	3.58	3.18	3.26	3.40	4.02	4.65	mA
				16 MHz	1.83	1.87	1.98	2.15	2.50	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.97	1.00	1.11	1.27	1.62	1.07	1.16	1.32	1.73	2.36	
				4 MHz	0.54	0.57	0.67	0.84	1.18	0.59	0.69	0.88	1.23	1.96	
				2 MHz	0.33	0.36	0.46	0.62	0.96	0.37	0.45	0.63	0.98	1.70	
				1 MHz	0.22	0.25	0.35	0.51	0.85	0.25	0.33	0.50	0.86	1.57	
				100 kHz	0.12	0.15	0.25	0.41	0.75	0.15	0.21	0.39	0.74	1.45	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.57	11.86	12.07	13.11	
				72 MHz	9.25	9.31	9.46	9.68	10.1	10.18	10.41	10.55	10.76	11.80	
				64 MHz	8.25	8.31	8.46	8.67	9.08	9.08	9.37	9.66	9.87	10.91	
				48 MHz	6.26	6.33	6.48	6.69	7.11	6.89	7.11	7.25	7.67	8.50	
				32 MHz	4.22	4.28	4.42	4.63	5.03	4.64	4.86	5.15	5.56	6.19	
				24 MHz	3.20	3.25	3.38	3.59	3.99	3.52	3.70	3.84	4.26	5.09	
				16 MHz	2.18	2.22	2.35	2.55	2.94	2.40	2.55	2.84	3.25	4.09	
I_{DD}(LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	242	275	384	562	924	300	380	573	927	1677	µA
				1 MHz	130	162	269	445	809	180	243	435	810	1560	
				400 kHz	61	90	197	374	734	95	160	353	728	1478	
				100 kHz	26	56	163	339	702	55	122	314	679	1429	

1. Guaranteed by characterization results, unless otherwise specified.

Table 35. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	6.59	24.7	92.7	208	437	16	62	232	520	1093	µA
				2.4 V	6.65	24.8	92.9	209	439	17	62	232	523	1098	
				3 V	6.65	24.9	93.3	210	442	17	62	233	525	1105	
				3.6 V	6.70	25.1	93.8	212	447	17	63	235	530	1118	
		-	LCD enabled(2) clocked by LSI	1.8 V	7.00	25.2	97.2	219	461	18	63	243	548	1153	
				2.4 V	7.14	25.4	97.5	220	463	18	64	244	550	1158	
				3 V	7.24	25.7	97.7	221	465	18	64	244	553	1163	
				3.6 V	7.36	26.1	98.7	223	471	18	65	247	558	1178	
I_{DD} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	LCD disabled	1.8 V	6.88	25.0	93.1	209	439	17	63	233	523	1098	µA
				2.4 V	7.02	25.2	93.7	210	441	18	63	234	525	1103	
				3 V	7.12	25.4	94.2	212	444	18	64	236	530	1110	
				3.6 V	7.25	25.7	95.2	214	449	18	64	238	535	1123	
			LCD enabled(2)	1.8 V	7.01	26.1	99.0	223	467	18	65	248	558	1168	
				2.4 V	7.14	26.3	99.6	225	470	18	66	249	563	1175	
				3 V	7.31	26.6	100.0	226	474	18	67	250	565	1185	
				3.6 V	7.41	26.9	102.0	229	480	19	67	255	573	1200	
		RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	6.91	25.2	93.4	210	440	17	63	234	525	1100	
				2.4 V	7.04	25.3	94.2	211	443	18	63	236	528	1108	
				3 V	7.19	25.7	95.0	212	446	18	64	238	530	1115	
				3.6 V	7.97	26.0	96.1	215	451	20	65	240	538	1128	
		RTC clocked by LSE quartz(3) in low drive mode	LCD disabled	1.8 V	6.85	25.0	93.0	208.3	-	17	63	233	521	-	
				2.4 V	6.94	25.1	93.2	209.3	-	17	63	233	523	-	
				3 V	7.10	25.2	93.6	210.3	-	18	63	234	526	-	
				3.6 V	7.34	25.4	94.1	212.3	-	18	64	235	531	-	

Table 40. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	USART2 independent clock domain	4.1	3.6	3.8	µA/MHz
	USART2 APB clock domain	1.4	1.1	1.5	
	USART3 independent clock domain	4.7	4.1	4.2	
	USART3 APB clock domain	1.5	1.3	1.7	
	UART4 independent clock domain	3.9	3.2	3.5	
	UART4 APB clock domain	1.5	1.3	1.6	
	UART5 independent clock domain	3.9	3.2	3.5	
	UART5 APB clock domain	1.3	1.2	1.4	
	WWDG	0.5	0.5	0.5	
	All APB1 on	84.2	70.7	80.2	
APB2	AHB to APB2 bridge(4)	1.0	0.9	0.9	
	DFSDM	5.6	4.6	5.3	
	FW	0.7	0.5	0.7	
	SAI1 independent clock domain	2.6	2.1	2.3	
	SAI1 APB clock domain	2.1	1.8	2.0	
	SAI2 independent clock domain	3.3	2.7	3.0	
	SAI2 APB clock domain	2.4	2.1	2.2	
	SDMMC1 independent clock domain	4.7	3.9	4.2	
	SDMMC1 APB clock domain	2.5	1.9	2.1	
	SPI1	2.0	1.6	1.9	
	SYSCFG/VREFBUF/COMP	0.6	0.4	0.5	
	TIM1	8.3	6.9	7.9	
	TIM8	8.6	7.1	8.1	
	TIM15	4.1	3.4	3.9	
	TIM16	3.0	2.5	2.9	
	TIM17	3.0	2.4	2.9	
	USART1 independent clock domain	4.9	4.0	4.4	
	USART1 APB clock domain	1.5	1.3	1.7	
	All APB2 on	56.8	43.3	48.2	
ALL		256.8	189.6	215.5	

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

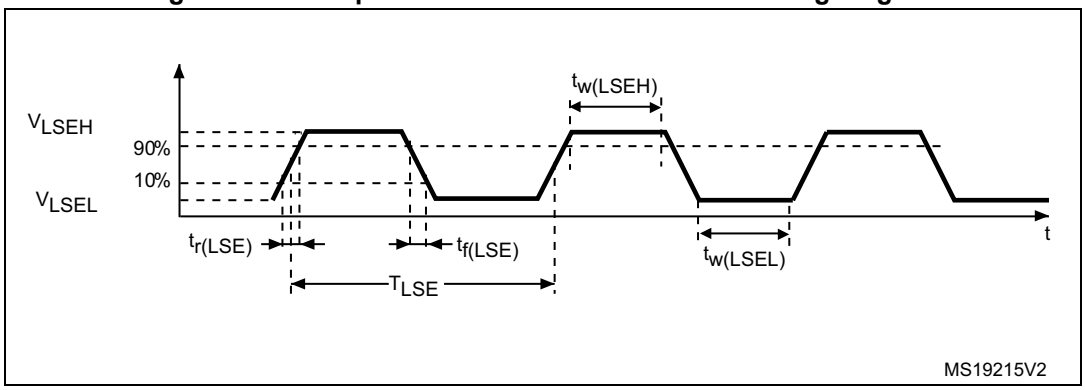
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 17*.

Table 44. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

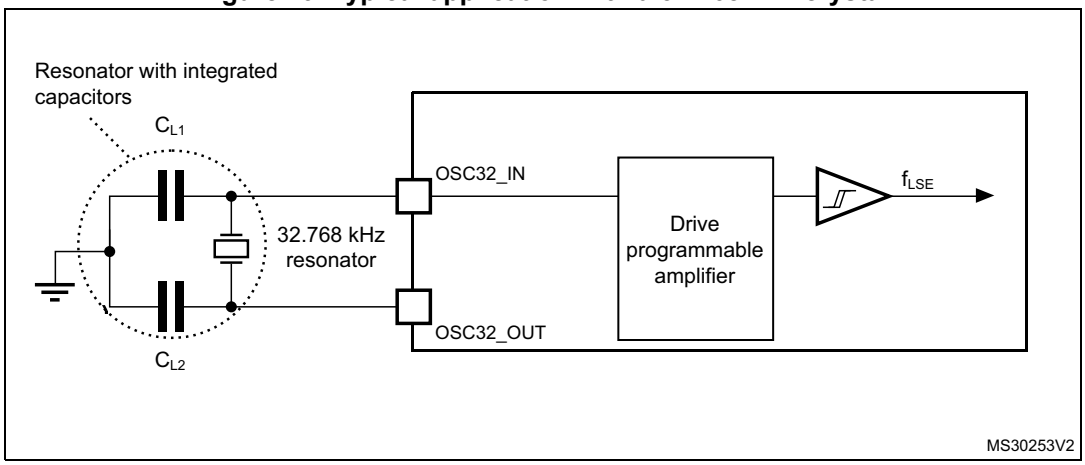
Figure 17. Low-speed external clock source AC timing diagram



1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Figure 20. HSI16 frequency versus temperature

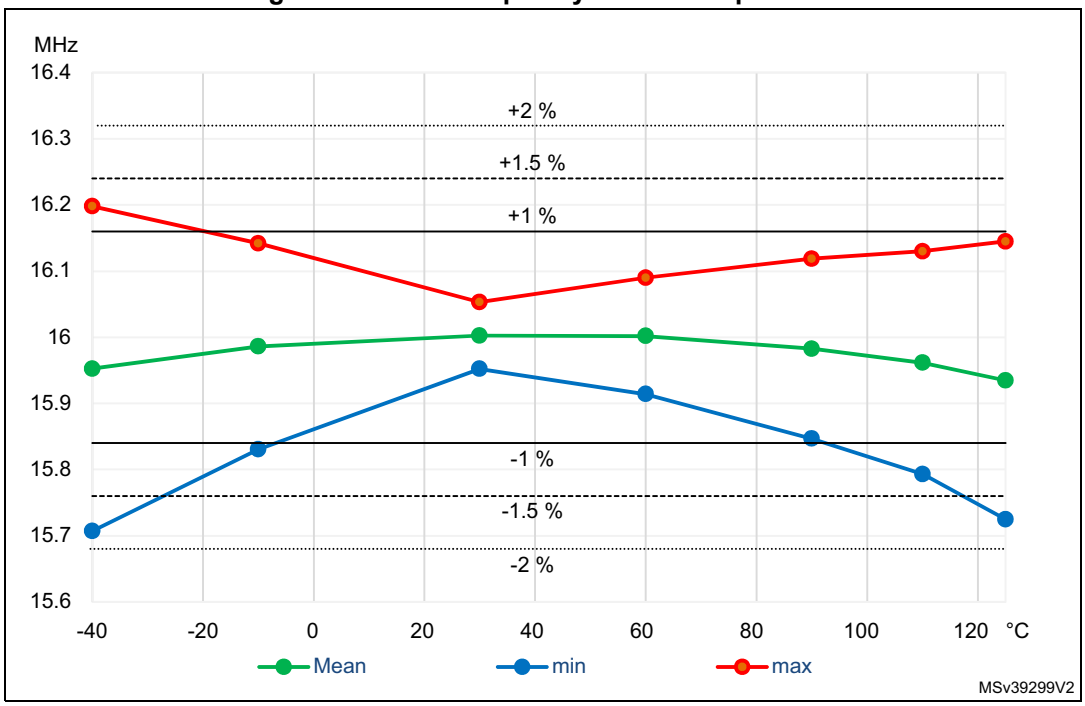


Table 66. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 67. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

6.3.28 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 90* to *Table 103* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 37 through *Figure 40* represent asynchronous waveforms and *Table 90* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Figure 37. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

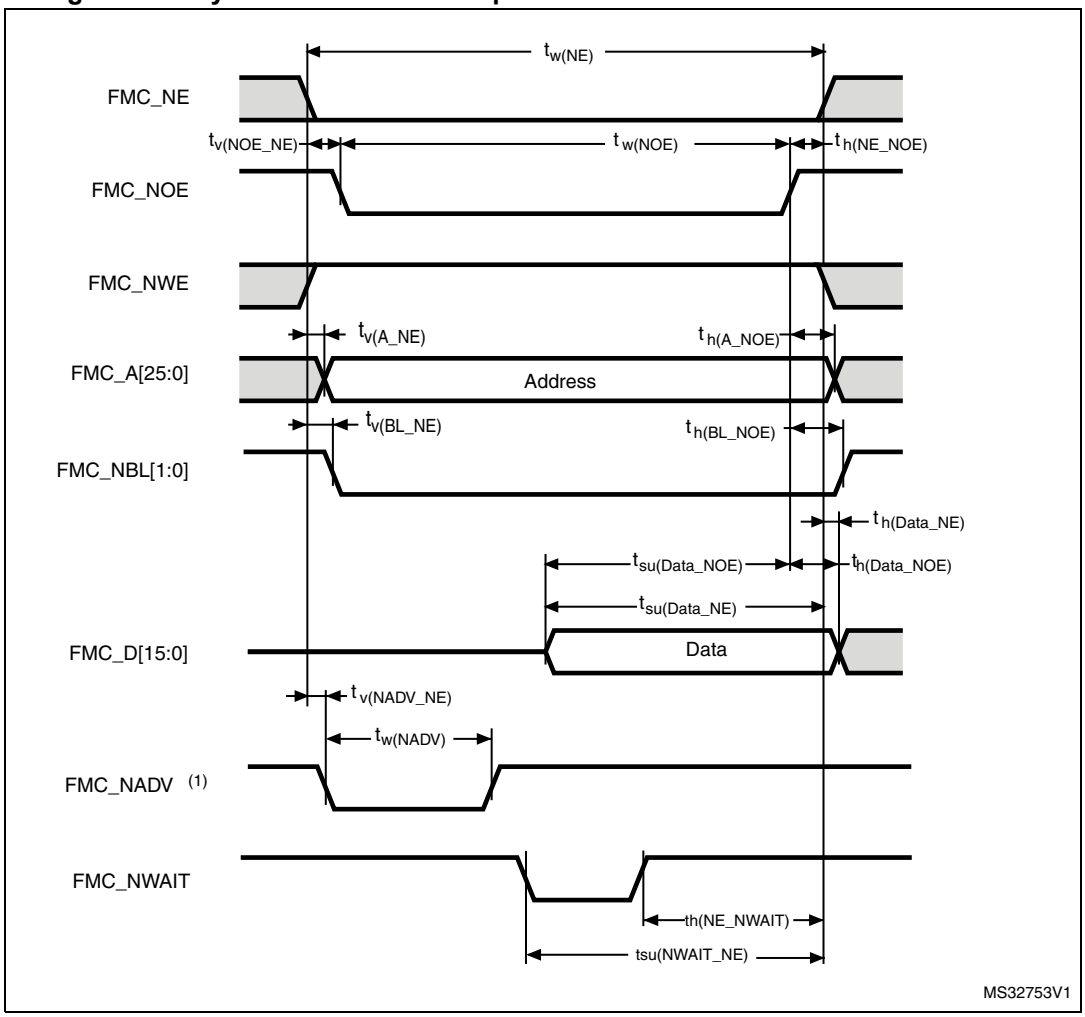


Table 96. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2xT_{HCLK}$-1.5	$2xT_{HCLK}$+1.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK} +4	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} +0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 97. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+2	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$-1.5	$7T_{HCLK}$+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$-3	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 41 through *Figure 44* represent synchronous waveforms and *Table 98* through *Table 101* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

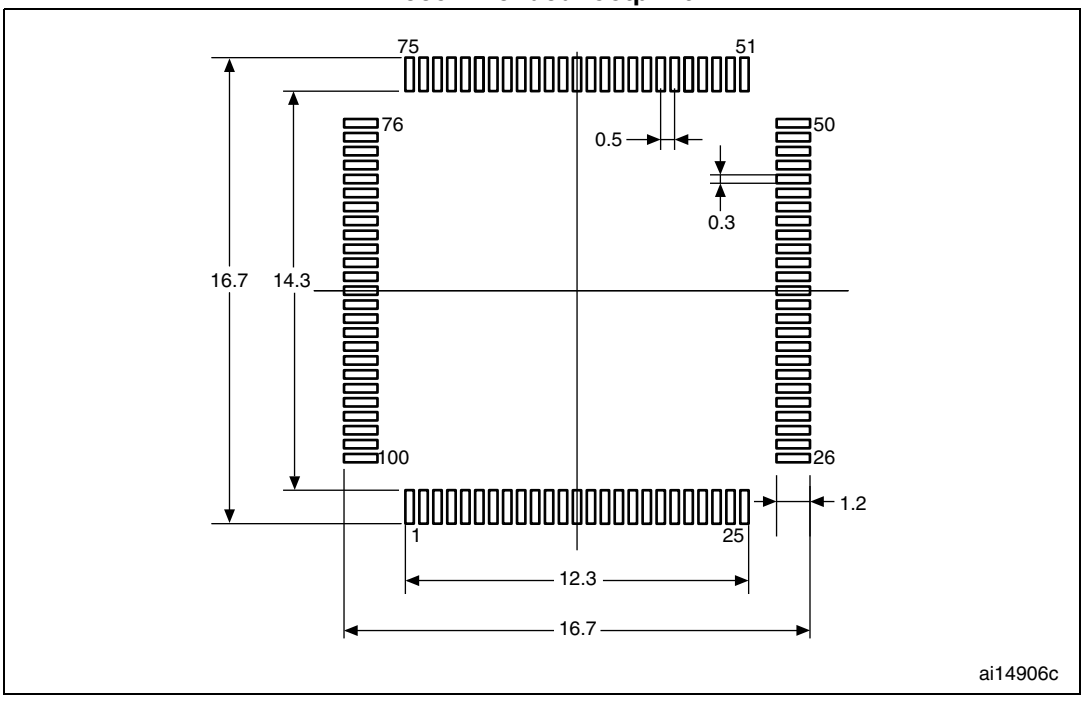
- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 56. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

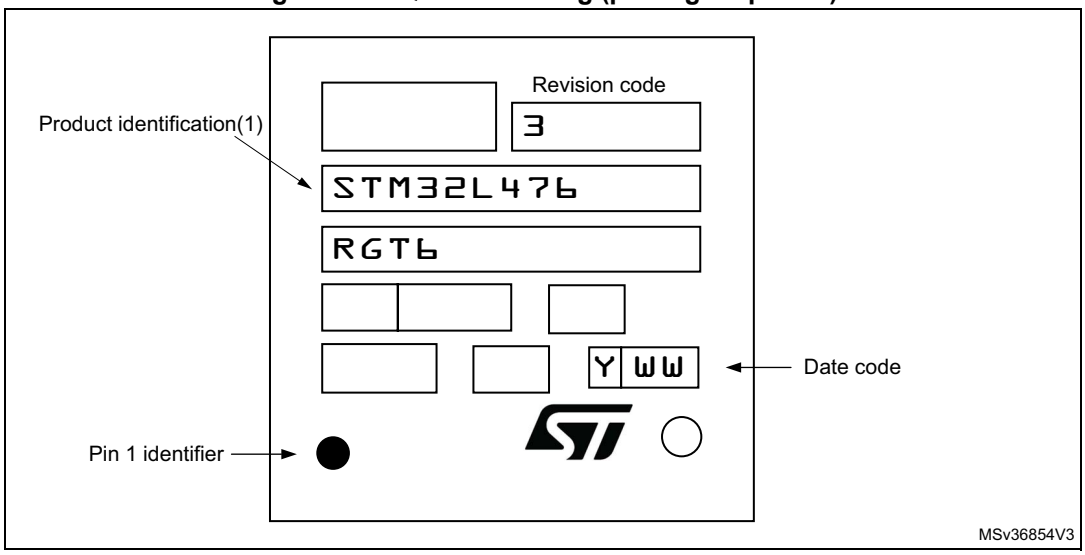


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 66. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 115. Document revision history (continued)

Date	Revision	Changes
03-Dec-2015	4	In all the document: – Stop 1 with main regulator becomes Stop 0 – Stop 1 with low-power regulator remains as Stop 1. In *Section 4: Pinouts and pin description*: – PC14/OSC32_IN becomes PC14-OSC32_IN (PC14) – PC15/OSC32_OUT becomes PC15-OSC32_OUT (PC15) – PH0/OSC_IN becomes PH0-OSC_IN (PH0) – PH1/OSC_OUT becomes PH1-OSC_OUT (PH1) – PA13 becomes PA13 (JTMS-SWDIO) – PA14 becomes PA14 (JTCK-SWCLK) – PA15 becomes PA15 (JTDI) – PB3 becomes PB3 (JTDO-TRACESWO) – PB4 becomes PB4 (NJTRST). Added *Table 12: STM32L4x6 USART/UART/LPUART features*. Added *Note 5.* Updated *Table 25: Embedded internal voltage reference*. Updated *Table 34: Current consumption in Stop 2 mode*. Updated *Table 35: Current consumption in Stop 1 mode*. Updated *Table 36: Current consumption in Stop 0 mode*. Updated *Table 37: Current consumption in Standby mode*. Updated *Table 38: Current consumption in Shutdown mode*. Updated *Table 41: Low-power mode wakeup timings*. Added *Figure 15: VREFINT versus temperature*. Updated *Figure 20: HSI16 frequency versus temperature*. Updated *Table 58: I/O static characteristics*. Updated *Table 69: DAC characteristics*. Updated *Figure 52: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline*. Updated *Table 105: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data*.