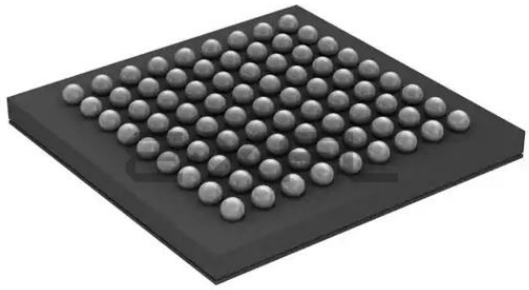

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## What is "Embedded - Microcontrollers"?

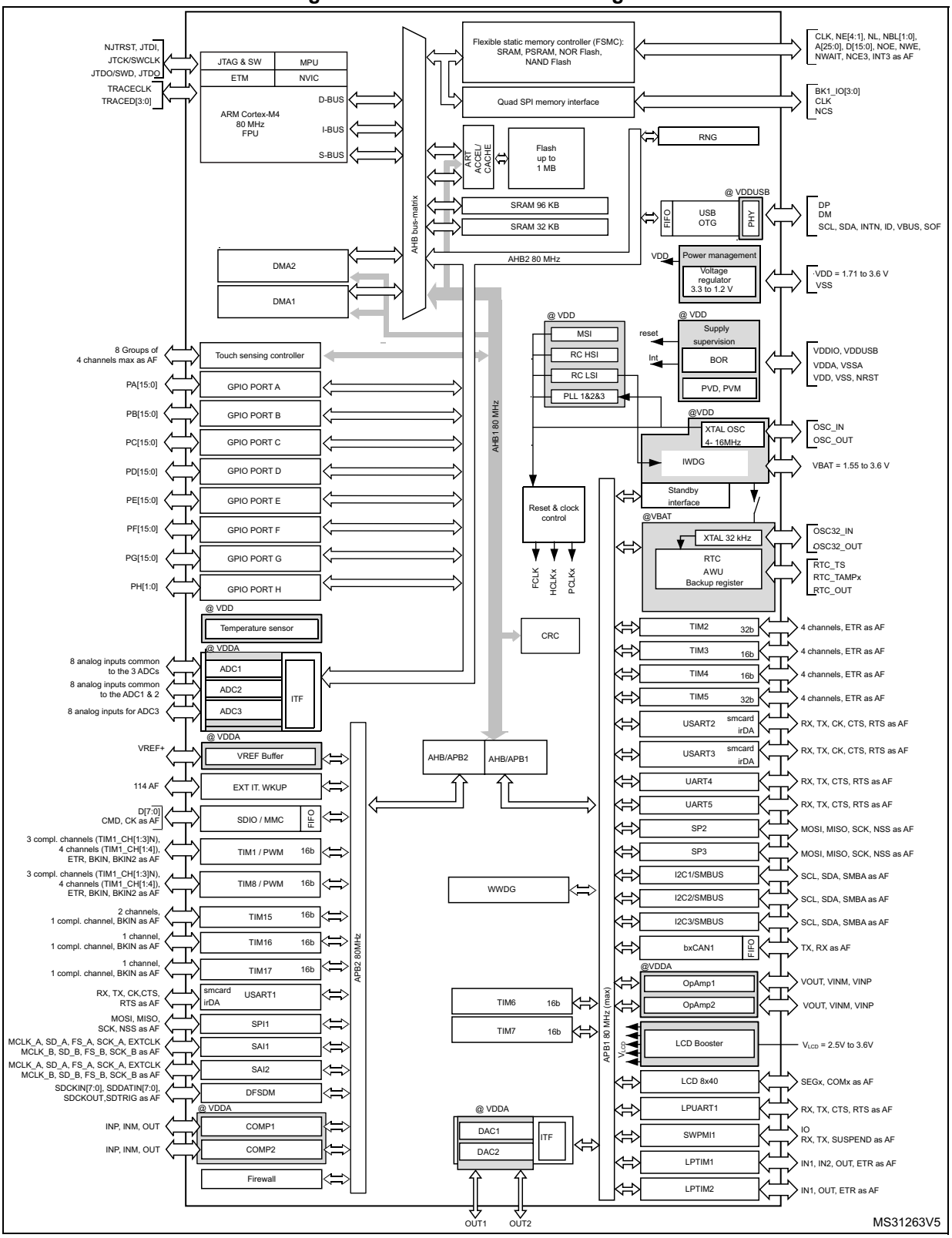
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, PWM, WDT |
| Number of I/O | 65 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 81-UFBGA, WLCSP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476mgy6tr |

# List of tables

**Figure 1. STM32L476xx block diagram**




*Note: AF: alternate function on I/O pins.*

Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

## 3.28 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

| Pin Number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP72 | WLCSP81 | LQFP100 | UFBGA132 | LQFP144 | | | | | Alternate functions | Additional functions |
| - | - | - | 45 | M11 | 67 | PE14 | I/O | FT | - | TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT | - |
| - | - | - | 46 | M12 | 68 | PE15 | I/O | FT | - | TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT | - |
| 29 | H3 | H3 | 47 | L10 | 69 | PB10 | I/O | FT_fl | - | TIM2_CH3, I2C2_SCL, SPI2_SCK, DFSDM_DATIN7, USART3_TX, LPUART1_RX, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT | - |
| 30 | G3 | G3 | 48 | L11 | 70 | PB11 | I/O | FT_fl | - | TIM2_CH4, I2C2_SDA, DFSDM_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT | - |
| 31 | J2 | J2 | 49 | F12 | 71 | VSS | S | - | - | - | - |
| 32 | J1 | J1 | 50 | G12 | 72 | VDD | S | - | - | - | - |
| 33 | H1 | H1 | 51 | L12 | 73 | PB12 | I/O | FT_l | - | TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT | - |

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

| Pin Number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP72 | WLCSP81 | LQFP100 | UFBGA132 | LQFP144 | | | | | Alternate functions | Additional functions |
| 45 | C1 | C1 | 71 | A12 | 104 | PA12 | I/O | FT_u | - | TIM1_ETR, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT | - |
| 46 | C2 | C2 | 72 | A11 | 105 | PA13 (JTMS-SWDIO) | I/O | FT | (3) | JTMS-SWDIO, IR_OUT, OTG_FS_NOE, EVENTOUT | - |
| 47 | B1 | B1 | - | - | - | VSS | S | - | - | - | - |
| 48 | A1 | A1 | 73 | C11 | 106 | VDDUSB | S | - | - | - | - |
| - | - | - | 74 | F11 | 107 | VSS | S | - | - | - | - |
| - | - | - | 75 | G11 | 108 | VDD | S | - | - | - | - |
| 49 | B2 | B2 | 76 | A10 | 109 | PA14 (JTCK-SWCLK) | I/O | FT | (3) | JTCK-SWCLK, EVENTOUT | - |
| 50 | A2 | A2 | 77 | A9 | 110 | PA15 (JTDI) | I/O | FT_l | (3) | JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, SPI3_NSS, UART4_RTS_DE, TSC_G3_IO1, LCD_SEG17, SAI2_FS_B, EVENTOUT | - |
| 51 | D3 | D3 | 78 | B11 | 111 | PC10 | I/O | FT_l | - | SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, LCD_COM4/LCD_SEG28/ LCD_SEG40, SDMMC1_D2, SAI2_SCK_B, EVENTOUT | - |
| 52 | C3 | C3 | 79 | C10 | 112 | PC11 | I/O | FT_l | - | SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, LCD_COM5/LCD_SEG29/ LCD_SEG41, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT | - |
| 53 | B3 | B3 | 80 | B10 | 113 | PC12 | I/O | FT_l | - | SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, LCD_COM6/LCD_SEG30/ LCD_SEG42, SDMMC1_CK, SAI2_SD_B, EVENTOUT | - |
| - | - | - | 81 | C9 | 114 | PD0 | I/O | FT | - | SPI2_NSS, DFSDM_DATIN7, CAN1_RX, FMC_D2, EVENTOUT | - |

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | UART4, UART5, LPUART1 | CAN1, TSC | OTG_FS, QUADSPI | LCD | SDMMC1, COMP1, COMP2, FMC, SWPMI1 | SAI1, SAI2 | TIM2, TIM15, TIM16, TIM17, LPTIM2 | EVENTOUT |
| Port C | PC0 | LPUART1_RX | - | - | LCD_SEG18 | - | - | LPTIM2_IN1 | EVENTOUT |
| | PC1 | LPUART1_TX | - | - | LCD_SEG19 | - | - | - | EVENTOUT |
| | PC2 | - | - | - | LCD_SEG20 | - | - | - | EVENTOUT |
| | PC3 | - | - | - | LCD_VLCD | - | SAI1_SD_A | LPTIM2_ETR | EVENTOUT |
| | PC4 | - | - | - | LCD_SEG22 | - | - | - | EVENTOUT |
| | PC5 | - | - | - | LCD_SEG23 | - | - | - | EVENTOUT |
| | PC6 | - | TSC_G4_IO1 | - | LCD_SEG24 | SDMMC1_D6 | SAI2_MCLK_A | - | EVENTOUT |
| | PC7 | - | TSC_G4_IO2 | - | LCD_SEG25 | SDMMC1_D7 | SAI2_MCLK_B | - | EVENTOUT |
| | PC8 | - | TSC_G4_IO3 | - | LCD_SEG26 | SDMMC1_D0 | - | - | EVENTOUT |
| | PC9 | - | TSC_G4_IO4 | OTG_FS_NOE | LCD_SEG27 | SDMMC1_D1 | SAI2_EXTCLK | TIM8_BKIN2_COMP1 | EVENTOUT |
| | PC10 | UART4_TX | TSC_G3_IO2 | - | LCD_COM4/ LCD_SEG28/ LCD_SEG40 | SDMMC1_D2 | SAI2_SCK_B | - | EVENTOUT |
| | PC11 | UART4_RX | TSC_G3_IO3 | - | LCD_COM5/ LCD_SEG29/ LCD_SEG41 | SDMMC1_D3 | SAI2_MCLK_B | - | EVENTOUT |
| | PC12 | UART5_TX | TSC_G3_IO4 | - | LCD_COM6/ LCD_SEG30/ LCD_SEG42 | SDMMC1_CK | SAI2_SD_B | - | EVENTOUT |
| | PC13 | - | - | - | - | - | - | - | EVENTOUT |
| | PC14 | - | - | - | - | - | - | - | EVENTOUT |
| | PC15 | - | - | - | - | - | - | - | EVENTOUT |

**Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)**

| Symbol | Parameter | Conditions | | | TYP | Unit | TYP | Unit |
|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | Code | 25 °C | | 25 °C | |
| $I_{DD}$(Run) | Supply current in Run mode | $f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable | Range 2 $f_{HCLK}$ = 26 MHz | Reduced code(1) | 2.9 | mA | 111 | µA/MHz |
| | | | | Coremark | 3.1 | | 118 | |
| | | | | Dhrystone 2.1 | 3.1 | | 119 | |
| | | | | Fibonacci | 2.9 | | 112 | |
| | | | | While(1) | 2.8 | | 108 | |
| | | | Range 1 $f_{HCLK}$ = 80 MHz | Reduced code(1) | 10.2 | mA | 127 | µA/MHz |
| | | | | Coremark | 10.9 | | 136 | |
| | | | | Dhrystone 2.1 | 11.0 | | 137 | |
| | | | | Fibonacci | 10.5 | | 131 | |
| | | | | While(1) | 9.9 | | 124 | |
| $I_{DD}$(LPRun) | Supply current in Low-power run | $f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable | | Reduced code(1) | 272 | µA | 136 | µA/MHz |
| | | | | Coremark | 291 | | 145 | |
| | | | | Dhrystone 2.1 | 302 | | 151 | |
| | | | | Fibonacci | 269 | | 135 | |
| | | | | While(1) | 269 | | 135 | |

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

**Table 39. Current consumption in VBAT mode**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{BAT}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$(VBAT) | Backup domain supply current | RTC disabled | 1.8 V | 4 | 29 | 196 | 587 | 1663 | 10.8 | 73 | 490 | 1468 | 4158 | nA |
| | | | 2.4 V | 5.27 | 36 | 226 | 673 | 1884 | 13.2 | 90 | 565 | 1683 | 4710 | |
| | | | 3 V | 6 | 42 | 264 | 775 | 2147 | 15.5 | 106 | 660 | 1938 | 5368 | |
| | | | 3.6 V | 10 | 58 | 323 | 919 | 2488 | 25.8 | 144 | 808 | 2298 | 6220 | |
| | | RTC enabled and clocked by LSE bypassed at 32768 Hz | 1.8 V | 183 | 201 | 367 | 729 | - | - | - | - | - | - | |
| | | | 2.4 V | 268 | 295 | 486 | 901 | - | - | - | - | - | - | |
| | | | 3 V | 376 | 412 | 602 | 1075 | - | - | - | - | - | - | |
| | | | 3.6 V | 508 | 558 | 752 | 1299 | - | - | - | - | - | - | |
| | | RTC enabled and clocked by LSE quartz(2) | 1.8 V | 302 | 344 | 521 | 915 | 1978 | - | - | - | - | - | |
| | | | 2.4 V | 388 | 436 | 639 | 1091 | 2289 | - | - | - | - | - | |
| | | | 3 V | 494 | 549 | 784 | 1301 | 2656 | - | - | - | - | - | |
| | | | 3.6 V | 630 | 692 | 971 | 1571 | 3115 | - | - | - | - | - | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

**Table 42. Regulator modes transition times(1)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WULPRUN}$ | Wakeup time from Low-power run mode to Run mode(2) | Code run with MSI 2 MHz | 5 | 7 | µs |
| $t_{VOST}$ | Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3) | Code run with MSI 24 MHz | 20 | 40 | |

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

## 6.3.7 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

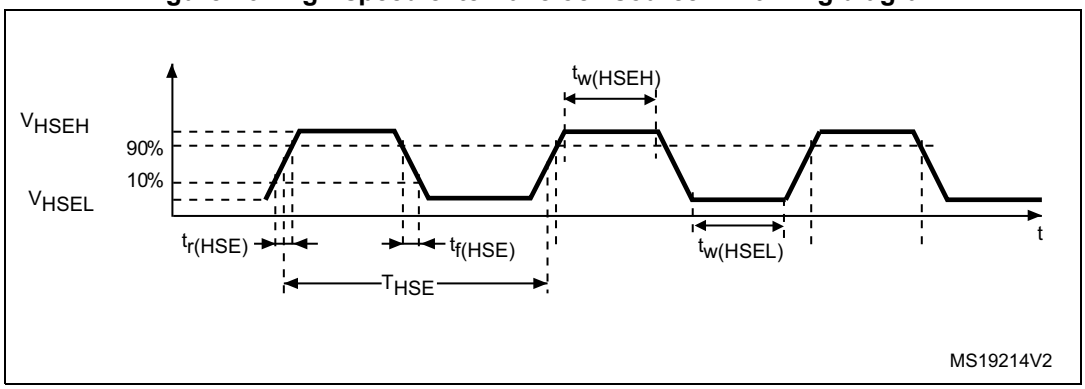
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16: High-speed external clock source AC timing diagram*.

**Table 43. High-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | Voltage scaling Range 1 | - | 8 | 48 | MHz |
| | | Voltage scaling Range 2 | - | 8 | 26 | |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | - | 0.7 $V_{DDIOx}$ | - | $V_{DDIOx}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DDIOx}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | Voltage scaling Range 1 | 7 | - | - | ns |
| | | Voltage scaling Range 2 | 18 | - | - | |

1. Guaranteed by design.

**Figure 16. High-speed external clock source AC timing diagram**



## 6.3.8 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

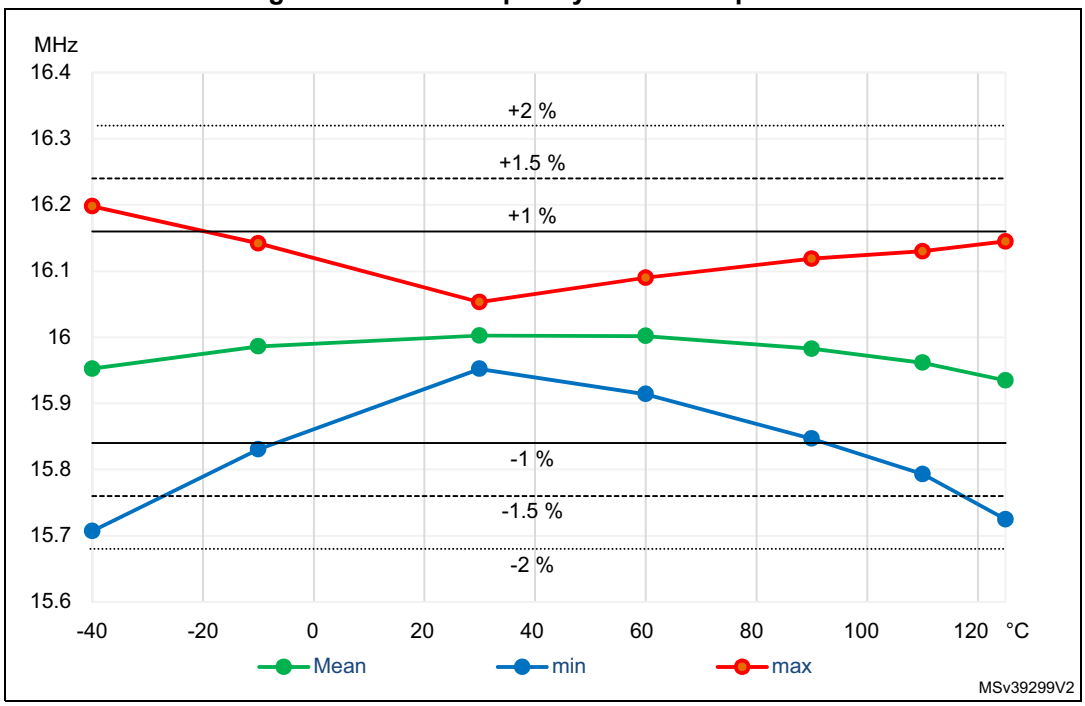
### High-speed internal (HSI16) RC oscillator

**Table 47. HSI16 oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI16}$ | HSI16 Frequency | $V_{DD}$=3.0 V, $T_A$=30 °C | 15.88 | - | 16.08 | MHz |
| TRIM | HSI16 user trimming step | Trimming code is not a multiple of 64 | 0.2 | 0.3 | 0.4 | % |
| | | Trimming code is a multiple of 64 | -4 | -6 | -8 | |
| DuCy(HSI16)(2) | Duty Cycle | - | 45 | - | 55 | % |
| $\Delta_{Temp}$(HSI16) | HSI16 oscillator frequency drift over temperature | $T_A$= 0 to 85 °C | -1 | - | 1 | % |
| | | $T_A$= -40 to 125 °C | -2 | - | 1.5 | % |
| $\Delta_{VDD}$(HSI16) | HSI16 oscillator frequency drift over $V_{DD}$ | $V_{DD}$=1.62 V to 3.6 V | -0.1 | - | 0.05 | % |
| $t_{su}$(HSI16)(2) | HSI16 oscillator start-up time | - | - | 0.8 | 1.2 | µs |
| $t_{stab}$(HSI16)(2) | HSI16 oscillator stabilization time | - | - | 3 | 5 | µs |
| $I_{DD}$(HSI16)(2) | HSI16 oscillator power consumption | - | - | 155 | 190 | µA |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Figure 20. HSI16 frequency versus temperature**



### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 56. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A(1) |

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DDIOx}$ (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 57*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

**Table 57. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 pin | -0 | NA(1) | mA |
| | Injected current on pins except PA4, PA5, BOOT0 | -5 | NA(1) | |
| | Injected current on PA4, PA5 pins | -5 | 0 | |

1. NA: not applicable

**Table 60. I/O AC characteristics(1)(2)**

| Speed | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 00 | Fmax | Maximum frequency | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 5 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 1 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 0.1 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 10 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 1.5 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 0.1 | |
| | Tr/Tf | Output rise and fall time | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 25 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 52 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 140 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 17 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 37 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 110 | |
| 01 | Fmax | Maximum frequency | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 25 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 10 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 1 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 50 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 15 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 1 | |
| | Tr/Tf | Output rise and fall time | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 9 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 16 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 40 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 4.5 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 9 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 21 | |

### 6.3.17 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 63* are preliminary values derived from tests performed under ambient temperature, $f_{PCLK}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 63. ADC characteristics(1) (2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.62 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | $V_{DDA} \geq 2$ V | 2 | - | $V_{DDA}$ | V |
| | | $V_{DDA} < 2$ V | $V_{DDA}$ | | | V |
| $V_{REF-}$ | Negative reference voltage | - | $V_{SSA}$ | | | V |
| $f_{ADC}$ | ADC clock frequency | Range 1 | - | - | 80 | MHz |
| | | Range 2 | - | - | 26 | |
| $f_s$ | Sampling rate for FAST channels | Resolution = 12 bits | - | - | 5.33 | Msps |
| | | Resolution = 10 bits | - | - | 6.15 | |
| | | Resolution = 8 bits | - | - | 7.27 | |
| | | Resolution = 6 bits | - | - | 8.88 | |
| | Sampling rate for SLOW channels | Resolution = 12 bits | - | - | 4.21 | |
| | | Resolution = 10 bits | - | - | 4.71 | |
| | | Resolution = 8 bits | - | - | 5.33 | |
| | | Resolution = 6 bits | - | - | 6.15 | |
| $f_{TRIG}$ | External trigger frequency | $f_{ADC}$ = 80 MHz Resolution = 12 bits | - | - | 5.33 | MHz |
| | | Resolution = 12 bits | - | - | 15 | $1/f_{ADC}$ |
| $V_{AIN}$ (3) | Conversion voltage range(2) | - | 0 | - | $V_{REF+}$ | V |
| $R_{AIN}$ | External input impedance | - | - | - | 50 | kΩ |
| $C_{ADC}$ | Internal sample and hold capacitor | - | - | 5 | - | pF |
| $t_{STAB}$ | Power-up time | - | 1 | | | conversion cycle |
| $t_{CAL}$ | Calibration time | $f_{ADC}$ = 80 MHz | 1.45 | | | µs |
| | | - | 116 | | | $1/f_{ADC}$ |
| $t_{LATR}$ | Trigger conversion latency Regular and injected channels without conversion abort | CKMODE = 00 | 1.5 | 2 | 2.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | - | - | 2.0 | |
| | | CKMODE = 10 | - | - | 2.25 | |
| | | CKMODE = 11 | - | - | 2.125 | |

**Table 65. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)**

| Sym-bol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+}$ = 3 V, TA = 25 °C | Single ended | Fast channel (max speed) | - | -74 | -73 | dB |
| | | | | Slow channel (max speed) | - | -74 | -73 | |
| | | | Differential | Fast channel (max speed) | - | -79 | -76 | |
| | | | | Slow channel (max speed) | - | -79 | -76 | |

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4 V). It is disable when $V_{DDA}$ ≥ 2.4 V. No oversampling.

**Table 94. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}$-0.5 | $3T_{HCLK}$+2 | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | $2T_{HCLK}$-0.5 | $2T_{HCLK}$+0.5 | |
| $t_{w(NOE)}$ | FMC_NOE low time | $T_{HCLK}$+0.5 | $T_{HCLK}$+1 | |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 3 | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 1 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{HCLK}$-0.5 | $T_{HCLK}$+1 | |
| $t_{h(AD\_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high | 0 | - | |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | $T_{HCLK}$-0.5 | - | |
| $t_{h(BL\_NOE)}$ | FMC_BL time after FMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 2 | |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK}$-2 | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time | $T_{HCLK}$-1 | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. CL = 30 pF.
2. Guaranteed by characterization results.

**Table 95. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)**

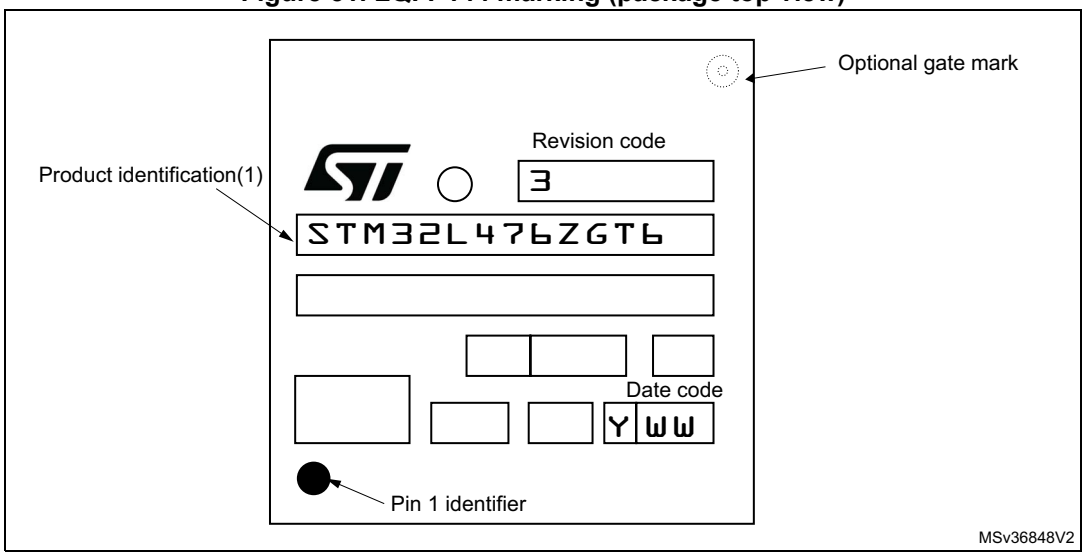
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}$+2 | $8T_{HCLK}$+4 | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{HCLK}$-1 | $5T_{HCLK}$+1.5 | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{HCLK}$+1.5 | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}$+1 | - | |

1. CL = 30 pF.
2. Guaranteed by characterization results.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 51. LQFP144 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

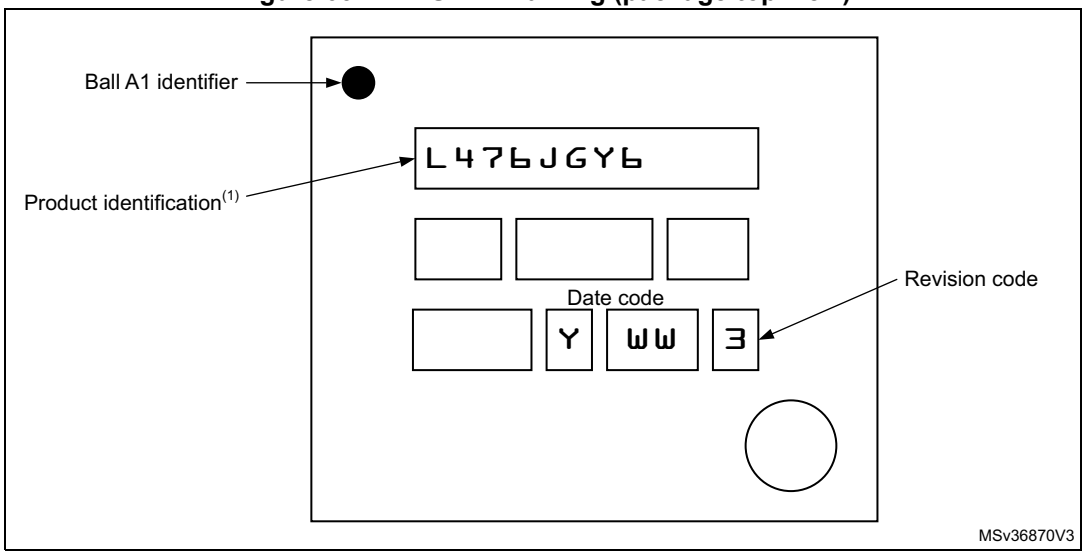
**Table 111. WLCSP72 recommended PCB design rules (0.4 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typ. (depends on the solder mask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

## Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

**Figure 63. WLCSP72 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Part numbering

**Table 114. STM32L476xx ordering information scheme**

Example: STM32 L 476 R G T 6 TR

**Device family**

STM32 = ARM® based 32-bit microcontroller

**Product type**

L = ultra-low-power

**Device subfamily**

476: STM32L476xx

**Pin count**

R = 64 pins

J = 72 pins

M = 81 pins

V = 100 pins

Q = 132 pins

Z = 144 pins

**Flash memory size**

C = 256 KB of Flash memory

E = 512 KB of Flash memory

G = 1 MB of Flash memory

**Package**

T = LQFP ECOPACK®2

I = UFBGA ECOPACK®2

Y = CSP ECOPACK®2

**Temperature range**

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

**Packing**

TR = tape and reel

xxx = programmed parts