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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	109
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476qgi6p

Contents

Table 2. STM32L476xx family device features and peripheral counts (continued)

Peripheral	STM32L476 Zx	STM32L476 Qx	STM32L476 Vx	STM32L476 Mx	STM32L476 Jx	STM32L476 Rx
Max. CPU frequency	80 MHz					
Operating voltage	1.71 to 3.6 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C					
Packages	LQFP144	UFBGA132	LQFP100	WLCSP81	WLCSP72	LQFP64

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	59	J10	81	PD12	I/O	FT_l	-	TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	-	60	H12	82	PD13	I/O	FT_l	-	TIM4_CH2, TSC_G6_IO4, LCD_SEG33, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	83	VSS	S	-	-	-	-
-	-	-	-	-	84	VDD	S	-	-	-	-
-	-	-	61	H11	85	PD14	I/O	FT_l	-	TIM4_CH3, LCD_SEG34, FMC_D0, EVENTOUT	-
-	-	-	62	H10	86	PD15	I/O	FT_l	-	TIM4_CH4, LCD_SEG35, FMC_D1, EVENTOUT	-
-	-	-	-	G10	87	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	F9	88	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	F10	89	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	E9	90	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	-	-	G4	91	PG6	I/O	FT_s	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-
-	-	-	-	H4	92	PG7	I/O	FT_fs	-	I2C3_SCL, LPUART1_TX, FMC_INT3, EVENTOUT	-
-	-	-	-	J6	93	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	95	VDDIO2	S	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

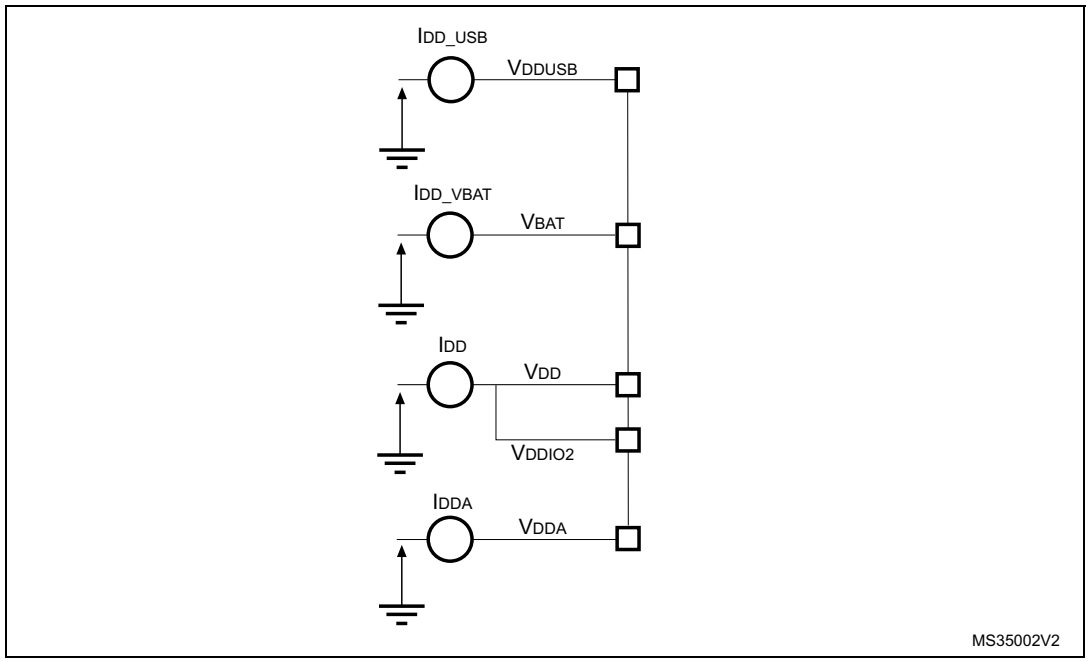
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 18. STM32L476xx memory map and peripheral register boundary addresses (1)

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI
	0xA000 0000 - 0xA000 0FFF	4 KB	FMC
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5004 0400 - 0x5006 07FF	129 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) + 4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 34. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	1.8 V	1.42	4.04	15	34.9	77.2	3.1	10	38	87	193	µA
			2.4 V	1.5	4.22	15.4	35.7	79.2	3.2	11	39	89	198	
			3 V	1.64	4.37	15.8	36.7	81.4	3.4	11	40	92	204	
			3.6 V	1.79	4.65	16.6	38.4	85.4	3.6	12	42	96	214	
		RTC clocked by LSI, LCD enabled(3)	1.8 V	1.53	4.07	15.1	35.1	77.4	3.3	10	38	88	194	
			2.4 V	1.62	4.32	15.5	35.9	79.5	3.4	11	39	90	199	
			3 V	1.69	4.43	15.9	36.8	81.7	3.5	11	40	92	204	
			3.6 V	1.86	4.65	16.7	38.5	85.5	3.7	12	42	96	214	
		RTC clocked by LSE bypassed at 32768Hz,LCD disabled	1.8 V	1.5	4.13	15.2	35.3	77.6	3.2	10	38	88	194	
			2.4 V	1.63	4.33	15.6	36	79.6	3.4	11	39	90	199	
			3 V	1.79	4.55	16.1	37	81.8	3.6	11	40	93	205	
			3.6 V	2.04	4.9	16.8	38.7	85.6	3.9	12	42	97	214	
		RTC clocked by LSE quartz(4) in low drive mode, LCD disabled	1.8 V	1.43	3.99	14.7	35	-	3.2	10	37	88	-	
			2.4 V	1.54	4.11	15	35.8	-	3.3	10	38	90	-	
			3 V	1.67	4.29	15.5	36.7	-	3.4	11	39	92	-	
			3.6 V	1.87	4.57	16.2	38.3	-	3.7	11	41	96	-	
I_{DD}(wakeup from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See (5).	3 V	1.9	-	-	-	-	-					mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (5).	3 V	2.24	-	-	-	-						
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See (5).	3 V	2.1	-	-	-	-						

1. Guaranteed by characterization results, unless otherwise specified.

Table 35. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	6.59	24.7	92.7	208	437	16	62	232	520	1093	µA
				2.4 V	6.65	24.8	92.9	209	439	17	62	232	523	1098	
				3 V	6.65	24.9	93.3	210	442	17	62	233	525	1105	
				3.6 V	6.70	25.1	93.8	212	447	17	63	235	530	1118	
		-	LCD enabled(2) clocked by LSI	1.8 V	7.00	25.2	97.2	219	461	18	63	243	548	1153	
				2.4 V	7.14	25.4	97.5	220	463	18	64	244	550	1158	
				3 V	7.24	25.7	97.7	221	465	18	64	244	553	1163	
				3.6 V	7.36	26.1	98.7	223	471	18	65	247	558	1178	
I_{DD} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	LCD disabled	1.8 V	6.88	25.0	93.1	209	439	17	63	233	523	1098	µA
				2.4 V	7.02	25.2	93.7	210	441	18	63	234	525	1103	
				3 V	7.12	25.4	94.2	212	444	18	64	236	530	1110	
				3.6 V	7.25	25.7	95.2	214	449	18	64	238	535	1123	
			LCD enabled(2)	1.8 V	7.01	26.1	99.0	223	467	18	65	248	558	1168	
				2.4 V	7.14	26.3	99.6	225	470	18	66	249	563	1175	
				3 V	7.31	26.6	100.0	226	474	18	67	250	565	1185	
				3.6 V	7.41	26.9	102.0	229	480	19	67	255	573	1200	
		RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	6.91	25.2	93.4	210	440	17	63	234	525	1100	
				2.4 V	7.04	25.3	94.2	211	443	18	63	236	528	1108	
				3 V	7.19	25.7	95.0	212	446	18	64	238	530	1115	
				3.6 V	7.97	26.0	96.1	215	451	20	65	240	538	1128	
		RTC clocked by LSE quartz(3) in low drive mode	LCD disabled	1.8 V	6.85	25.0	93.0	208.3	-	17	63	233	521	-	
				2.4 V	6.94	25.1	93.2	209.3	-	17	63	233	523	-	
				3 V	7.10	25.2	93.6	210.3	-	18	63	234	526	-	
				3.6 V	7.34	25.4	94.1	212.3	-	18	64	235	531	-	

Table 37. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	114	355	1540	4146	10735	176	888	3850	10365	26838	nA
			2.4 V	138	407	1795	4828	12451	223	1018	4488	12070	31128	
			3 V	150	486	2074	5589	14291	263	1215	5185	13973	35728	
			3.6 V	198	618	2608	6928	17499	383	1545	6520	17320 (2)	43748	
		with independent watchdog	1.8 V	317	-	-	-	-	-	-	-	-	-	
			2.4 V	391	-	-	-	-	-	-	-	-	-	
			3 V	438	-	-	-	-	-	-	-	-	-	
			3.6 V	566	-	-	-	-	-	-	-	-	-	
I_{DD}(Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	377	621	1873	4564	11318	491	1207	4250	10867	27537	nA
			2.4 V	464	756	2210	5348	13166	614	1436	4986	12694	31986	
			3 V	572	913	2599	6219	15197	770	1727	5815	14729	36815	
			3.6 V	722	1144	3253	7724	18696	1012	2176	7294	18275	45184	
		RTC clocked by LSI, with independent watchdog	1.8 V	456	-	-	-	-	-	-	-	-	-	
			2.4 V	557	-	-	-	-	-	-	-	-	-	
			3 V	663	-	-	-	-	-	-	-	-	-	
			3.6 V	885	-	-	-	-	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768Hz	1.8 V	289	527	1747	4402	11009	-	-	-	-	-	nA
			2.4 V	396	671	2108	5202	12869	-	-	-	-	-	
			3 V	528	853	2531	6095	14915	-	-	-	-	-	
			3.6 V	710	1111	3115	7470	18221	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	416	640	1862	4479	11908	-	-	-	-	-	
			2.4 V	514	796	2193	5236	13689	-	-	-	-	-	
			3 V	652	961	2589	6103	15598	-	-	-	-	-	
			3.6 V	821	1226	3235	7551	17947	-	-	-	-	-	

Table 41. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.2	10.2	µs
			Wakeup clock HSI16 = 16 MHz	6.3	8.99	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	10.46	
			Wakeup clock HSI16 = 16 MHz	6.3	8.87	
			Wakeup clock MSI = 4 MHz	8.0	13.23	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	4.5	5.78	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.0	6.5	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
			Wakeup clock MSI = 4 MHz	8.2	13.5	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	12.7	20	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			10.7	21.5	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.0	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
		Range 2	Wakeup clock MSI = 24 MHz	8.2	9.9	
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
			Wakeup clock MSI = 4 MHz	10.6	15.8	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.1	6.7	
			Wakeup clock HSI16 = 16 MHz	5.7	8	
		Range 2	Wakeup clock MSI = 24 MHz	5.5	6.65	
			Wakeup clock HSI16 = 16 MHz	5.7	7.53	
			Wakeup clock MSI = 4 MHz	8.2	16.6	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	20.8	µs
			Wakeup clock MSI = 4 MHz	20.1	35.5	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	24.3	µs
			Wakeup clock MSI = 4 MHz	20.1	38.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	256	330.6	µs

1. Guaranteed by characterization results.

Table 48. MSI oscillator characteristics(1) (continued)

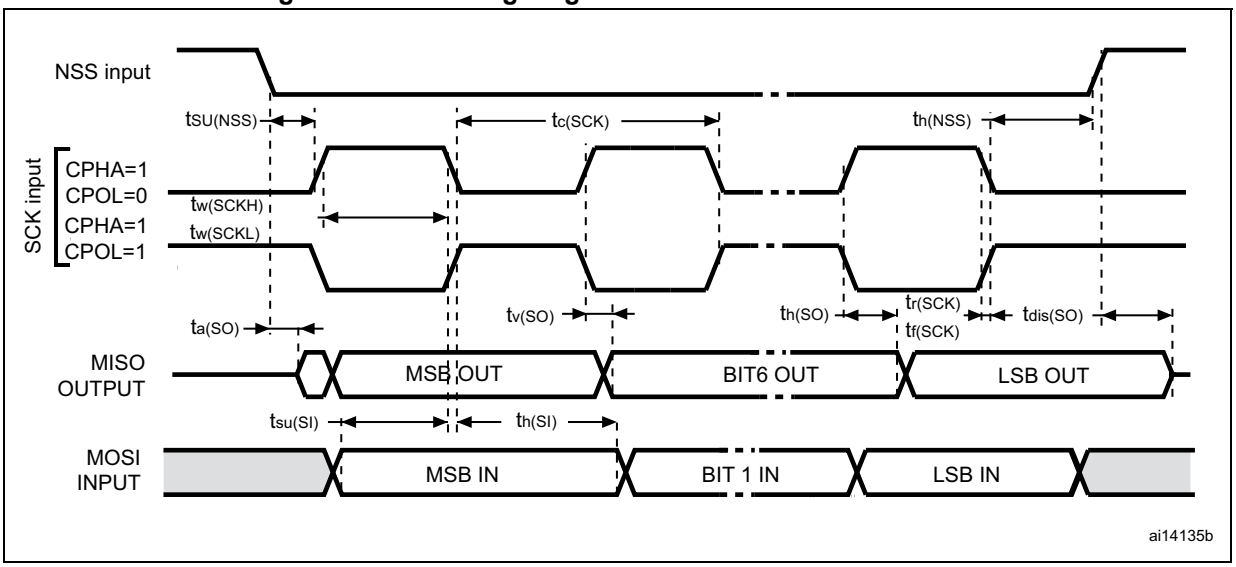
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
Δ_{VDD}(MSI)(2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)(2)(6)	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
t_{SU}(MSI)(6)	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
t_{STAB}(MSI)(6)	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

6.3.20 Comparator characteristics

Table 72. COMP characteristics(1)

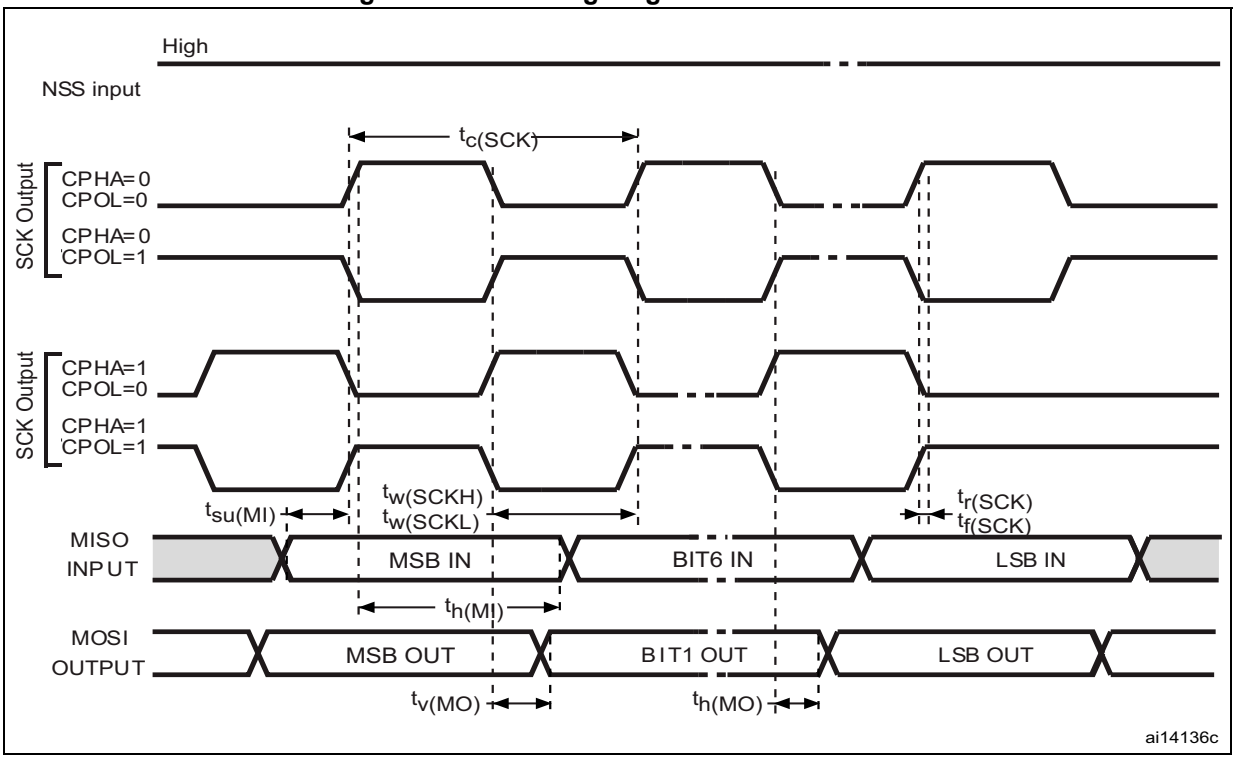
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

Figure 29. SPI timing diagram - slave mode and CPHA = 1



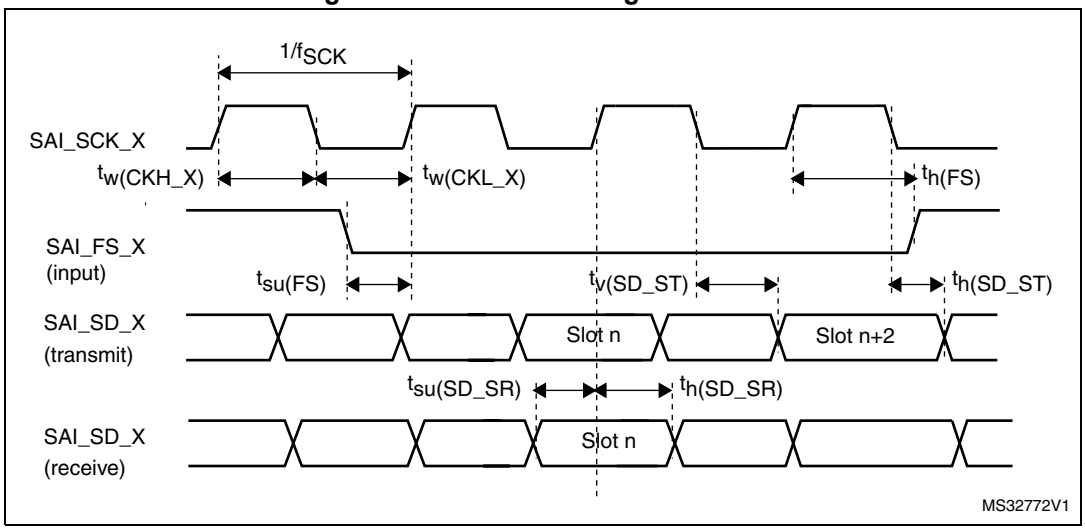
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 34. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 87* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 87. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	4.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	14	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	2	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	4.5	-	-	ns

Table 94. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-0.5	$3T_{HCLK}$+2	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	
$t_{w(NOE)}$	FMC_NOE low time	T_{HCLK}+0.5	T_{HCLK}+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	T_{HCLK}-0.5	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-2	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	T_{HCLK}-1	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$+2	$8T_{HCLK}$+4	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-1	$5T_{HCLK}$+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+1.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 45. NAND controller waveforms for read access

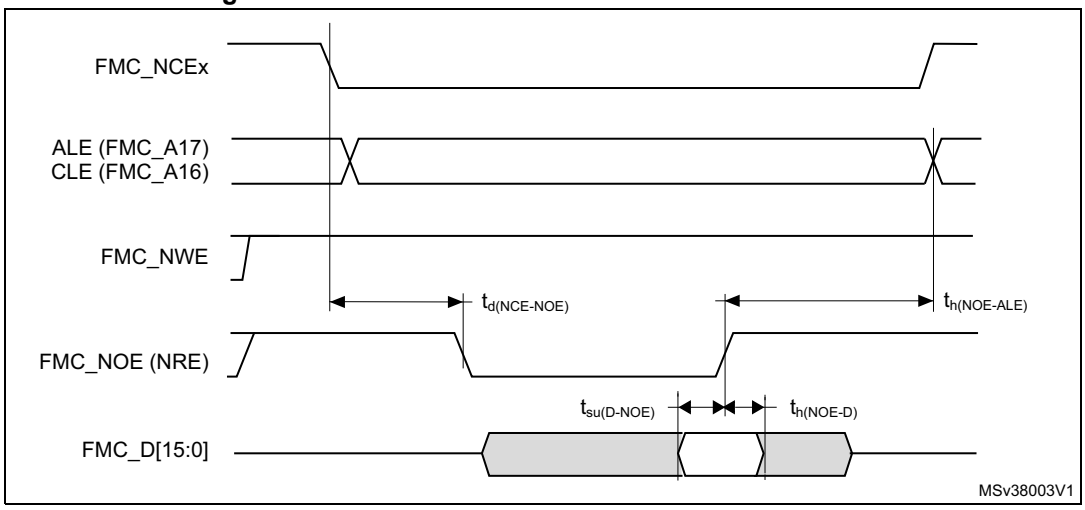


Figure 46. NAND controller waveforms for write access

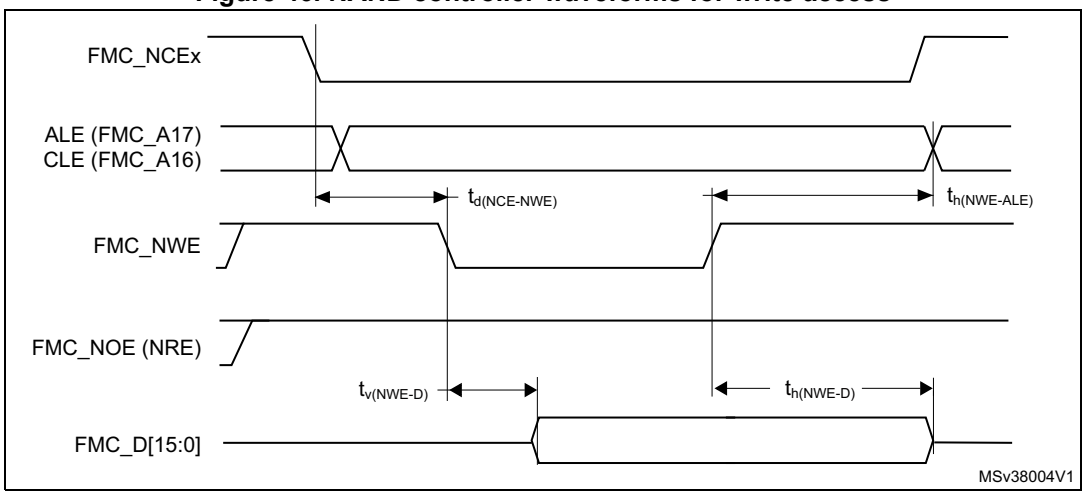


Figure 47. NAND controller waveforms for common memory read access

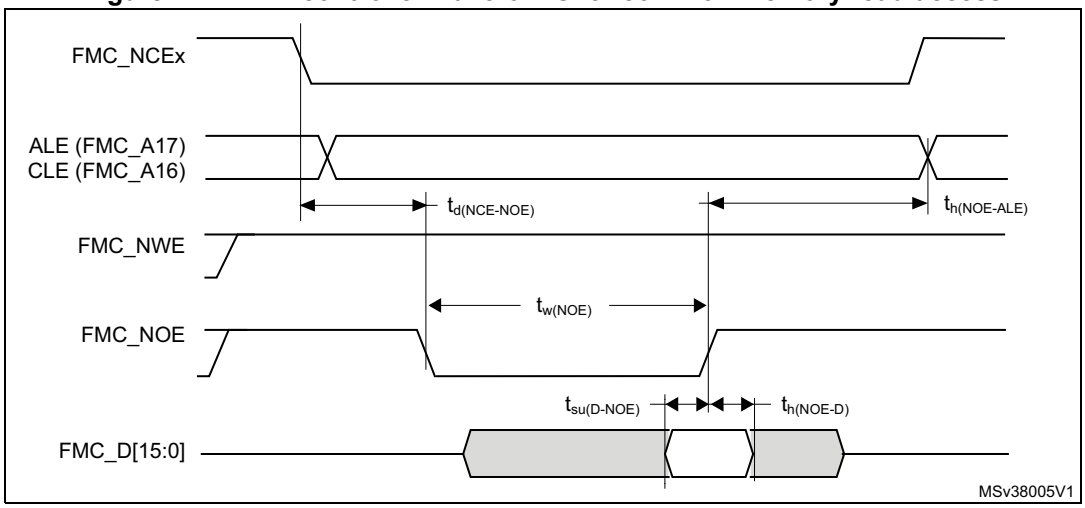


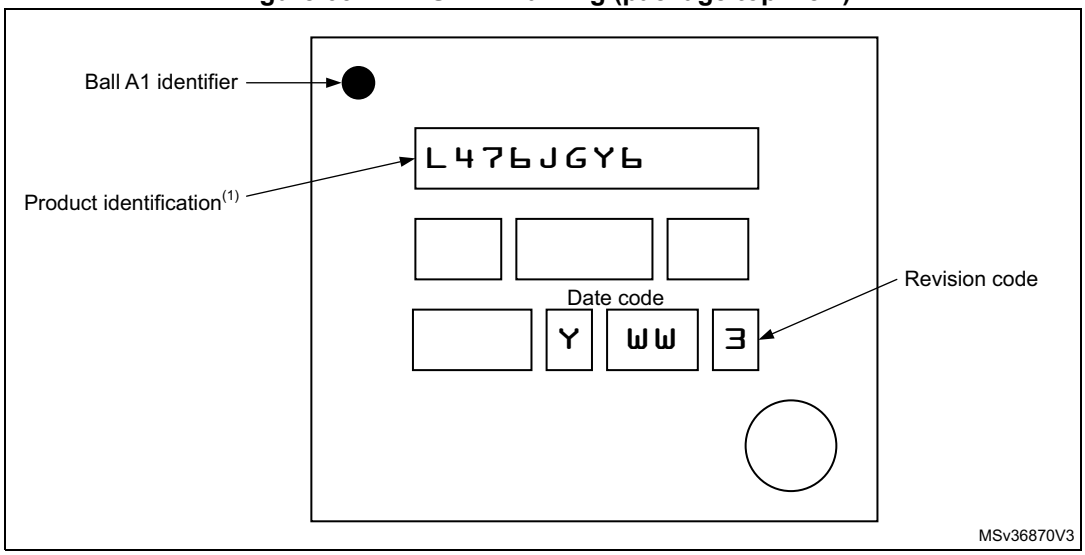
Table 111. WLCSP72 recommended PCB design rules (0.4 mm pitch BGA)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 63. WLCSP72 marking (package top view)



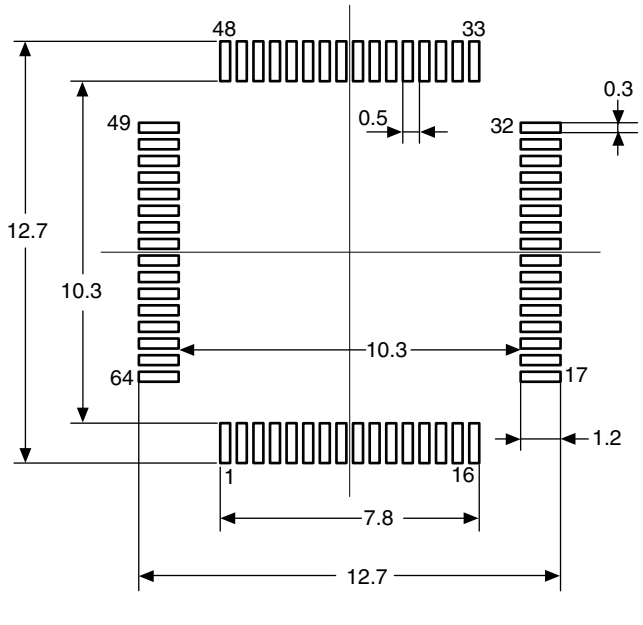
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 112. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 65. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.