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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476ret6

Table 2. STM32L476xx family device features and peripheral counts (continued)

Peripheral	STM32L476 Zx	STM32L476 Qx	STM32L476 Vx	STM32L476 Mx	STM32L476 Jx	STM32L476 Rx
Max. CPU frequency	80 MHz					
Operating voltage	1.71 to 3.6 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C					
Packages	LQFP144	UFBGA132	LQFP100	WLCSP81	WLCSP72	LQFP64

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in

3.11 Clocks and startup

The clock controller (see *Figure 3*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

3.19 Operational amplifier (OPAMP)

The STM32L476xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
34	H2	H2	52	K12	74	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM_CKIN1, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SWPMI1_TX, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
35	G2	G2	53	K11	75	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM_DATIN2, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
36	G1	G1	54	K10	76	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM_CKIN2, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	F5	55	K9	77	PD8	I/O	FT_l	-	USART3_TX, LCD_SEG28, FMC_D13, EVENTOUT	-
-	-	F4	56	K8	78	PD9	I/O	FT_l	-	USART3_RX, LCD_SEG29, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	-	-	57	J12	79	PD10	I/O	FT_l	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	58	J11	80	PD11	I/O	FT_l	-	USART3_CTS, TSC_G6_IO2, LCD_SEG31, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	-	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	-	-	-	-	TIM15_CH2	EVENTOUT
	PF11	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

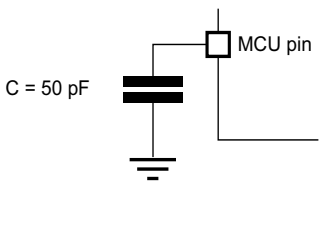
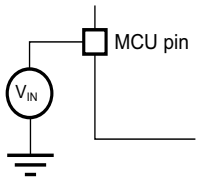
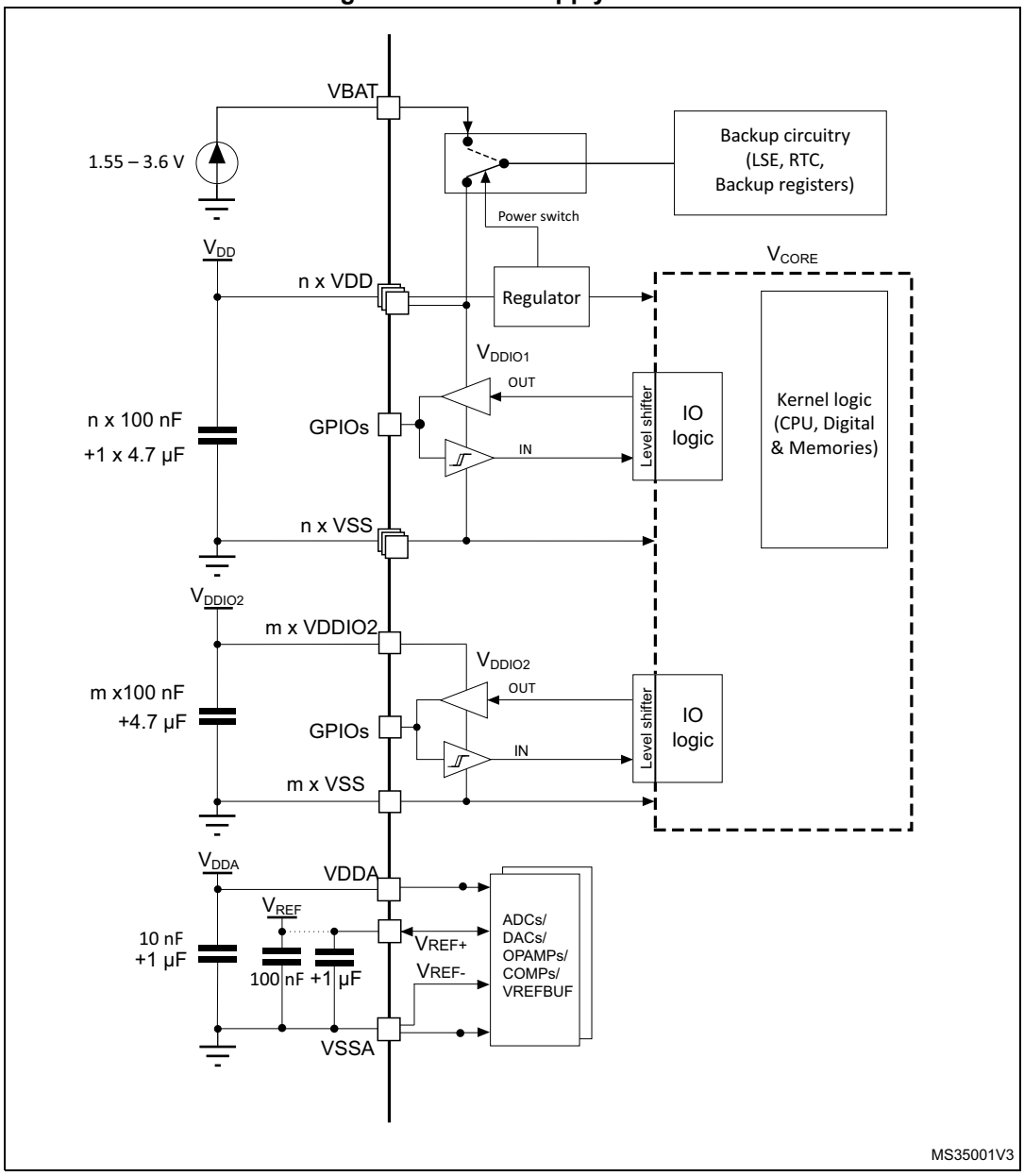


Figure 12. Pin input voltage



6.1.6 Power supply scheme

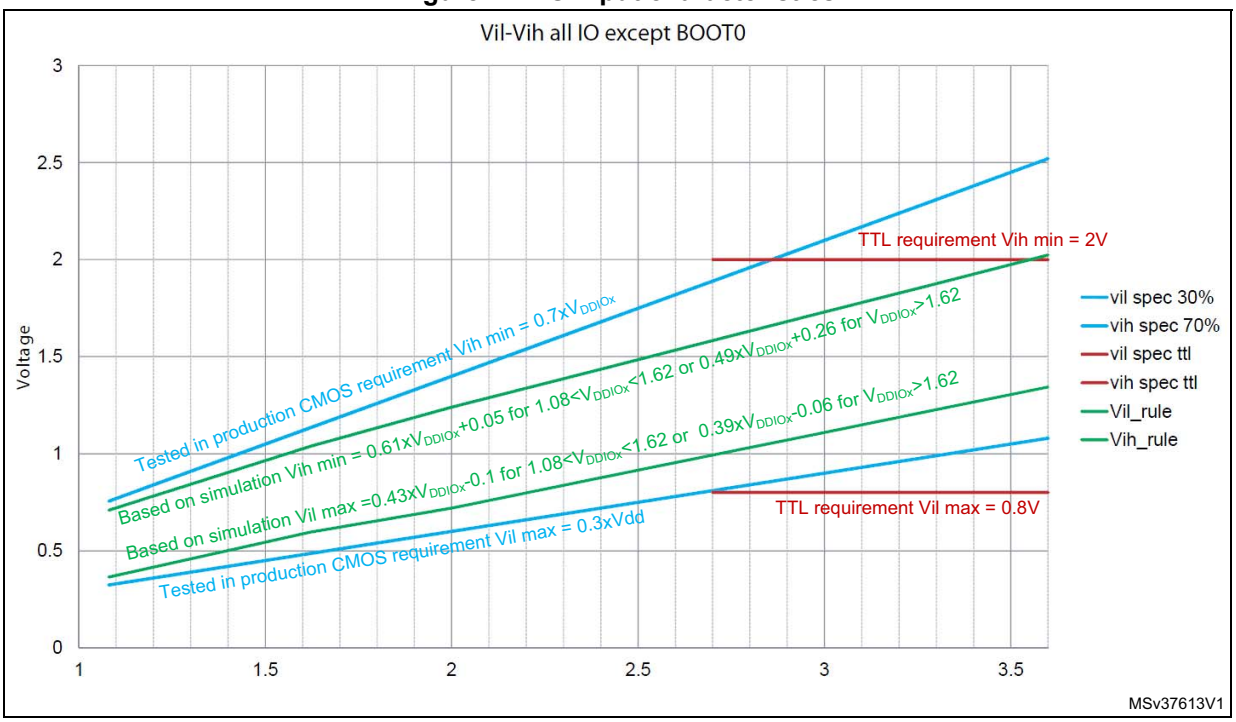
Figure 13. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 22* for 5 V tolerant I/Os.

Figure 22. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

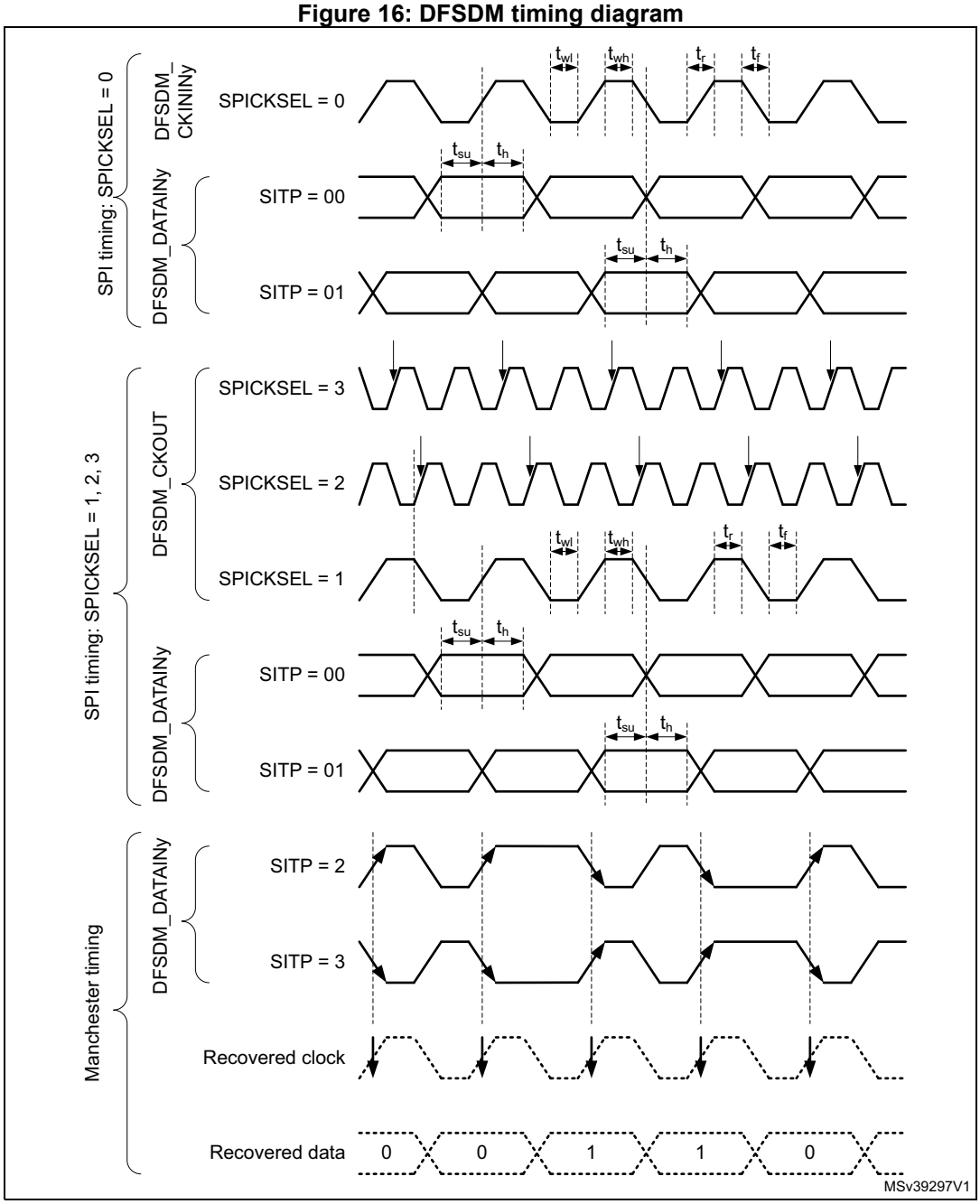
In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 19: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 19: Voltage characteristics*).

Table 66. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Figure 16: DFSDM timing diagram



6.3.26 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

6.3.27 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

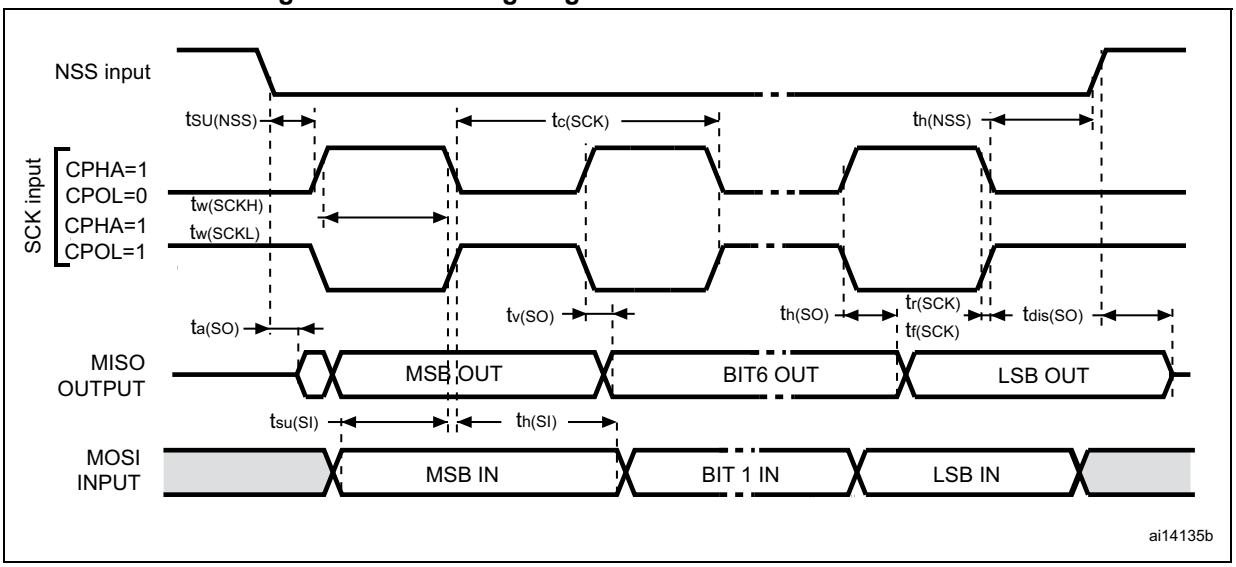
All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 82. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

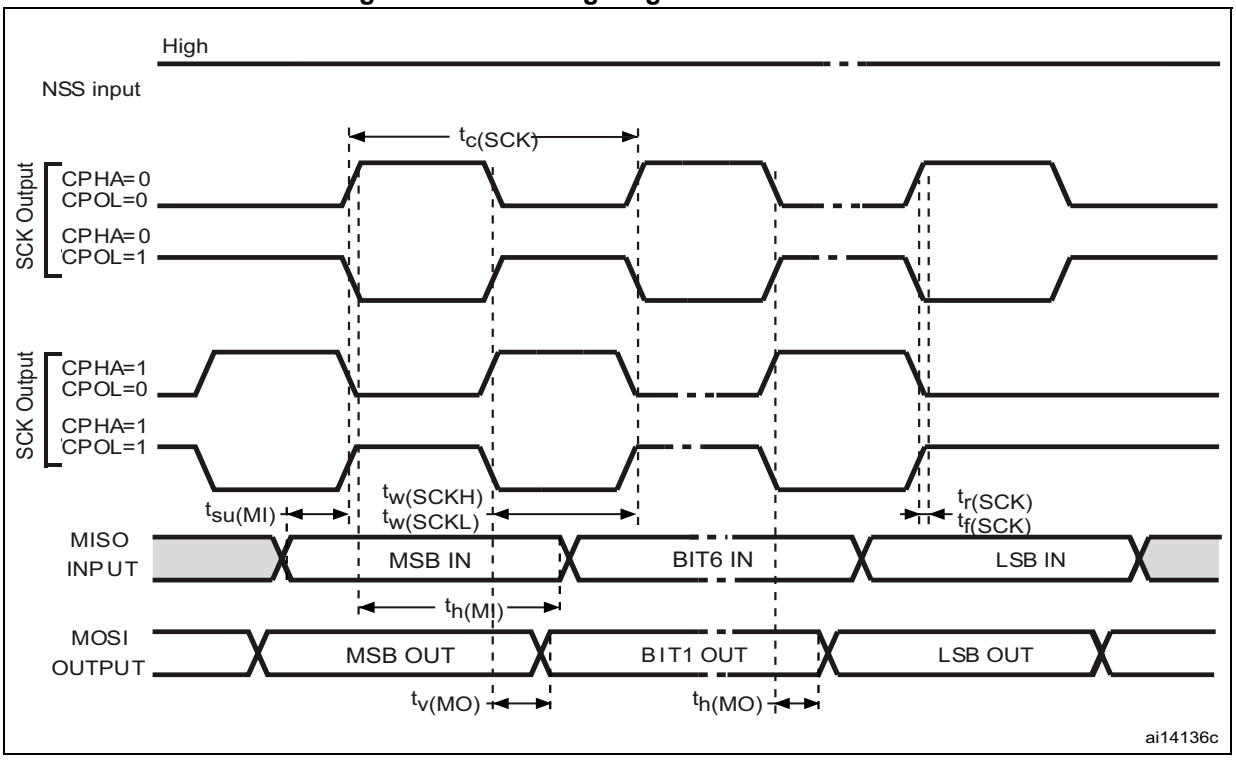
1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

6.3.28 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 90* to *Table 103* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 37 through *Figure 40* represent asynchronous waveforms and *Table 90* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

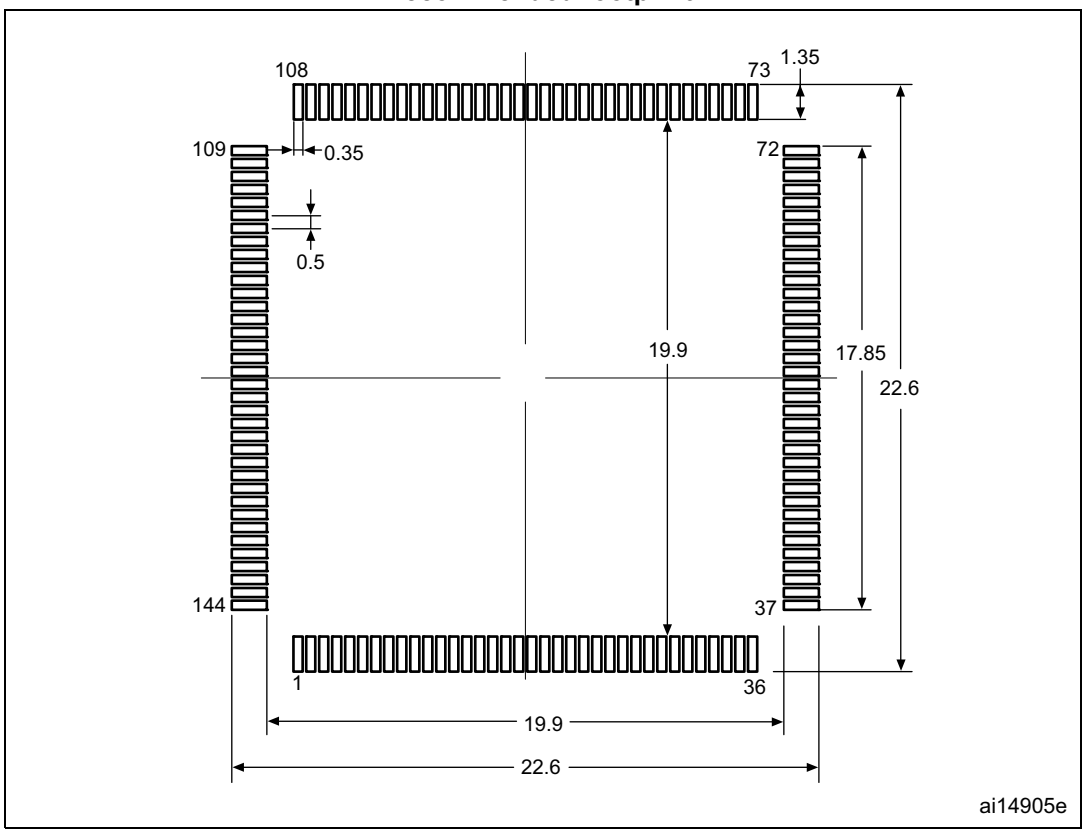
In all timing tables, the THCLK is the HCLK clock period.

Table 98. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

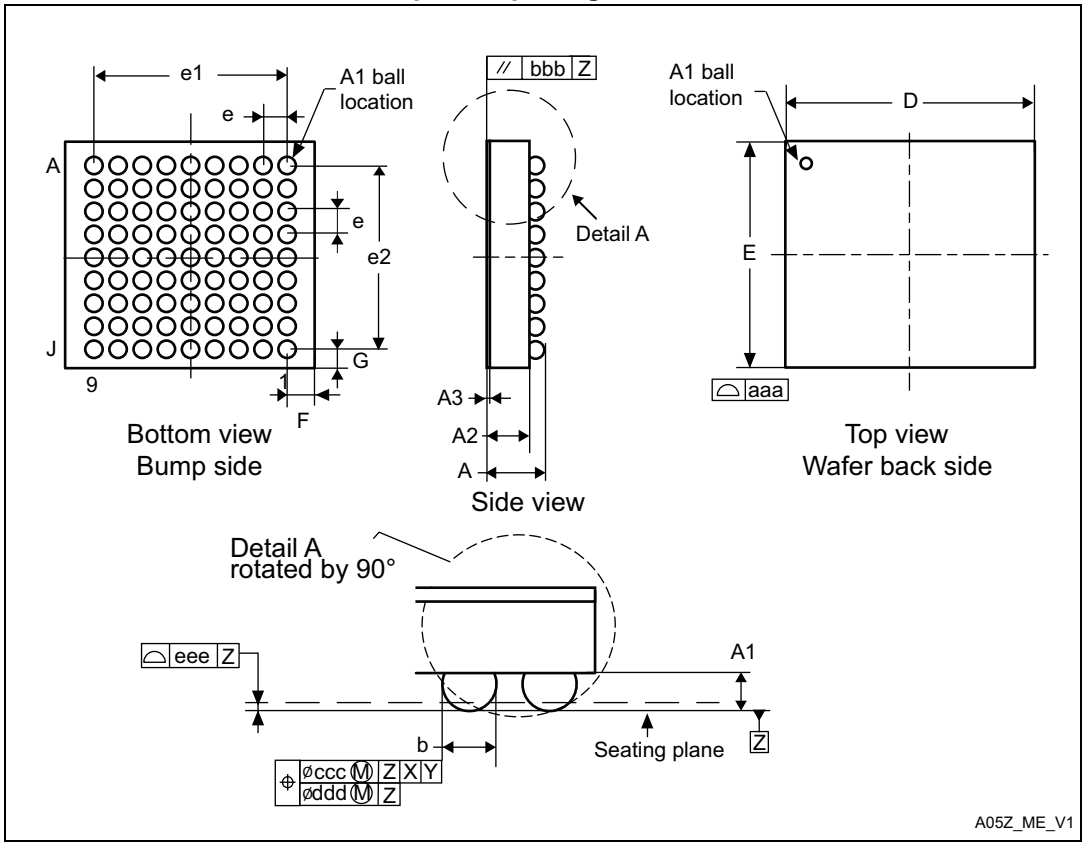
Figure 50. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.4 WLCSP81 package information

Figure 58. WLCSP81 - 81-ball, 4.4084 x 3.7594 mm, 0.4 mm pitch wafer level chip scale package outline

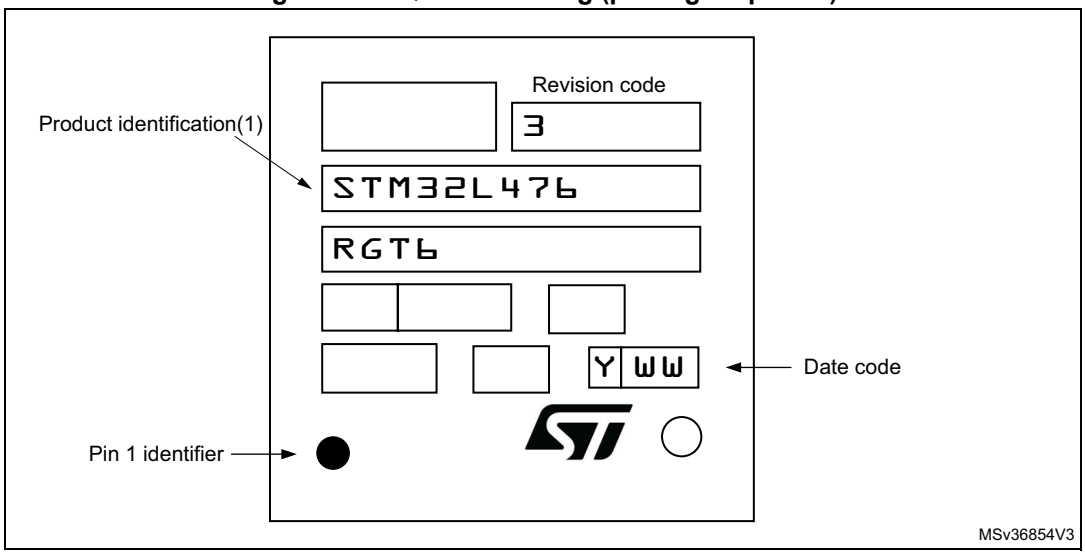


1. Drawing is not to scale.

Table 108. WLCSP81- 81-ball, 4.4084 x 3.7594 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.3734	4.4084	4.4434	0.1722	0.1736	0.1749
E	3.7244	3.7594	3.7944	0.1466	0.1480	0.1494
e	-	0.400	-	-	0.0157	-
e1	-	3.200	-	-	0.1260	-
e2	-	3.200	-	-	0.1260	-

Figure 66. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WLCSP72	46	
	Thermal resistance junction-ambient WLCSP81	41	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

Table 115. Document revision history (continued)

Date	Revision	Changes
03-Dec-2015	4	In all the document: – Stop 1 with main regulator becomes Stop 0 – Stop 1 with low-power regulator remains as Stop 1. In *Section 4: Pinouts and pin description*: – PC14/OSC32_IN becomes PC14-OSC32_IN (PC14) – PC15/OSC32_OUT becomes PC15-OSC32_OUT (PC15) – PH0/OSC_IN becomes PH0-OSC_IN (PH0) – PH1/OSC_OUT becomes PH1-OSC_OUT (PH1) – PA13 becomes PA13 (JTMS-SWDIO) – PA14 becomes PA14 (JTCK-SWCLK) – PA15 becomes PA15 (JTDI) – PB3 becomes PB3 (JTDO-TRACESWO) – PB4 becomes PB4 (NJTRST). Added *Table 12: STM32L4x6 USART/UART/LPUART features*. Added *Note 5.* Updated *Table 25: Embedded internal voltage reference*. Updated *Table 34: Current consumption in Stop 2 mode*. Updated *Table 35: Current consumption in Stop 1 mode*. Updated *Table 36: Current consumption in Stop 0 mode*. Updated *Table 37: Current consumption in Standby mode*. Updated *Table 38: Current consumption in Shutdown mode*. Updated *Table 41: Low-power mode wakeup timings*. Added *Figure 15: VREFINT versus temperature*. Updated *Figure 20: HSI16 frequency versus temperature*. Updated *Table 58: I/O static characteristics*. Updated *Table 69: DAC characteristics*. Updated *Figure 52: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline*. Updated *Table 105: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data*.