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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476rgt3

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L476xx microcontrollers.

This document should be read in conjunction with the STM32L4x6 reference manual (RM0351). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 32 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L476xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L476xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources:

3.10 Interconnect matrix

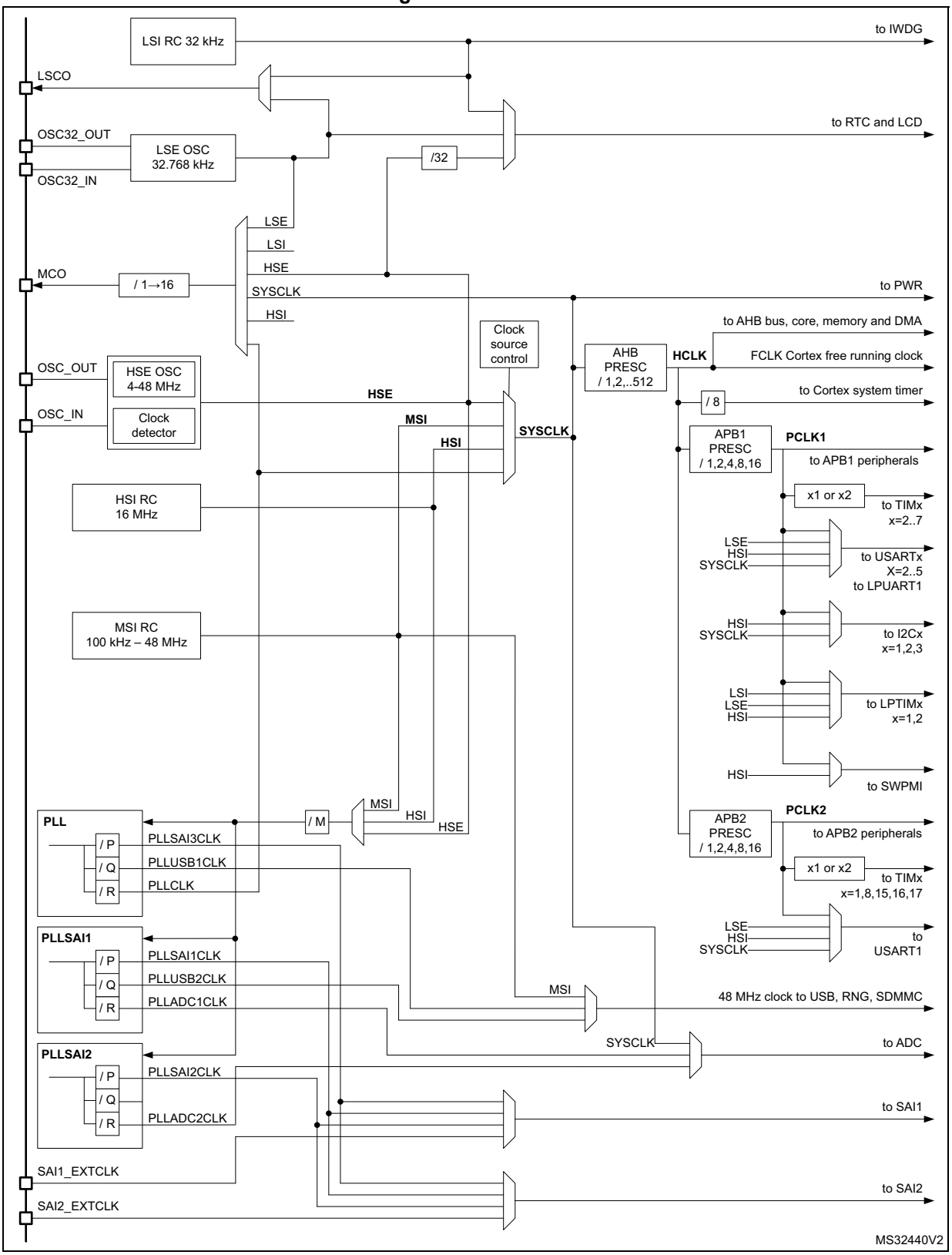
Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 6. STM32L476xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DACx DFSDM	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-

Figure 3. Clock tree



3.15 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 24 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 Internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.24.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.24.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L476 (see *Table 10* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.24.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.24.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.24.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.24.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.24.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.25 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2. The related I/O structures in *Table 15* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 15* are: FT_u, FT_lu.
4. The related I/O structures in *Table 15* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Table 15. STM32L476xxSTM32L476xx pin definitions

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	1	B2	1	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, TSC_G7_IO1, LCD_SEG38, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	-	2	A1	2	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, TSC_G7_IO2, LCD_SEG39, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	-	-	3	B1	3	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	-	4	C2	4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	-	-	5	D2	5	PE6	I/O	FT	-	TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_ TAMP3/ WKUP3
1	B9	B9	6	E2	6	VBAT	S	-	-	-	-
2	B8	B8	7	C1	7	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_ TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
3	C9	C9	8	D1	8	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	C8	C8	9	E1	9	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_ OUT
-	-	-	-	D6	10	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	-	-	D5	11	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	20	-	31	VREF-	S	-	-	-	-
12	G9	G9	-	J1	-	VSSA/VREF-	-	-	-	-	-
-	G8	G8	21	L1	32	VREF+	S	-	-	-	VREFBUF_OUT
-	H9	H9	22	M1	33	VDDA	S	-	-	-	-
13	-	-	-	-	-	VDDA/VREF+	S	-	-	-	-
14	H8	H8	23	L2	34	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, RTC_TAMP2/WKUP1
-	-	-	-	M3	-	OPAMP1_VINM	I	TT	-	-	-
15	G4	G4	24	M2	35	PA1	I/O	FT_la	-	TIM2_CH2, TIM5_CH2, USART2_RTS_DE, UART4_RX, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6
16	G6	G6	25	K3	36	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LCD_SEG1, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO
17	H7	H7	26	L3	37	PA3	I/O	TT	-	TIM2_CH4, TIM5_CH4, USART2_RX, LCD_SEG2, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC12_IN8
18	J9	J9	27	E3	38	VSS	S	-	-	-	-
19	J8	J8	28	H3	39	VDD	S	-	-	-	-
20	G5	G5	29	J4	40	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_IN9, DAC1_OUT1
21	H6	H6	30	K4	41	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC12_IN10, DAC1_OUT2
22	H5	H5	31	L4	42	PA6	I/O	FT_la	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, USART3_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port D	PD0	-	-	-	-	-	SPI2_NSS	DFSDM_DATIN7	-
	PD1	-	-	-	-	-	SPI2_SCK	DFSDM_CKIN7	-
	PD2	-	-	TIM3_ETR	-	-	-	-	USART3_RTS_ DE
	PD3	-	-	-	-	-	SPI2_MISO	DFSDM_DATIN0	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM_CKIN0	USART2_RTS_ DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	-	-	DFSDM_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	-	-	-	USART3_CTS
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS_ DE
	PD13	-	-	TIM4_CH2	-	-	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port E	PE0	-	-	-	LCD_SEG36	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	LCD_SEG37	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	LCD_SEG38	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	LCD_SEG39	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	-	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	-	-	-	-	TIM15_CH2	EVENTOUT
	PF11	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.9	mA	111	µA/MHz
				Coremark	3.1		118	
				Dhrystone 2.1	3.1		119	
				Fibonacci	2.9		112	
				While(1)	2.8		108	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.2	mA	127	µA/MHz
				Coremark	10.9		136	
				Dhrystone 2.1	11.0		137	
				Fibonacci	10.5		131	
				While(1)	9.9		124	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	272	µA	136	µA/MHz
				Coremark	291		145	
				Dhrystone 2.1	302		151	
				Fibonacci	269		135	
				While(1)	269		135	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 40*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 19: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 40*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 40. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	4.5	3.7	4.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC AHB clock domain	5.5	4.7	5.5	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	FMC	8.9	7.5	8.4	
	GPIOA(2)	4.8	3.8	4.4	
	GPIOB(2)	4.8	4.0	4.6	
	GPIOC(2)	4.5	3.8	4.3	
	GPIOD(2)	4.6	3.9	4.4	
	GPIOE(2)	5.2	4.5	4.9	
	GPIOF(2)	5.9	4.9	5.7	
	GPIOG(2)	4.3	3.8	4.2	
	GPIOH(2)	0.7	0.6	0.8	
	OTG_FS independent clock domain	23.2	NA	NA	
	OTG_FS AHB clock domain	16.4	NA	NA	
	QUADSPI	7.8	6.7	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG AHB clock domain	0.6	NA	NA	
	SRAM1	0.9	0.8	0.9	

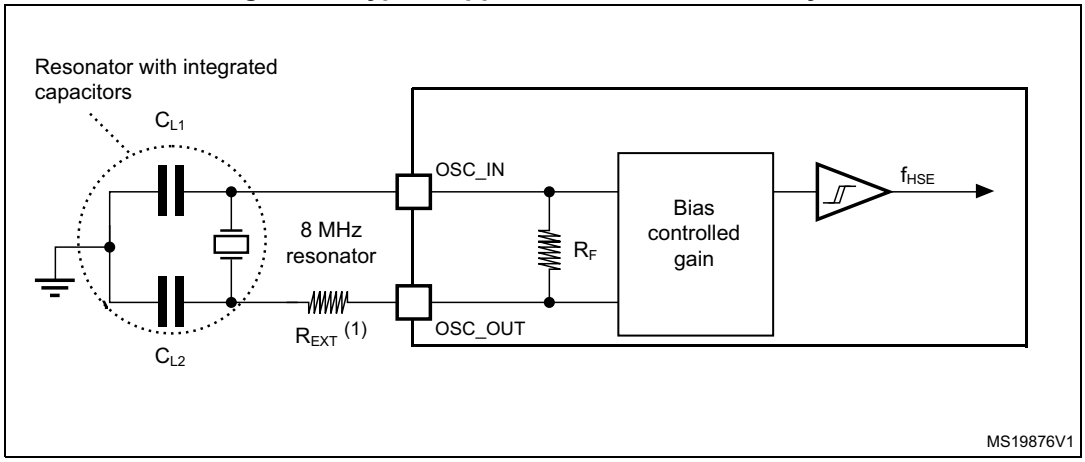
Table 41. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.2	10.2	µs
			Wakeup clock HSI16 = 16 MHz	6.3	8.99	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	10.46	
			Wakeup clock HSI16 = 16 MHz	6.3	8.87	
			Wakeup clock MSI = 4 MHz	8.0	13.23	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	4.5	5.78	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.0	6.5	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
			Wakeup clock MSI = 4 MHz	8.2	13.5	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	12.7	20	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			10.7	21.5	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.0	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
		Range 2	Wakeup clock MSI = 24 MHz	8.2	9.9	
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
			Wakeup clock MSI = 4 MHz	10.6	15.8	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.1	6.7	
			Wakeup clock HSI16 = 16 MHz	5.7	8	
		Range 2	Wakeup clock MSI = 24 MHz	5.5	6.65	
			Wakeup clock HSI16 = 16 MHz	5.7	7.53	
			Wakeup clock MSI = 4 MHz	8.2	16.6	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	20.8	µs
			Wakeup clock MSI = 4 MHz	20.1	35.5	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	24.3	µs
			Wakeup clock MSI = 4 MHz	20.1	38.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	256	330.6	µs

1. Guaranteed by characterization results.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Table 65. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 86. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 ≤ V_{DD} ≤ 3.6	-	22	ns
		Slave transmitter (after enable edge) 1.71 ≤ V_{DD} ≤ 3.6	-	34	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 ≤ V_{DD} ≤ 3.6	-	27	ns
		Master transmitter (after enable edge) 1.71 ≤ V_{DD} ≤ 3.6	-	40	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 33. SAI master timing waveforms

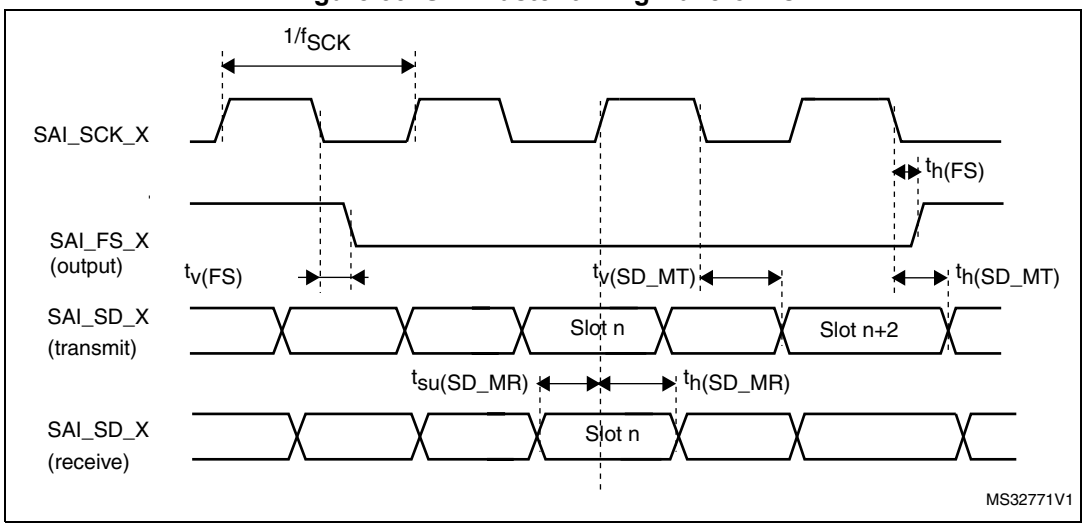
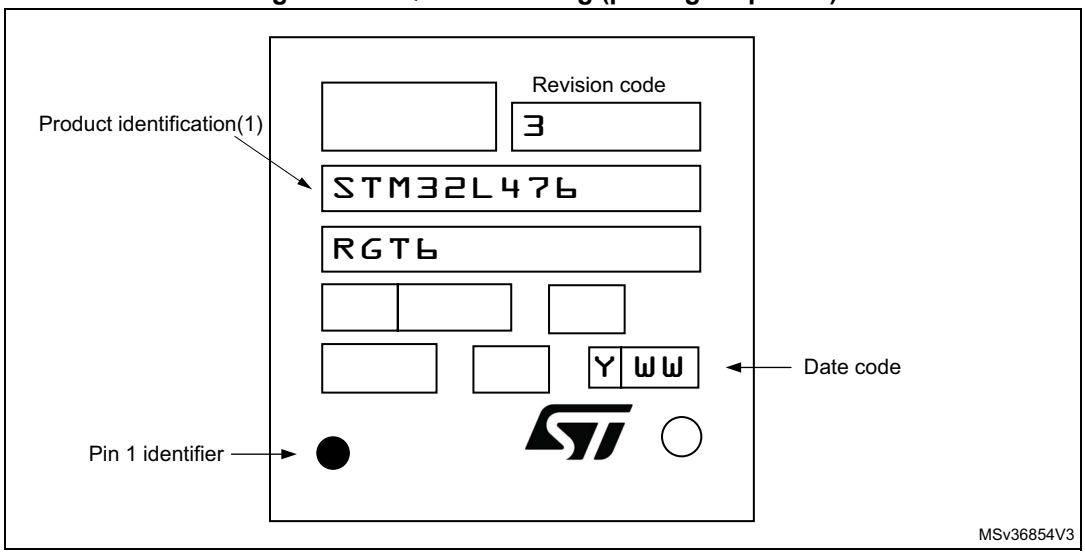


Figure 66. LQFP64 marking (package top view)



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