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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476rgt6

Table 2. STM32L476xx family device features and peripheral counts (continued)

Peripheral	STM32L476 Zx	STM32L476 Qx	STM32L476 Vx	STM32L476 Mx	STM32L476 Jx	STM32L476 Rx
Max. CPU frequency	80 MHz					
Operating voltage	1.71 to 3.6 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C					
Packages	LQFP144	UFBGA132	LQFP100	WLCSP81	WLCSP72	LQFP64

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L476xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L476xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

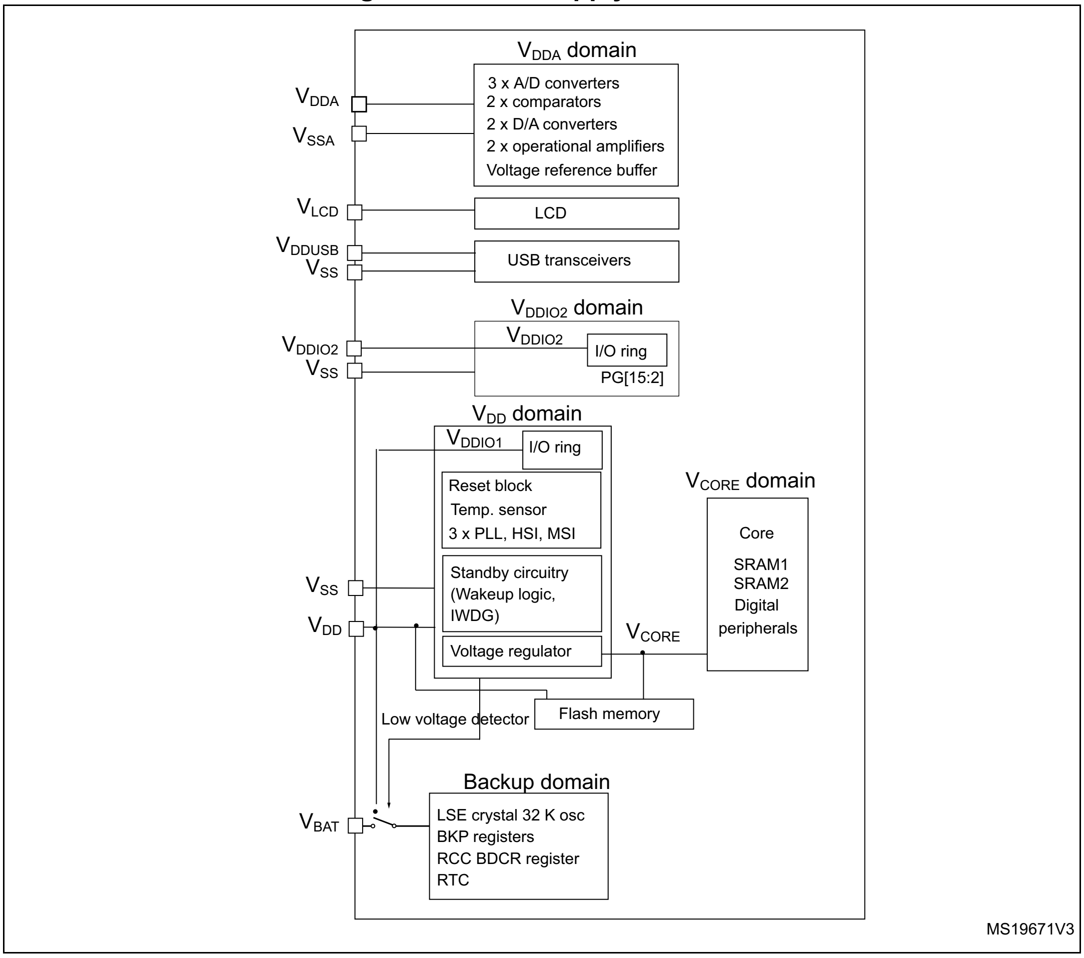
3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.19 Operational amplifier (OPAMP)

The STM32L476xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

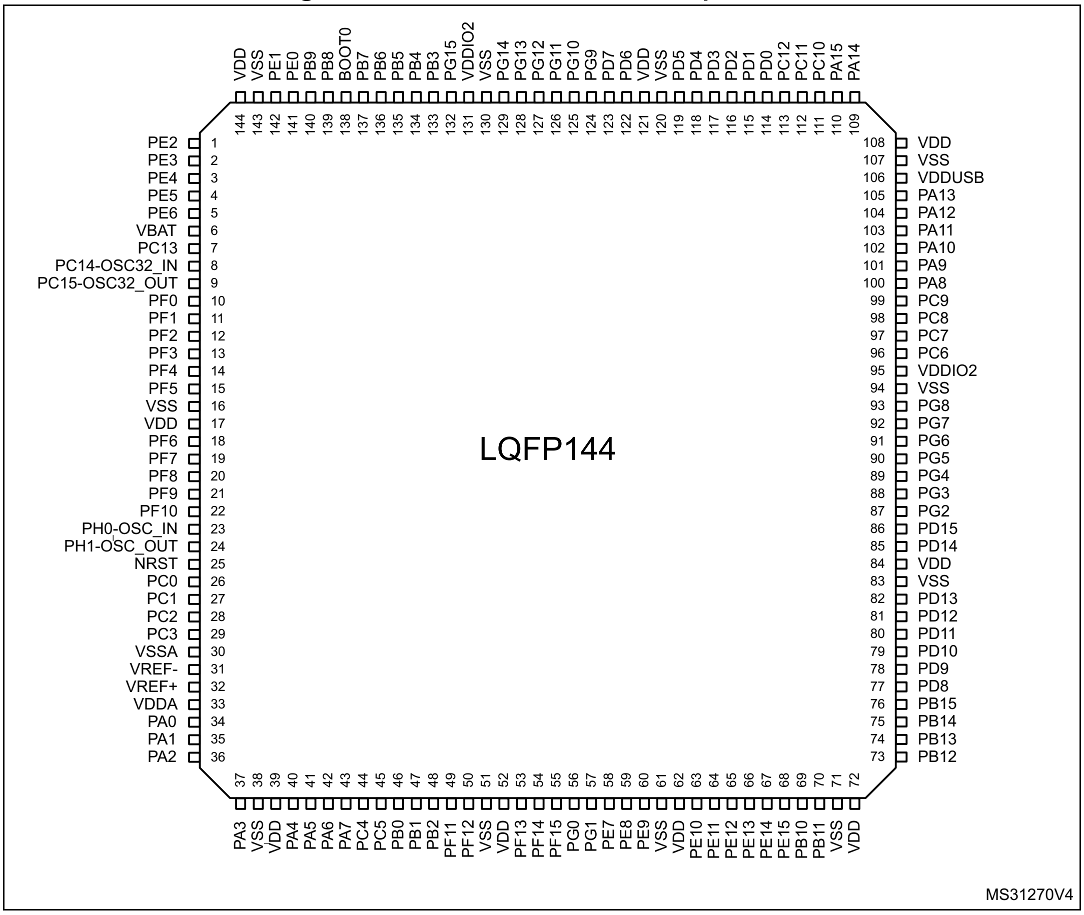
The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

4 Pinouts and pin description

Figure 4. STM32L476Zx LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
37	F3	F3	63	E12	96	PC6	I/O	FT_l	-	TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, TSC_G4_IO1, LCD_SEG24, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
38	F1	F1	64	E11	97	PC7	I/O	FT_l	-	TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, TSC_G4_IO2, LCD_SEG25, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
39	F2	F2	65	E10	98	PC8	I/O	FT_l	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, LCD_SEG26, SDMMC1_D0, EVENTOUT	-
40	E1	E1	66	D12	99	PC9	I/O	FT_l	-	TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, OTG_FS_NOE, LCD_SEG27, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT	-
41	E2	E2	67	D11	100	PA8	I/O	FT_l	-	MCO, TIM1_CH1, USART1_CK, OTG_FS_SOF, LCD_COM0, LPTIM2_OUT, EVENTOUT	-
42	E3	E3	68	D10	101	PA9	I/O	FT_lu	-	TIM1_CH2, USART1_TX, LCD_COM1, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
43	D2	D2	69	C12	102	PA10	I/O	FT_lu	-	TIM1_CH3, USART1_RX, OTG_FS_ID, LCD_COM2, TIM17_BKIN, EVENTOUT	-
44	D1	D1	70	B12	103	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, USART1_CTS, CAN1_RX, OTG_FS_DM, TIM1_BKIN2_COMP1, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
59	A7	A7	93	B4	137	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, DFSDM_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, LCD_SEG21, FMC_NL, TIM8_BKIN_COMP1, TIM17_CH1N, EVENTOUT	COMP2_ INM, PVD_IN
60	D7	D7	94	A4	138	BOOT0	I	-	-	-	-
61	E7	E7	95	A3	139	PB8	I/O	FT_fl	-	TIM4_CH3, I2C1_SCL, DFSDM_DATIN6, CAN1_RX, LCD_SEG16, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
62	E8	E8	96	B3	140	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM_CKIN6, CAN1_TX, LCD_COM3, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	-	97	C3	141	PE0	I/O	FT_l	-	TIM4_ETR, LCD_SEG36, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	-	98	A2	142	PE1	I/O	FT_l	-	LCD_SEG37, FMC_NBL1, TIM17_CH1, EVENTOUT	-
63	A8	A8	99	D3	143	VSS	S	-	-	-	-
64	A9	A9	100	C4	144	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0351 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	μs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)(2)	BOR(3) (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	3.1	mA	119	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.8		111	
				Fibonacci	2.7		104	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.0	mA	125	µA/MHz
				Coremark	9.4		117	
				Dhrystone 2.1	9.1		114	
				Fibonacci	9.0		112	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code(1)	358	µA	179	µA/MHz
				Coremark	392		196	
				Dhrystone 2.1	390		195	
				Fibonacci	385		192	
				While(1)	385		192	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.9	mA	111	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.9		111	
				Fibonacci	2.6		100	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.2	mA	127	µA/MHz
				Coremark	10.4		130	
				Dhrystone 2.1	10.3		129	
				Fibonacci	9.6		120	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code(1)	242	µA	121	µA/MHz
				Coremark	242		121	
				Dhrystone 2.1	242		121	
				Fibonacci	225		112	
				While(1)	242		121	

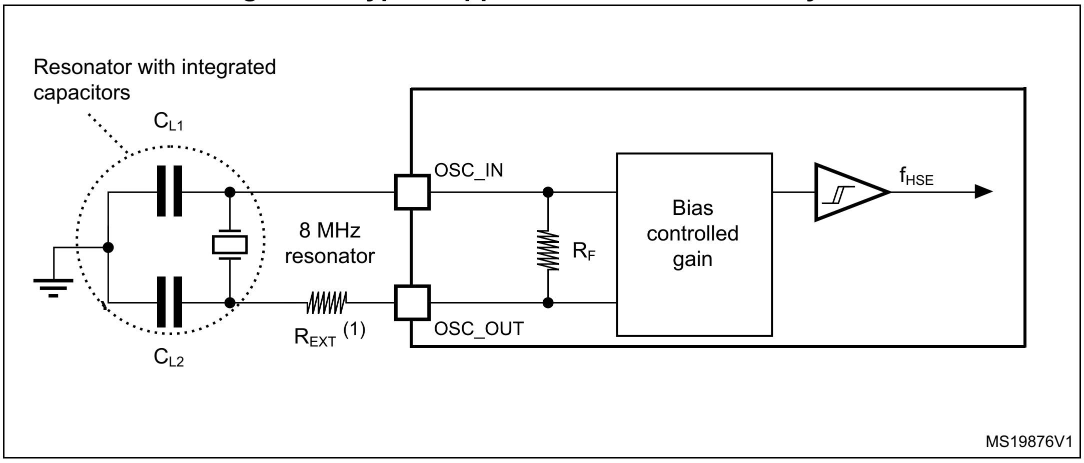
1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 40. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	SRAM2	1.6	1.4	1.6	µA/MHz
	TSC	1.8	1.4	1.6	
	All AHB Peripherals	118.5	77.3	87.6	
APB1	AHB to APB1 bridge[(3)]	0.9	0.7	0.9	µA/MHz
	CAN1	4.6	4.0	4.4	
	DAC1	2.4	1.9	2.2	
	I2C1 independent clock domain	3.7	3.1	3.2	
	I2C1 APB clock domain	1.3	1.1	1.5	
	I2C2 independent clock domain	3.7	3.0	3.2	
	I2C2 APB clock domain	1.4	1.1	1.5	
	I2C3 independent clock domain	2.9	2.3	2.5	
	I2C3 APB clock domain	0.9	0.9	1.1	
	LCD	1.0	0.8	0.9	
	LPUART1 independent clock domain	2.1	1.6	2.0	
	LPUART1 APB clock domain	0.6	0.6	0.6	
	LPTIM1 independent clock domain	3.3	2.6	2.9	
	LPTIM1 APB clock domain	0.9	0.8	1.0	
	LPTIM2 independent clock domain	3.1	2.7	2.9	
	LPTIM2 APB clock domain	0.8	0.6	0.7	
	OPAMP	0.4	0.4	0.3	
	PWR	0.5	0.5	0.4	
	SPI2	1.8	1.6	1.6	
	SPI3	2.1	1.7	1.8	
	SWPMI1 independent clock domain	2.3	1.8	2.2	
	SWPMI1 APB clock domain	1.1	1.1	1.0	
	TIM2	6.8	5.7	6.3	
	TIM3	5.4	4.6	5.0	
	TIM4	5.2	4.4	4.9	
	TIM5	6.5	5.5	6.1	
	TIM6	1.1	1.0	1.0	
	TIM7	1.1	0.9	1.0	

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

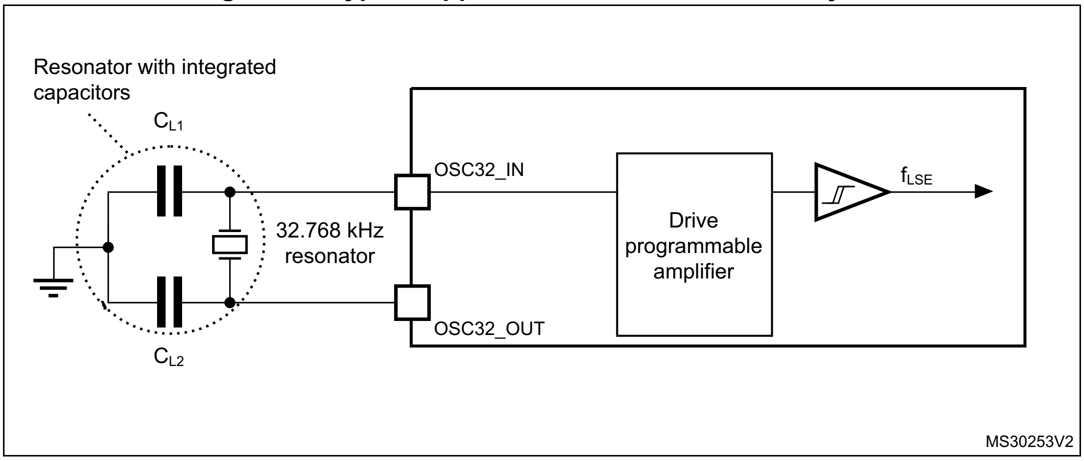
Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.10 Flash memory characteristics

Table 51. Flash memory characteristics[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 52. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 71. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. To well control inrush current of VREFBUF during start-up phase and scaling change, V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 0.

6.3.22 Temperature sensor characteristics

Table 74. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[(1)]	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope[(2)]	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)[(3)]	0.742	0.76	0.785	V
t_{START} (TS_BUF)[(1)]	Sensor Buffer Start-up time in continuous mode[(4)]	-	8	15	µs
t_{START}[(1)]	Start-up time when entering in continuous mode[(4)]	-	70	120	µs
t_{S_temp}[(1)]	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)[(1)]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.23 V_{BAT} monitoring characteristics

Table 75. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[(1)]	Error on Q	-10	-	10	%
t_{S_vbat}[(1)]	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 76. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

Figure 42. Synchronous multiplexed PSRAM write timings

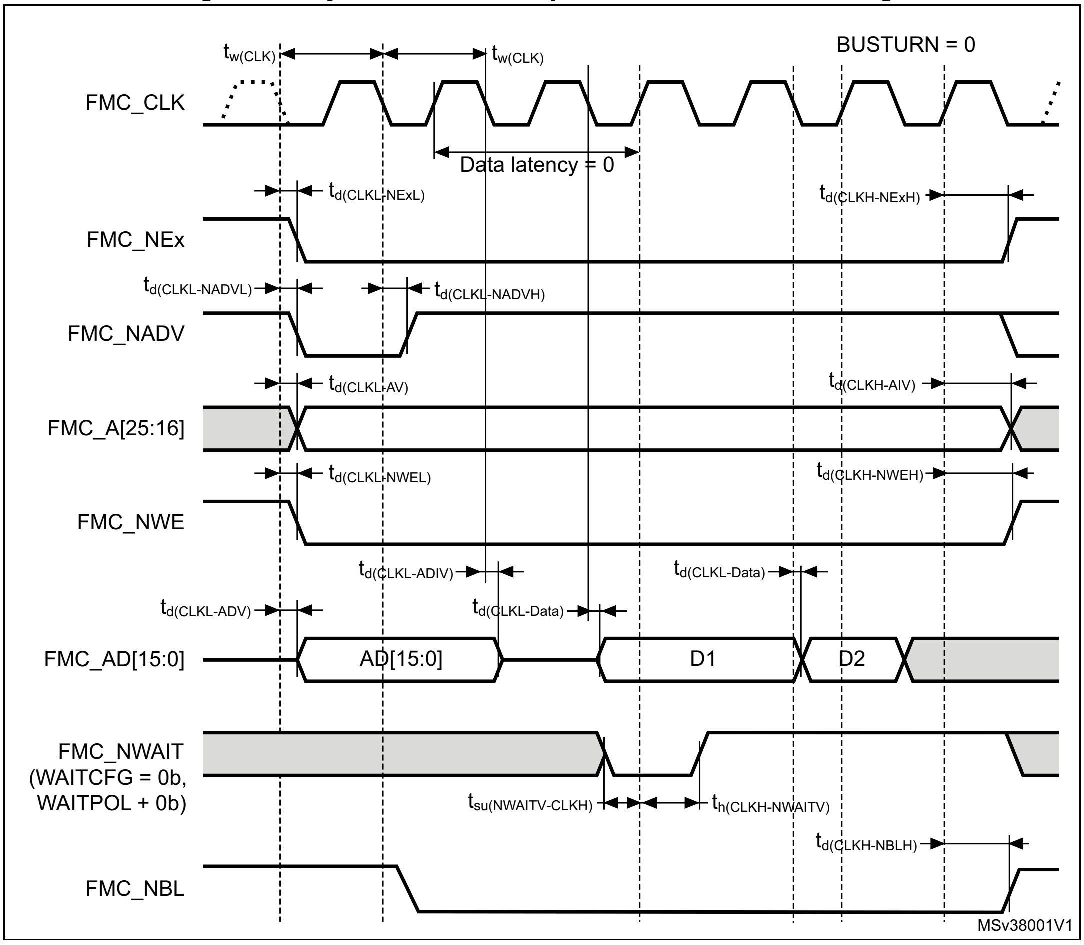


Figure 43. Synchronous non-multiplexed NOR/PSRAM read timings

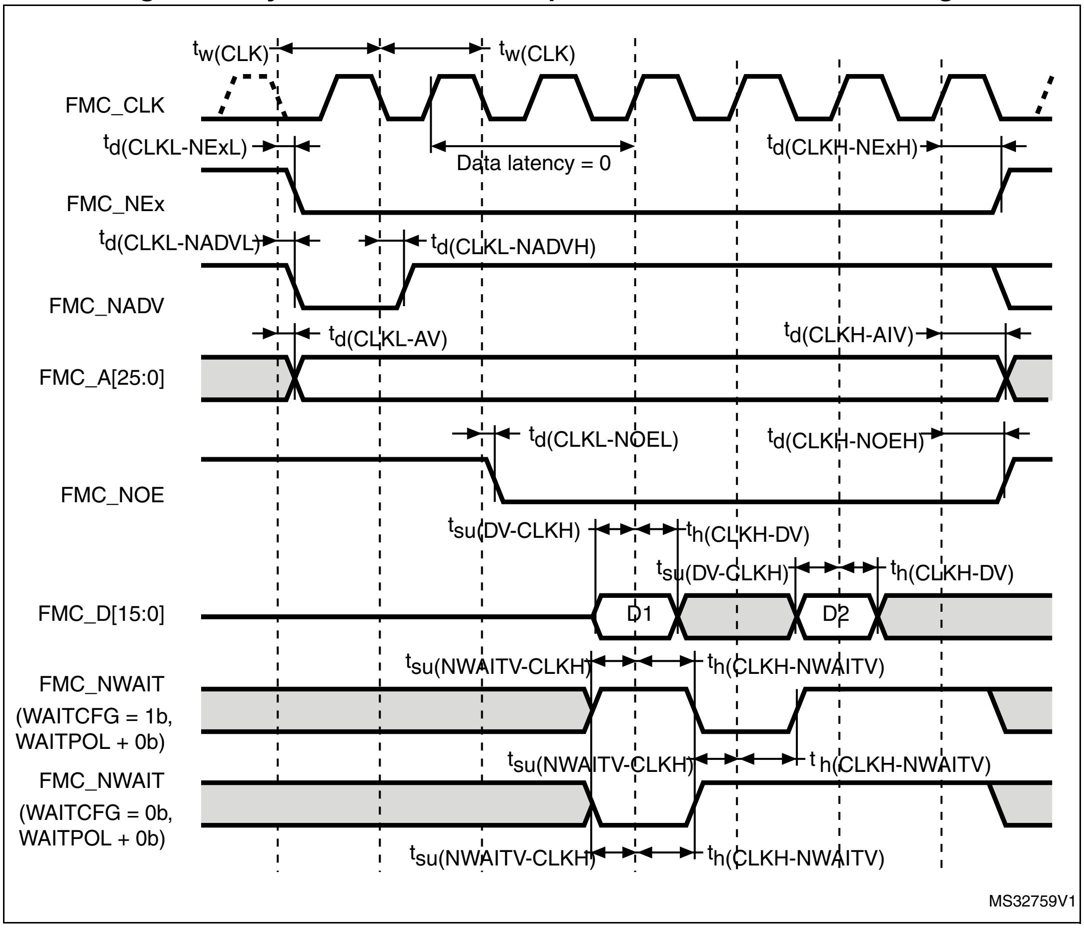


Table 100. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}-0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}-0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	