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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476vct6

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	-	M4	-	OPAMP2_VINM	I	TT	-	-	-
23	H4	H4	32	J5	43	PA7	I/O	FT_la	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
24	J7	J7	33	K5	44	PC4	I/O	FT_la	-	USART3_TX, LCD_SEG22, EVENTOUT	COMP1_INM, ADC12_IN13
25	J6	J6	34	L5	45	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
26	J5	J5	35	M5	46	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, EVENTOUT	OPAMP2_VOUT, ADC12_IN15
27	J4	J4	36	M6	47	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN0, USART3_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	J3	J3	37	L6	48	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM_CKIN0, EVENTOUT	COMP1_INP
-	-	-	-	K6	49	PF11	I/O	FT	-	EVENTOUT	-
-	-	-	-	J7	50	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	52	VDD	S	-	-	-	-
-	-	-	-	K7	53	PF13	I/O	FT	-	DFSDM_DATIN6, FMC_A7, EVENTOUT	-
-	-	-	-	J8	54	PF14	I/O	FT	-	DFSDM_CKIN6, TSC_G8_IO1, FMC_A8, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	82	B9	115	PD1	I/O	FT	-	SPI2_SCK, DFSDM_CKIN7, CAN1_TX, FMC_D3, EVENTOUT	-
54	A3	A3	83	C8	116	PD2	I/O	FT_l	-	TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, LCD_COM7/LCD_SEG31/ LCD_SEG43, SDMMC1_CMD, EVENTOUT	-
-	-	-	84	B8	117	PD3	I/O	FT	-	SPI2_MISO, DFSDM_DATIN0, USART2_CTS, FMC_CLK, EVENTOUT	-
-	-	E5	85	B7	118	PD4	I/O	FT	-	SPI2_MOSI, DFSDM_CKIN0, USART2_RTS_DE, FMC_NOE, EVENTOUT	-
-	-	D4	86	A6	119	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	-	-	-	120	VSS	S	-	-	-	-
-	-	E4	-	-	121	VDD	S	-	-	-	-
-	-	D5	87	B6	122	PD6	I/O	FT	-	DFSDM_DATIN1, USART2_RX, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	-	D6	88	A5	123	PD7	I/O	FT	-	DFSDM_CKIN1, USART2_CK, FMC_NE1, EVENTOUT	-
-	A4	A4	-	D9	124	PG9	I/O	FT_s	-	SPI3_SCK, USART1_TX, FMC_NCE3/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	B4	B4	-	D8	125	PG10	I/O	FT_s	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	C4	C4	-	G3	126	PG11	I/O	FT_s	-	LPTIM1_IN2, SPI3_MOSI, USART1_CTS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	C5	C5	-	D7	127	PG12	I/O	FT_s	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	B5	B5	-	C7	128	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, FMC_A24, EVENTOUT	-
-	A5	A5	-	C6	129	PG14	I/O	FT_fs	-	I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	-	-	F7	130	VSS	S	-	-	-	-
-	B6	B6	-	G7	131	VDDIO2	S	-	-	-	-
-	-	-	-	K1	132	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, EVENTOUT	-
55	A6	A6	89	A8	133	PB3 (JTDO-TRACESWO)	I/O	FT_la	(3)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, EVENTOUT	COMP2_INM
56	C6	C6	90	A7	134	PB4 (NJTRST)	I/O	FT_la	(3)	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS_DE, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP
57	C7	C7	91	C5	135	PB5	I/O	FT_la	-	LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
58	B7	B7	92	B5	136	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, DFSDM_DATIN5, USART1_TX, TSC_G2_IO3, TIM8_BKIN2_COMP2, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP

2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 20. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(4)	
	Injected current on PA4, PA5	-5/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	80	
f_{PCLK2}	Internal APB2 clock frequency	-		0	80	
V_{DD}	Standard operating voltage	-		1.71 (1)	3.6	V
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used		1.08	3.6	V
		PG[15:2] not used		0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used		1.62	3.6	V
		DAC or OPAMP used		1.8		
		VREFBUF used		2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used		0		
V_{BAT}	Backup operating voltage	-		1.55	3.6	V
V_{DDUSB}	USB supply voltage	USB used		3.0	3.6	V
		USB not used		0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O		-0.3	V_{DDIOx}+0.3	V
		BOOT0		0	9	
		All I/O except BOOT0 and TT_xx		-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		LQFP64	-	-	444	
		UFBGA132	-	-	363	
		WLCSP81	-	-	487	
		WLCSP72	-	-	434	
P_D	Power dissipation at T_A = 125 °C for suffix 3(4)	LQFP144	-	-	156	mW
		LQFP100	-	-	119	
		LQFP64	-	-	111	
		UFBGA132	-	-	90	
		WLCSP81	-	-	121	
		WLCSP72	-	-	108	

Table 33. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	81	110	217	395	754	115	182	375	750	1500	µA
				1 MHz	50	78	185	362	720	80	149	342	717	1456	
				400 kHz	28	57	163	340	698	60	122	314	689	1429	
				100 kHz	18	47	155	332	686	50	114	313	688	1438	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled	1.8 V	1.14	3.77	14.7	34.7	77	2.7	9	37	87	193	µA
			2.4 V	1.15	3.86	15	35.5	79.1	2.7	10	38	89	198	
			3 V	1.18	3.97	15.4	36.4	81.3	2.8	10	39	91	203	
			3.6 V	1.26	4.11	16	38	85.1	3.0	10	40	95(2)	213	
		LCD enabled(3) clocked by LSI	1.8 V	1.43	3.98	15	35	77.3	3.2	10	38	88	193	
			2.4 V	1.49	4.07	15.3	35.8	79.4	3.2	10	38	90	199	
			3 V	1.54	4.24	15.7	36.7	81.6	3.3	11	39	92	204	
			3.6 V	1.75	4.47	16.1	38.3	85.4	3.5	11	40	96	214	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 58: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 40: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 42. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

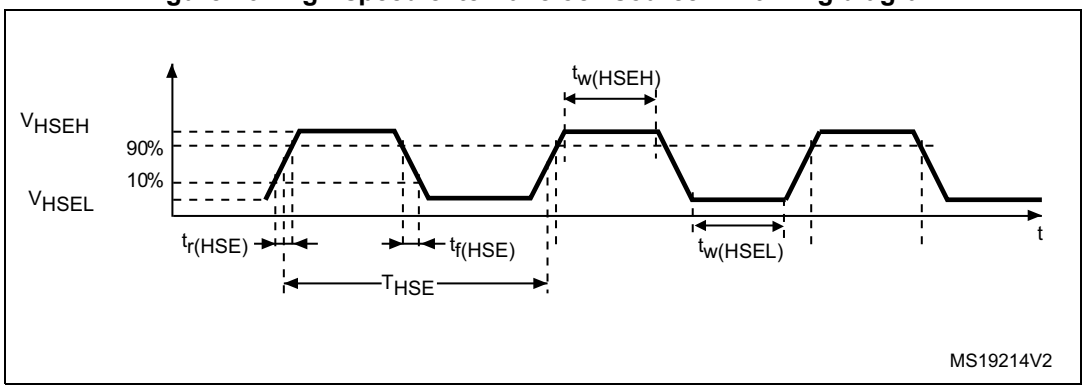
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16: High-speed external clock source AC timing diagram*.

Table 43. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 16. High-speed external clock source AC timing diagram



Multi-speed internal (MSI) RC oscillator

Table 48. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	99	100	101	kHz
			Range 1	198	200	202	
			Range 2	396	400	404	
			Range 3	792	800	808	
			Range 4	0.99	1	1.01	MHz
			Range 5	1.98	2	2.02	
			Range 6	3.96	4	4.04	
			Range 7	7.92	8	8.08	
			Range 8	15.8	16	16.16	
			Range 9	23.8	24	24.4	
			Range 10	31.7	32	32.32	
			Range 11	47.5	48	48.48	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 58. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL} (1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.3xV_{DDIOx} (2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.39xV_{DDIOx}-0.06 (3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	0.43xV_{DDIOx}-0.1 (3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	0.17xV_{DDIOx} (3)	
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	

Table 58. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	FT_xx input leakage current(3)	$V_{IN} \le Max(V_{DDXXX})$(4)	-	-	±100	nA
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)(5)	-	-	650(3)(6)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u and PC3 IO	$V_{IN} \le Max(V_{DDXXX})$ (4)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)	-	-	2500(3)(7)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN}$ < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	T_J = 75 °C	-	-	1	
R_{PU}	Weak pull-up equivalent resistor (8)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 22: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 64. Maximum ADC RAIN(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000

Table 69. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{network}$	R2/R1 internal resistance values in PGA mode(5)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
$I_{DDA}(OPAMP)$(3)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA
		Low-power mode		-	45	100	

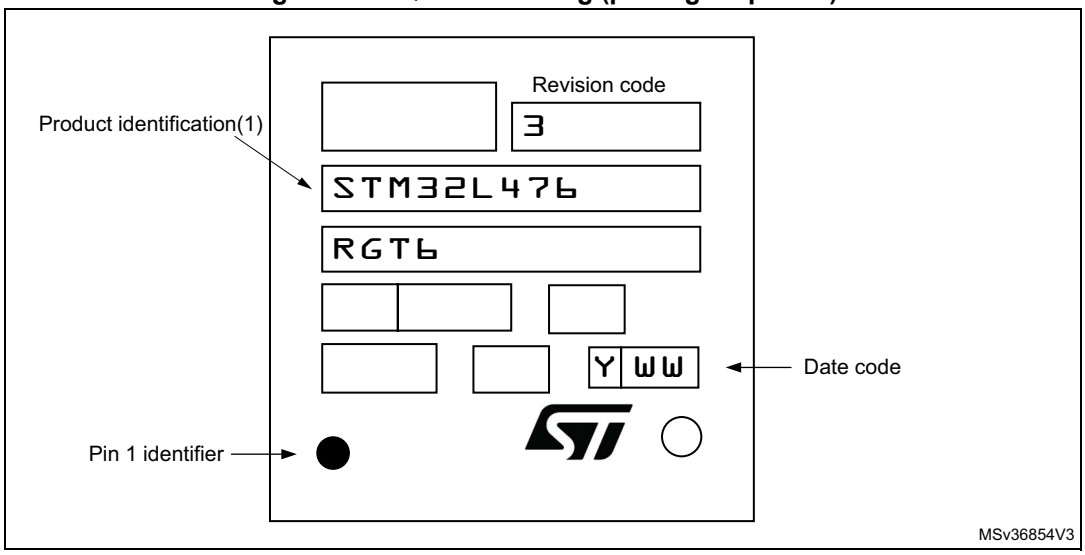
1. Guaranteed by design, unless otherwise specified.
2. The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V
3. Guaranteed by characterization results.
4. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in *Table 58: I/O static characteristics*.
5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

Table 99. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	5.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2.5	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 66. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WLCSP72	46	
	Thermal resistance junction-ambient WLCSP81	41	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L476xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 113* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Part numbering*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW