STMicroelectronics - STM32L476VGT3 Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476vgt3

2 Description

The STM32L476xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L476xx devices embed high-speed memories (Flash memory up to 1 Mbyte, up to 128 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L476xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces.

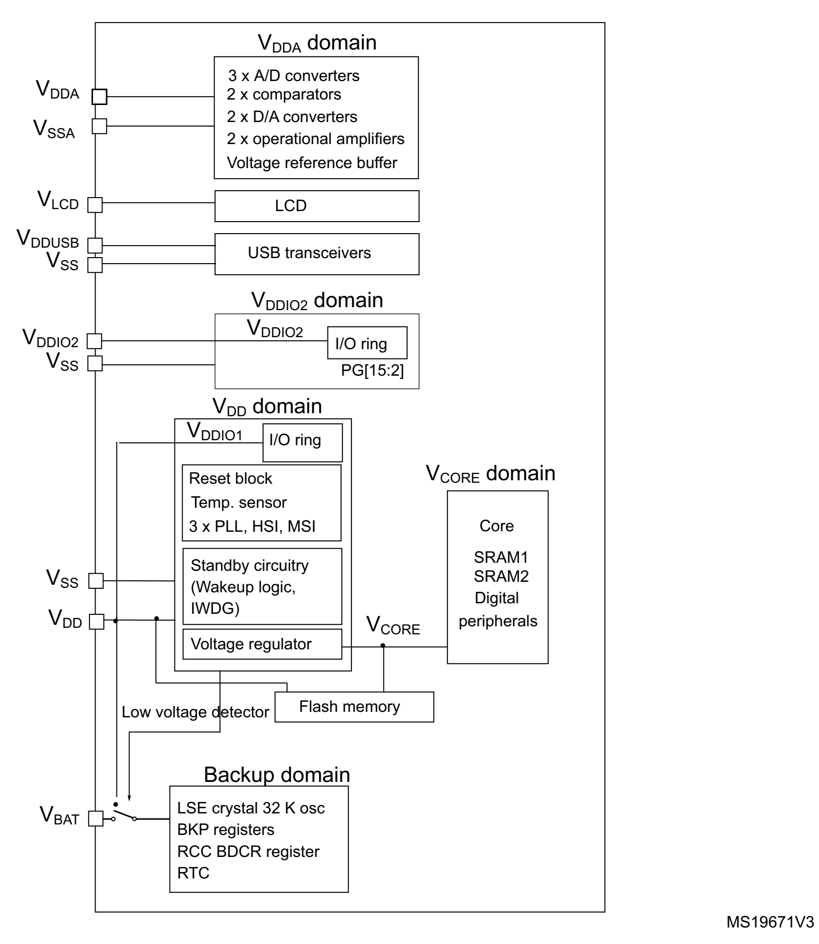
- Three I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB OTG full-speed
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L476xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, 3.3 V dedicated supply input for USB and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers.

The STM32L476xx family offers six packages from 64-pin to 144-pin packages.

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

Table 4. STM32L476 modes overview (continued)

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)(10) BOR, RTC, IWDG	0.35 µA w/o RTC 0.65 µA w/ RTC	14 µs
	OFF			Powered Off				0.12 µA w/o RTC 0.42 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down(11)	Reset pin 5 I/Os (WKUPx)(10) RTC	0.03 µA w/o RTC 0.33 µA w/ RTC	256 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. The SRAM1 and SRAM2 clocks can be gated on or off independently.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. OTG_FS wakeup by resume from suspend and attach detection protocol event.
9. SWPMI1 wakeup by resume from suspend.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Table 13. SAI implementation

SAI features[1]	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.31 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.32 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	-	J9	55	PF15	I/O	FT	-	TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	-	-	H9	56	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	G9	57	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	-	E6	38	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	-	F6	39	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	-	-	40	M8	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	-	-	F6	61	VSS	S	-	-	-	-
-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	63	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	-	-	42	M9	64	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT	-
-	-	-	43	L9	65	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	-	-	44	M10	66	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	**CAN1, TSC**	**OTG_FS, QUADSPI**	**LCD**	**SDMMC1, COMP1, COMP2, FMC, SWPMI1**	**SAI1, SAI2**	**TIM2, TIM15, TIM16, TIM17, LPTIM2**	**EVENTOUT**
Port C	PC0	LPUART1_RX	-	-	LCD_SEG18	-	-	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	-	LCD_SEG19	-	-	-	EVENTOUT
	PC2	-	-	-	LCD_SEG20	-	-	-	EVENTOUT
	PC3	-	-	-	LCD_VLCD	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	-	LCD_SEG22	-	-	-	EVENTOUT
	PC5	-	-	-	LCD_SEG23	-	-	-	EVENTOUT
	PC6	-	TSC_G4_IO1	-	LCD_SEG24	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	-	TSC_G4_IO2	-	LCD_SEG25	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	-	LCD_SEG26	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	LCD_SEG27	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2_COMP1	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	-	LCD_COM4/ LCD_SEG28/ LCD_SEG40	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	-	LCD_COM5/ LCD_SEG29/ LCD_SEG41	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	-	LCD_COM6/ LCD_SEG30/ LCD_SEG42	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

5 Memory mapping

Figure 10. STM32L476 memory map

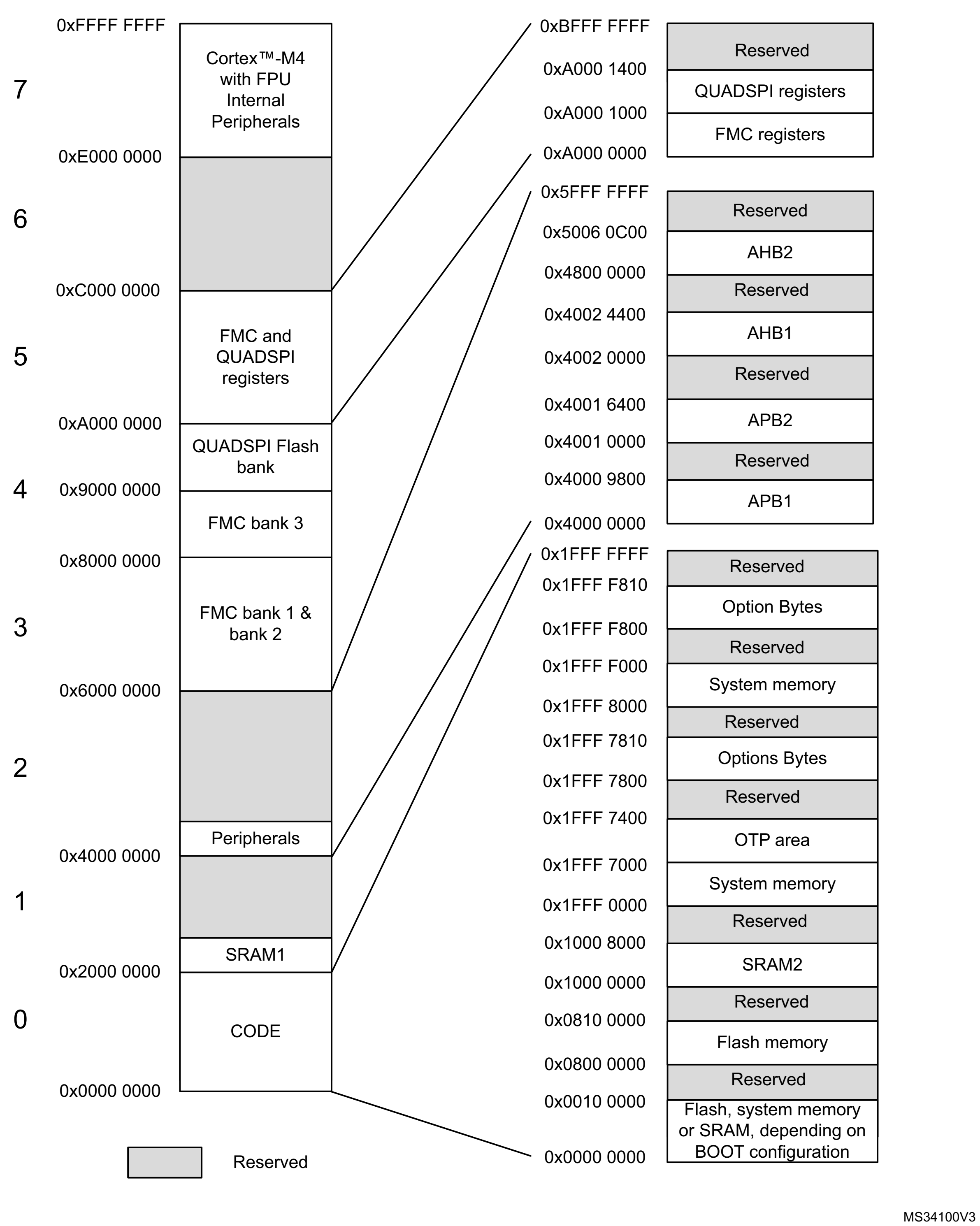


Table 18. STM32L476xx memory map and peripheral register boundary addresses (continued)(1)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

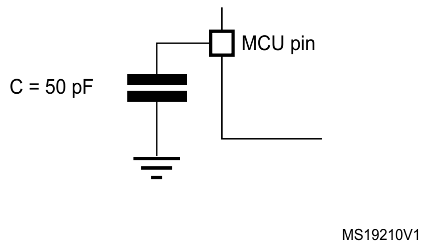


Figure 12. Pin input voltage

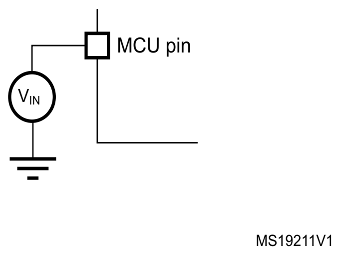
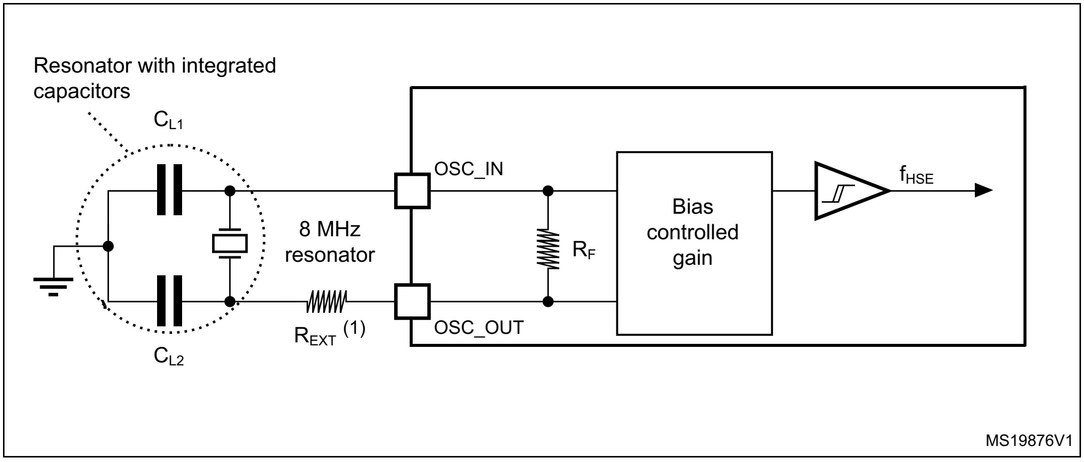


Table 35. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					MAX[1]					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	6.59	24.7	92.7	208	437	16	62	232	520	1093	µA
				2.4 V	6.65	24.8	92.9	209	439	17	62	232	523	1098	
				3 V	6.65	24.9	93.3	210	442	17	62	233	525	1105	
				3.6 V	6.70	25.1	93.8	212	447	17	63	235	530	1118	
		-	LCD enabled[2] clocked by LSI	1.8 V	7.00	25.2	97.2	219	461	18	63	243	548	1153	
				2.4 V	7.14	25.4	97.5	220	463	18	64	244	550	1158	
				3 V	7.24	25.7	97.7	221	465	18	64	244	553	1163	
				3.6 V	7.36	26.1	98.7	223	471	18	65	247	558	1178	
I_{DD} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	LCD disabled	1.8 V	6.88	25.0	93.1	209	439	17	63	233	523	1098	µA
				2.4 V	7.02	25.2	93.7	210	441	18	63	234	525	1103	
				3 V	7.12	25.4	94.2	212	444	18	64	236	530	1110	
				3.6 V	7.25	25.7	95.2	214	449	18	64	238	535	1123	
			LCD enabled[2]	1.8 V	7.01	26.1	99.0	223	467	18	65	248	558	1168	
				2.4 V	7.14	26.3	99.6	225	470	18	66	249	563	1175	
				3 V	7.31	26.6	100.0	226	474	18	67	250	565	1185	
				3.6 V	7.41	26.9	102.0	229	480	19	67	255	573	1200	
		RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	6.91	25.2	93.4	210	440	17	63	234	525	1100	
				2.4 V	7.04	25.3	94.2	211	443	18	63	236	528	1108	
				3 V	7.19	25.7	95.0	212	446	18	64	238	530	1115	
				3.6 V	7.97	26.0	96.1	215	451	20	65	240	538	1128	
		RTC clocked by LSE quartz[3] in low drive mode	LCD disabled	1.8 V	6.85	25.0	93.0	208.3	-	17	63	233	521	-	
				2.4 V	6.94	25.1	93.2	209.3	-	17	63	233	523	-	
				3 V	7.10	25.2	93.6	210.3	-	18	63	234	526	-	
				3.6 V	7.34	25.4	94.1	212.3	-	18	64	235	531	-	

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

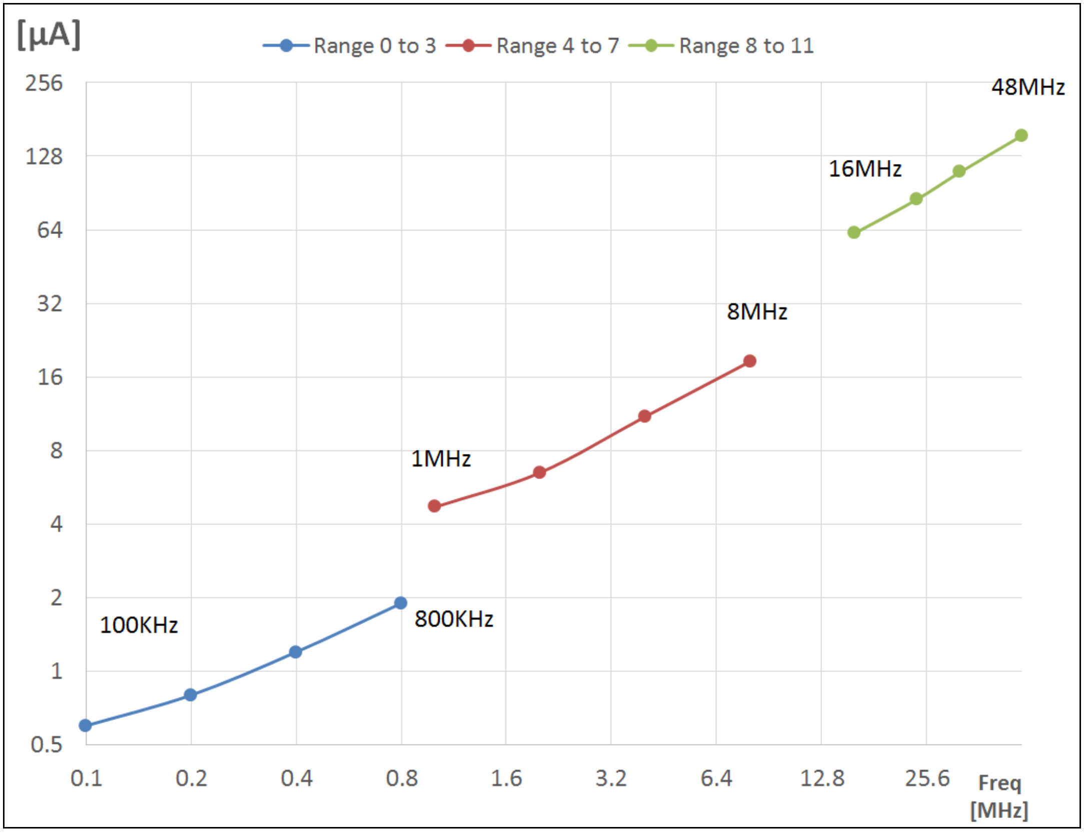
Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Figure 21. Typical current consumption versus MSI frequency



Low-speed internal (LSI) RC oscillator

Table 49. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, TA = -40 to 125 °C	29.5	-	34	
t_{SU}(LSI)(2)	LSI oscillator start-up time	-	-	80	130	µs
t_{STAB}(LSI)(2)	LSI oscillator stabilisation time	5% of final frequency	-	125	180	µs
I_{DD}(LSI)(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 50* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

6.3.10 Flash memory characteristics

Table 51. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 52. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 71. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. To well control inrush current of VREFBUF during start-up phase and scaling change, V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 0.

Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 84* and *Table 85* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 84. Quad SPI characteristics in SDR mode[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	$1.71 < V_{DD} < 3.6$ V, $C_{LOAD} = 20$ pF Voltage Range 1	-	-	40	MHz
		$1.71 < V_{DD} < 3.6$ V, $C_{LOAD} = 15$ pF Voltage Range 1	-	-	48	
		$2.7 < V_{DD} < 3.6$ V, $C_{LOAD} = 15$ pF Voltage Range 1	-	-	60	
		$1.71 < V_{DD} < 3.6$ V $C_{LOAD} = 20$ pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2-2$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2+2$	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	4	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	5.5	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2.5	5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	1.5	-	-	
		Voltage Range 2	2	-	-	

1. Guaranteed by characterization results.

Table 98. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Using the values obtained in *Table 113* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 67* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 67. LQFP64 P_D max vs. T_A

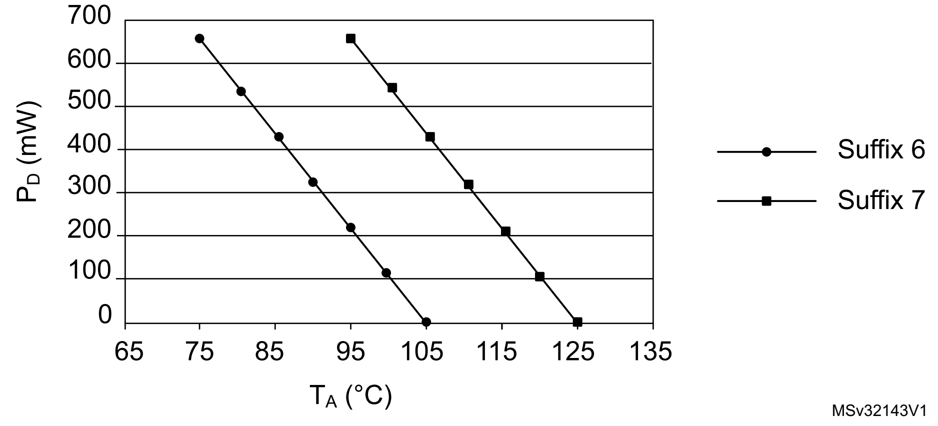


Table 115. Document revision history (continued)

Date	Revision	Changes
03-Dec-2015	4	In all the document: – Stop 1 with main regulator becomes Stop 0 – Stop 1 with low-power regulator remains as Stop 1. In *Section 4: Pinouts and pin description*: – PC14/OSC32_IN becomes PC14-OSC32_IN (PC14) – PC15/OSC32_OUT becomes PC15-OSC32_OUT (PC15) – PH0/OSC_IN becomes PH0-OSC_IN (PH0) – PH1/OSC_OUT becomes PH1-OSC_OUT (PH1) – PA13 becomes PA13 (JTMS-SWDIO) – PA14 becomes PA14 (JTCK-SWCLK) – PA15 becomes PA15 (JTDI) – PB3 becomes PB3 (JTDO-TRACESWO) – PB4 becomes PB4 (NJTRST). Added *Table 12: STM32L4x6 USART/UART/LPUART features*. Added *Note 5.* Updated *Table 25: Embedded internal voltage reference*. Updated *Table 34: Current consumption in Stop 2 mode*. Updated *Table 35: Current consumption in Stop 1 mode*. Updated *Table 36: Current consumption in Stop 0 mode*. Updated *Table 37: Current consumption in Standby mode*. Updated *Table 38: Current consumption in Shutdown mode*. Updated *Table 41: Low-power mode wakeup timings*. Added *Figure 15: VREFINT versus temperature*. Updated *Figure 20: HSI16 frequency versus temperature*. Updated *Table 58: I/O static characteristics*. Updated *Table 69: DAC characteristics*. Updated *Figure 52: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline*. Updated *Table 105: UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data*.