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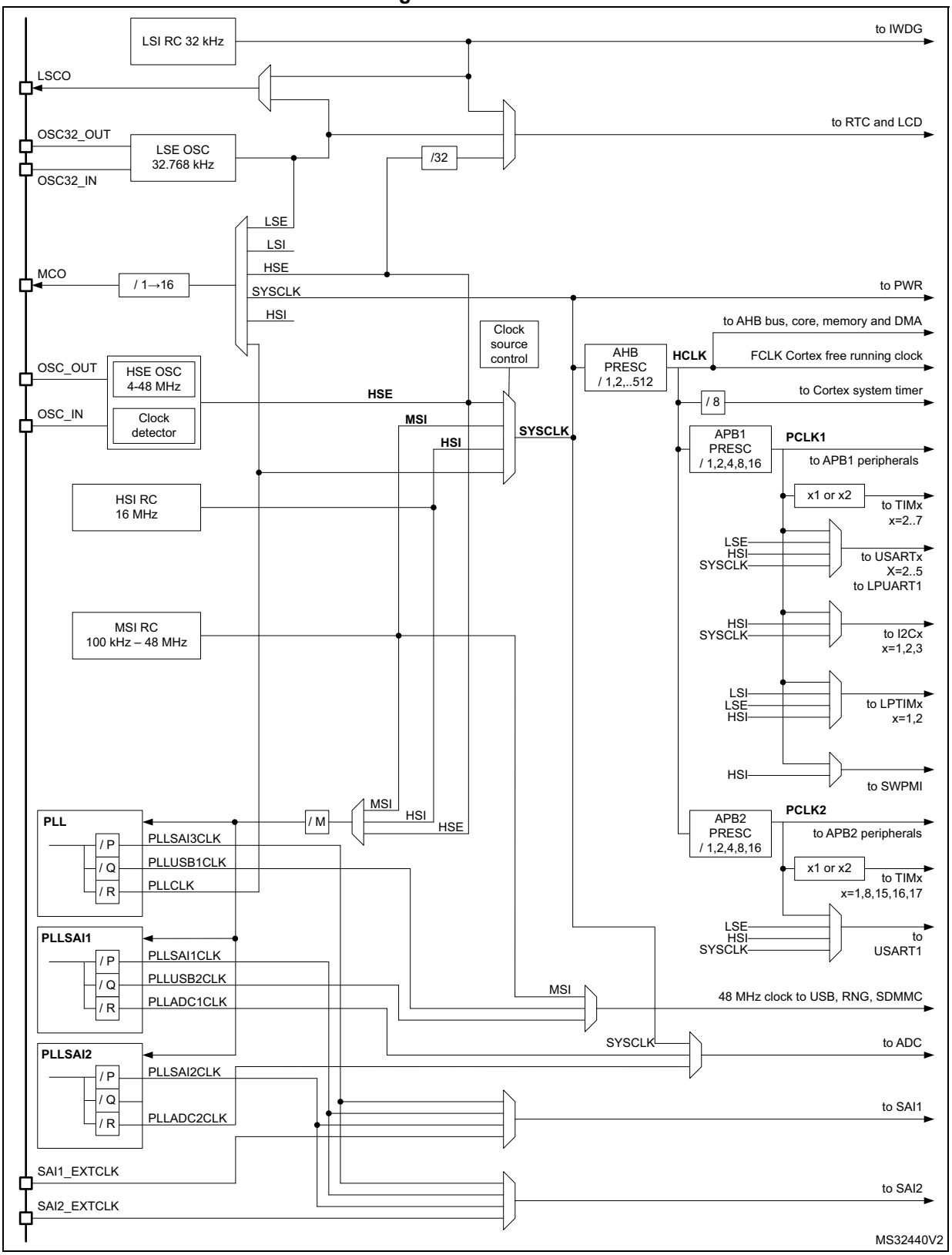
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l476vgt6

Figure 3. Clock tree



3.19 Operational amplifier (OPAMP)

The STM32L476xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.26 Inter-integrated circuit interface (I2C)

The device embeds 3 I2C. Refer to *Table 11: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol ($PMBus^{TM}$) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 3: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

1. X: supported

- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.33 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

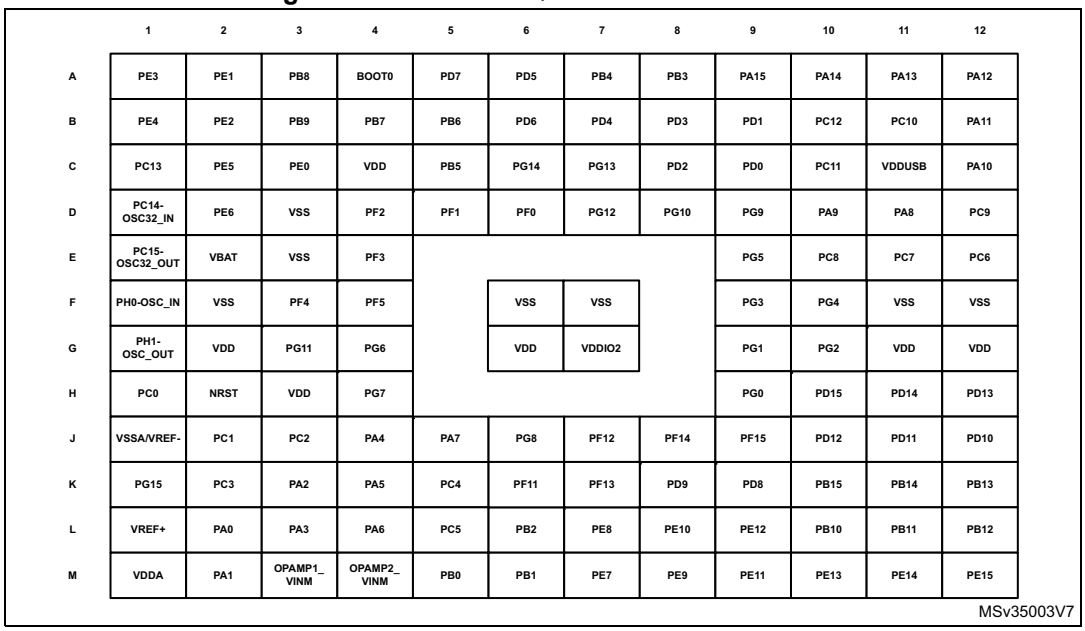
The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.34 Universal serial bus on-the-go full-speed (OTG_FS)

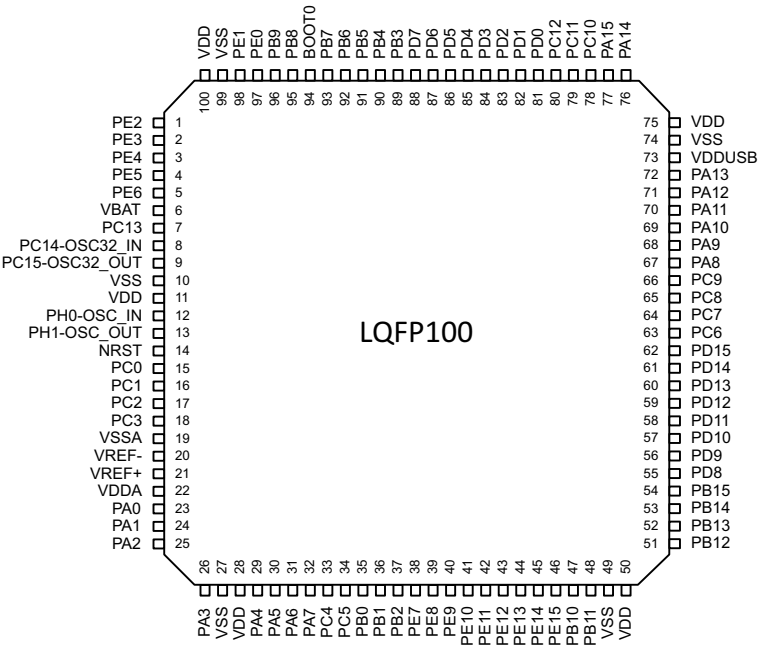
The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

Figure 5. STM32L476Qx UFBGA132 ballout(1)



1. The above figure shows the package top view.

Figure 6. STM32L476Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	-	M4	-	OPAMP2_VINM	I	TT	-	-	-
23	H4	H4	32	J5	43	PA7	I/O	FT_la	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
24	J7	J7	33	K5	44	PC4	I/O	FT_la	-	USART3_TX, LCD_SEG22, EVENTOUT	COMP1_INM, ADC12_IN13
25	J6	J6	34	L5	45	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
26	J5	J5	35	M5	46	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, EVENTOUT	OPAMP2_VOUT, ADC12_IN15
27	J4	J4	36	M6	47	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN0, USART3_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	J3	J3	37	L6	48	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM_CKIN0, EVENTOUT	COMP1_INP
-	-	-	-	K6	49	PF11	I/O	FT	-	EVENTOUT	-
-	-	-	-	J7	50	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	52	VDD	S	-	-	-	-
-	-	-	-	K7	53	PF13	I/O	FT	-	DFSDM_DATIN6, FMC_A7, EVENTOUT	-
-	-	-	-	J8	54	PF14	I/O	FT	-	DFSDM_CKIN6, TSC_G8_IO1, FMC_A8, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	-	J9	55	PF15	I/O	FT	-	TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	-	-	H9	56	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	G9	57	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	-	E6	38	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	-	F6	39	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	-	-	40	M8	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	-	-	F6	61	VSS	S	-	-	-	-
-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	63	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	-	-	42	M9	64	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT	-
-	-	-	43	L9	65	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	-	-	44	M10	66	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	45	M11	67	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	-	-	46	M12	68	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-
29	H3	H3	47	L10	69	PB10	I/O	FT_fl	-	TIM2_CH3, I2C2_SCL, SPI2_SCK, DFSDM_DATIN7, USART3_TX, LPUART1_RX, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	G3	G3	48	L11	70	PB11	I/O	FT_fl	-	TIM2_CH4, I2C2_SDA, DFSDM_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
31	J2	J2	49	F12	71	VSS	S	-	-	-	-
32	J1	J1	50	G12	72	VDD	S	-	-	-	-
33	H1	H1	51	L12	73	PB12	I/O	FT_l	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-

Table 15. STM32L476xxSTM32L476xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	WLCSP81	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
34	H2	H2	52	K12	74	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM_CKIN1, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SWPMI1_TX, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
35	G2	G2	53	K11	75	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM_DATIN2, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
36	G1	G1	54	K10	76	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM_CKIN2, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	F5	55	K9	77	PD8	I/O	FT_l	-	USART3_TX, LCD_SEG28, FMC_D13, EVENTOUT	-
-	-	F4	56	K8	78	PD9	I/O	FT_l	-	USART3_RX, LCD_SEG29, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	-	-	57	J12	79	PD10	I/O	FT_l	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	58	J11	80	PD11	I/O	FT_l	-	USART3_CTS, TSC_G6_IO2, LCD_SEG31, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-

Table 18. STM32L476xx memory map and peripheral register boundary addresses (continued)[1]

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 1800 - 0x4000 23FF	3 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 41* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 41. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		6	9.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	5.6	10.9	µs
			Wakeup clock HSI16 = 16 MHz	4.7	10.4	
		Range 2	Wakeup clock MSI = 24 MHz	5.7	11.1	
			Wakeup clock HSI16 = 16 MHz	4.5	10.5	
			Wakeup clock MSI = 4 MHz	6.6	14.2	
	Wake up time from Stop 0 mode to Low-power run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	0.7	2.05	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
		Range 2	Wakeup clock MSI = 24 MHz	0.8	2.72	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
			Wakeup clock MSI = 4 MHz	2.4	11.32	

Table 41. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.2	10.2	µs
			Wakeup clock HSI16 = 16 MHz	6.3	8.99	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	10.46	
			Wakeup clock HSI16 = 16 MHz	6.3	8.87	
			Wakeup clock MSI = 4 MHz	8.0	13.23	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	4.5	5.78	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.0	6.5	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
			Wakeup clock MSI = 4 MHz	8.2	13.5	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	12.7	20	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			10.7	21.5	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.0	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
		Range 2	Wakeup clock MSI = 24 MHz	8.2	9.9	
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
			Wakeup clock MSI = 4 MHz	10.6	15.8	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.1	6.7	
			Wakeup clock HSI16 = 16 MHz	5.7	8	
		Range 2	Wakeup clock MSI = 24 MHz	5.5	6.65	
			Wakeup clock HSI16 = 16 MHz	5.7	7.53	
			Wakeup clock MSI = 4 MHz	8.2	16.6	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	20.8	µs
			Wakeup clock MSI = 4 MHz	20.1	35.5	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	24.3	µs
			Wakeup clock MSI = 4 MHz	20.1	38.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	256	330.6	µs

1. Guaranteed by characterization results.

Table 42. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

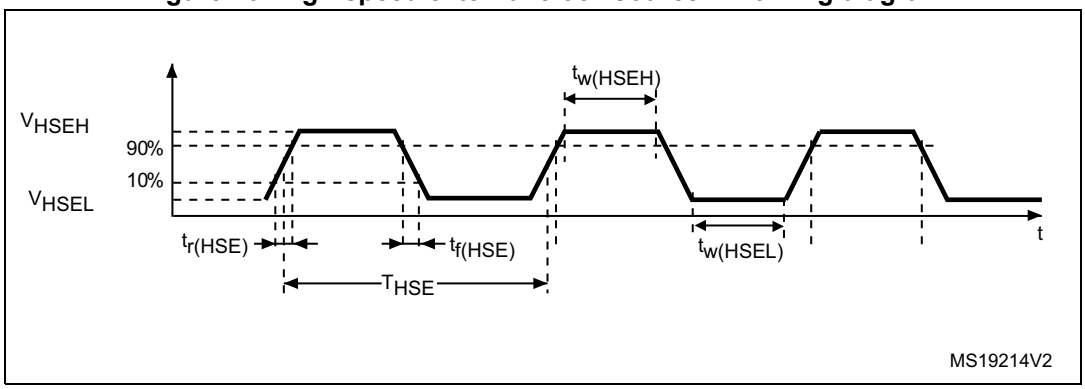
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16: High-speed external clock source AC timing diagram*.

Table 43. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 16. High-speed external clock source AC timing diagram



6.3.8 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 47. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 48. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	99	100	101	kHz
			Range 1	198	200	202	
			Range 2	396	400	404	
			Range 3	792	800	808	
			Range 4	0.99	1	1.01	MHz
			Range 5	1.98	2	2.02	
			Range 6	3.96	4	4.04	
			Range 7	7.92	8	8.08	
			Range 8	15.8	16	16.16	
			Range 9	23.8	24	24.4	
			Range 10	31.7	32	32.32	
			Range 11	47.5	48	48.48	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 66. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 25: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

6.3.21 Operational amplifiers characteristics

Table 73. OPAMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage(2)	-		1.8	-	3.6	V
CMIR	Common mode input range	-		0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.		-	-	±1.5	mV
		All voltage/Temp.		-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode		-	±5	-	µV/°C
		Low-power mode		-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-		-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-		-	1	1.35	
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	

Table 83. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	19	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	30	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	12.5	33	
-		Slave mode 1.08 < V_{DDIO2} < 1.32 V(3)	-	25	62.5	
$t_{v(MO)}$		Master mode	-	2.5	12.5	
$t_{h(SO)}$	Data output hold time	Slave mode	9	-	-	ns
-		Slave mode 1.08 < V_{DDIO2} < 1.32 V(3)	24	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 28. SPI timing diagram - slave mode and CPHA = 0

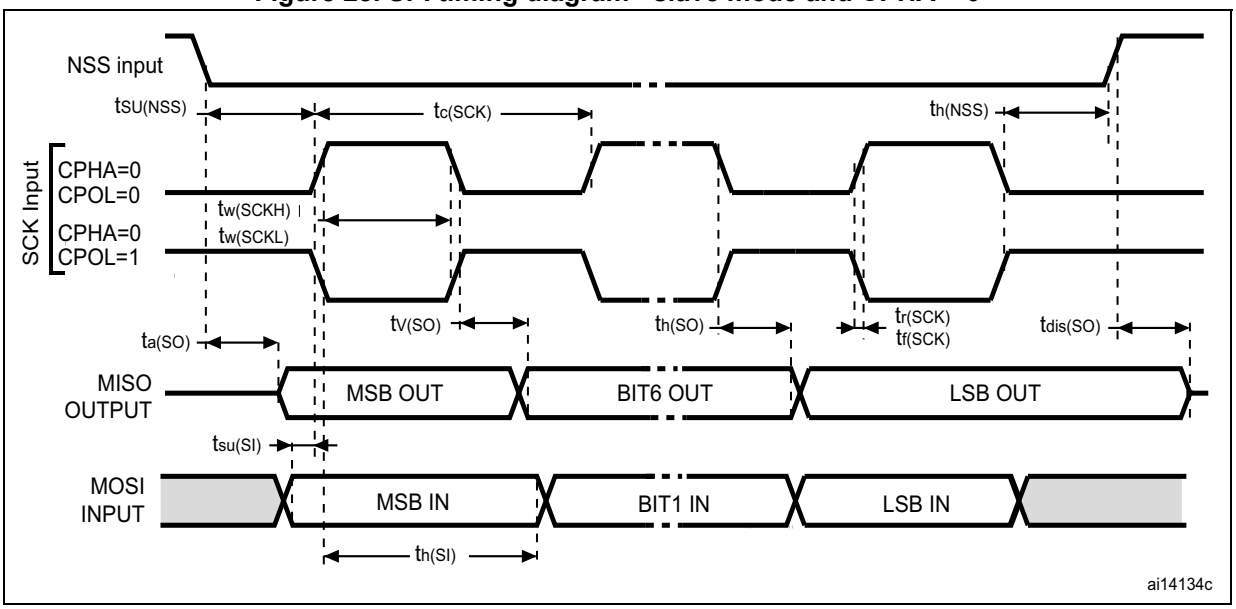
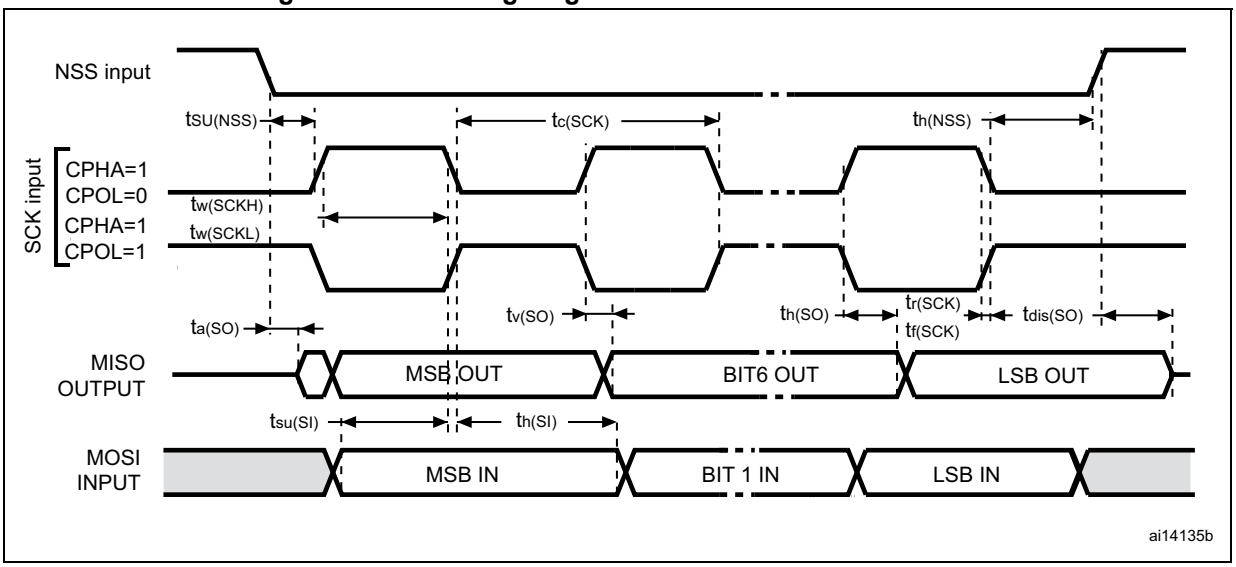
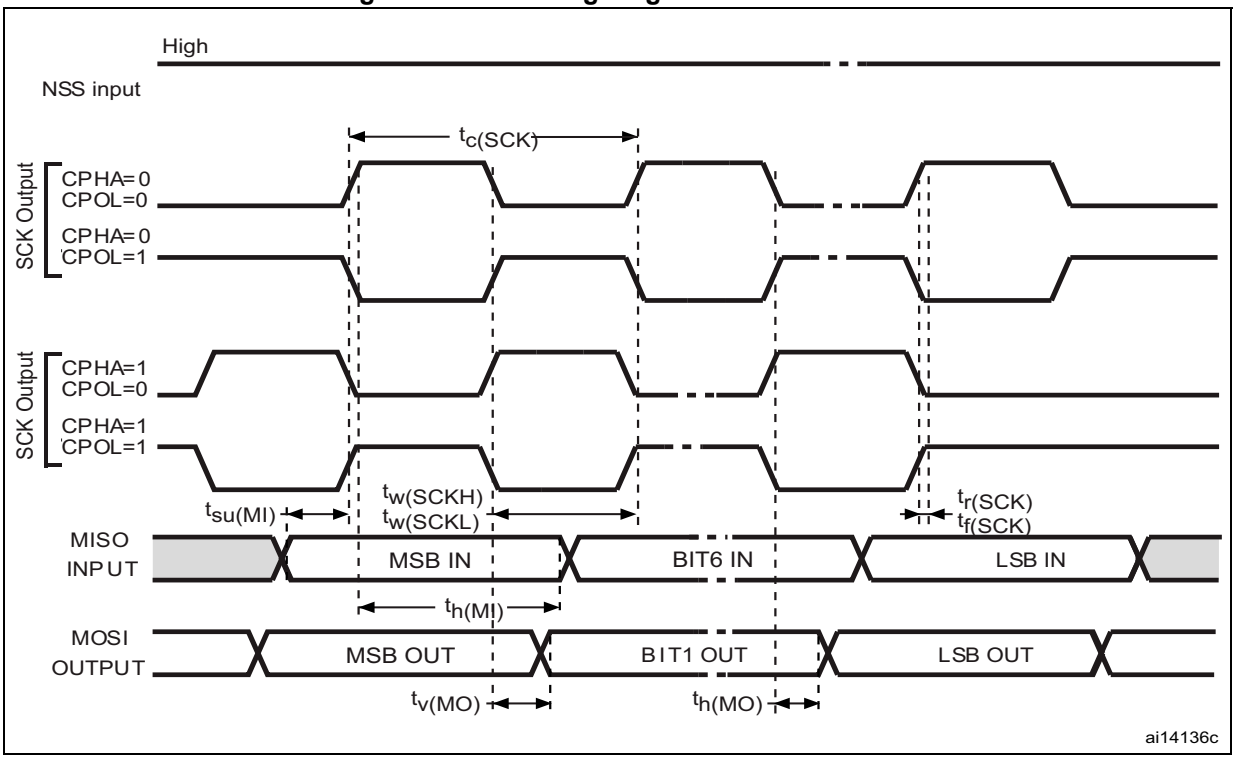


Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WLCSP72	46	
	Thermal resistance junction-ambient WLCSP81	41	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.