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#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg8e2ctg">https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg8e2ctg</a>

**Table 3-2. Stop Mode Behavior**

Peripheral	Mode	
	Stop2	Stop3
CPU	Off	Standby
RAM	Standby	Standby
FLASH	Off	Standby
Parallel Port Registers	Off	Standby
ADC	Off	Optionally On <sup>1</sup>
ACMP	Off	Optionally On <sup>2</sup>
BDM	Off <sup>3</sup>	Optionally On
ICS	Off	Optionally On <sup>4</sup>
IIC	Off	Standby
LVD/LVW	Off <sup>5</sup>	Optionally On
MTIM	Off	Standby
RTC	Optionally On	Optionally On
SCI	Off	Standby
SPI	Off	Standby
TPM	Off	Standby
Voltage Regulator	Standby	Optionally On <sup>6</sup>
XOSC	Off	Optionally On <sup>7</sup>
I/O Pins	States Held	States Held

<sup>1</sup> Requires the asynchronous ADC clock and LVD to be enabled, else in standby.

<sup>2</sup> Requires the LVD to be enabled when compare to internal bandgap reference option is enabled.

<sup>3</sup> If ENBDM is set when entering stop2, the MCU will actually enter stop3.

<sup>4</sup> IRCLKEN and IREFSTEN set in ICSC1, else in standby.

<sup>5</sup> If LVDSE is set when entering stop2, the MCU will actually enter stop3.

<sup>6</sup> Voltage regulator will be on if BDM is enabled or if LVD is enabled when entering stop3.

<sup>7</sup> ERCLKEN and EREFSTEN set in ICSC2, else in standby. For high frequency range (RANGE in ICSC2 set) requires the LVD to also be enabled in stop3.

## 4.2 Reset and Interrupt Vector Assignments

Table 4-1 shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the Freescale Semiconductor provided equate file for the MC9S08SG8.

**Table 4-1. Reset and Interrupt Vectors**

Address (High/Low)	Vector	Vector Name
0xFFC0:0xFFC1	Unused Vector Space (available for user program)	—
0xFFC2:0xFFC3	ACMP	Vacmp
0xFFC4:0xFFC5	Unused Vector Space (available for user program)	—
0xFFC6:0xFFC7	Unused Vector Space (available for user program)	—
0xFFC8:0xFFC9	Unused Vector Space (available for user program)	—
0xFFCA:0xFFCB	MTIM Overflow	Vmtim
0xFFCC:0xFFCD	RTC	Vrtc
0xFFCE:0xFFCF	IIC	Viic
0xFFD0:0xFFD1	ADC Conversion	Vadc
0xFFD2:0xFFD3	Unused Vector Space (available for user program)	—
0xFFD4:0xFFD5	Port B Pin Interrupt	Vportb
0xFFD6:0xFFD7	Port A Pin Interrupt	Vporta
0xFFD8:0xFFD9	Unused Vector Space (available for user program)	—
0xFFDA:0xFFDB	SCI Transmit	Vscitx
0xFFDC:0xFFDD	SCI Receive	Vscirx
0xFFDE:0xFFDF	SCI Error	Vscierr
0xFFE0:0xFFE1	SPI	Vspi
0xFFE2:0xFFE3	TPM2 Overflow	Vtpm2ovf
0xFFE4:0xFFE5	TPM2 Channel 1	Vtpm2ch1
0xFFE6:0xFFE7	TPM2 Channel 0	Vtpm2ch0
0xFFE8:0xFFE9	TPM1 Overflow	Vtpm1ovf
0xFFEA:0xFFEB	Unused Vector Space (available for user program)	—
0xFFEC:0xFFED	Unused Vector Space (available for user program)	—
0xFFEE:0xFFEF	Unused Vector Space (available for user program)	—
0xFFFF0:0xFFFF1	Unused Vector Space (available for user program)	—
0xFFFF2:0xFFFF3	TPM1 Channel 1	Vtpm1ch1
0xFFFF4:0xFFFF5	TPM1 Channel 0	Vtpm1ch0
0xFFFF6:0xFFFF7	Unused Vector Space (available for user program)	—
0xFFFF8:0xFFFF9	Low Voltage Detect	Vlvd
0xFFFFA:0xFFFFB	Unused Vector Space (available for user program)	—
0xFFFFC:0xFFFFD	SWI	Vswi
0xFFFFE:0xFFFFF	Reset	Vreset

Table 4-2. Direct-Page Register Summary (Sheet 2 of 3)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0039	SCIBDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x003A	SCIC1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x003B	SCIC2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x003C	SCIS1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x003D	SCIS2	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
0x003E	SCIC3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x003F	SCID	Bit 7	6	5	4	3	2	1	Bit 0
0x0040– 0x0047	Reserved	—	—	—	—	—	—	—	—
0x0048	ICSC1	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
0x0049	ICSC2	BDIV		RANGE	HGO	LP	EREFS	ERCLKEN	EREFSTEN
0x004A	ICSTRM	TRIM							
0x004B	ICSSC	0	0	0	IREFST	CLKST		OSCINIT	FTRIM
0x004C– 0x004F	Reserved	—	—	—	—	—	—	—	—
0x0050	SPIC1	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
0x0051	SPIC2	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
0x0052	SPIBR	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
0x0053	SPIS	SPRF	0	SPTEF	MODF	0	0	0	0
0x0054	Reserved	0	0	0	0	0	0	0	0
0x0055	SPID	Bit 7	6	5	4	3	2	1	Bit 0
0x0056– 0x0057	Reserved	—	—	—	—	—	—	—	—
0x0058	IICA	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0x0059	IICF	MULT			ICR				
0x005A	IICC1	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0
0x005B	IICS	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
0x005C	IICD	DATA							
0x005D	IICC2	GCAEN	ADEXT	0	0	0	AD10	AD9	AD8
0x005E– 0x005F	Reserved	—	—	—	—	—	—	—	—
0x0060	TPM2SC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
0x0061	TPM2CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x0062	TPM2CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x0063	TPM2MODH	Bit 15	14	13	12	11	10	9	Bit 8
0x0064	TPM2MODL	Bit 7	6	5	4	3	2	1	Bit 0
0x0065	TPM2C0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
0x0066	TPM2C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0067	TPM2C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0068	TPM2C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0

# Chapter 5

## Resets, Interrupts, and General System Control

### 5.1 Introduction

This section discusses basic reset and interrupt mechanisms and the various sources of reset and interrupt in the MC9S08SG8. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data sheet. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog are not part of on-chip peripheral systems with their own chapters.

### 5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation
- Reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vector for each module (reduces polling overhead) (see [Table 5-2](#))

### 5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFF:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with pull-up devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

The MC9S08SG8 has the following sources for reset:

- Power-on reset (POR)
- External pin reset (PIN)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect (IOP)
- Illegal address detect (ILAD)
- Background debug forced reset

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register (SRS).

Table 7-2. Instruction Set Summary (Sheet 5 of 9)

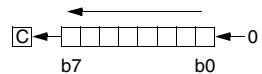
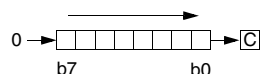
Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR				
						VH	I	N	Z	C
INC <i>opr8a</i> INCA INCX INC <i>opr8,X</i> INC ,X INC <i>opr8,SP</i>	Increment $M \leftarrow (M) + 0x01$ $A \leftarrow (A) + 0x01$ $X \leftarrow (X) + 0x01$ $M \leftarrow (M) + 0x01$ $M \leftarrow (M) + 0x01$ $M \leftarrow (M) + 0x01$	DIR INH INH IX1 IX SP1	3C dd 4C 5C 6C ff 7C 9E 6C ff	5 1 1 5 4 6	r fwpp p p r fwpp r fwp p rfwpp					
JMP <i>opr8a</i> JMP <i>opr16a</i> JMP <i>opr16,X</i> JMP <i>opr8,X</i> JMP ,X	Jump PC ← Jump Address	DIR EXT IX2 IX1 IX	BC dd CC hh ll DC ee ff EC ff FC	3 4 4 3 3	ppp pppp pppp ppp ppp					
JSR <i>opr8a</i> JSR <i>opr16a</i> JSR <i>opr16,X</i> JSR <i>opr8,X</i> JSR ,X	Jump to Subroutine PC ← (PC) + <i>n</i> ( <i>n</i> = 1, 2, or 3) Push (PCL); SP ← (SP) – 0x0001 Push (PCH); SP ← (SP) – 0x0001 PC ← Unconditional Address	DIR EXT IX2 IX1 IX	BD dd CD hh ll DD ee ff ED ff FD	5 6 6 5 5	ssppp pssppp pssppp ssppp ssppp					
LDA # <i>opr8i</i> LDA <i>opr8a</i> LDA <i>opr16a</i> LDA <i>opr16,X</i> LDA <i>opr8,X</i> LDA ,X LDA <i>opr16,SP</i> LDA <i>opr8,SP</i>	Load Accumulator from Memory $A \leftarrow (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	A6 ii B6 dd C6 hh ll D6 ee ff E6 ff F6 9E D6 ee ff 9E E6 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0				
LDHX # <i>opr16i</i> LDHX <i>opr8a</i> LDHX <i>opr16a</i> LDHX ,X LDHX <i>opr16,X</i> LDHX <i>opr8,X</i> LDHX <i>opr8,SP</i>	Load Index Register (H:X) $H:X \leftarrow (M:M + 0x0001)$	IMM DIR EXT IX IX2 IX1 SP1	45 jj kk 55 dd 32 hh ll 9E AE 9E BE ee ff 9E CE ff 9E FE ff	3 4 5 5 6 5 5	ppp rppp prppp prfp pprrpp prppp prppp	0				
LDX # <i>opr8i</i> LDX <i>opr8a</i> LDX <i>opr16a</i> LDX <i>opr16,X</i> LDX <i>opr8,X</i> LDX ,X LDX <i>opr16,SP</i> LDX <i>opr8,SP</i>	Load X (Index Register Low) from Memory $X \leftarrow (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	AE ii BE dd CE hh ll DE ee ff EE ff FE 9E DE ee ff 9E EE ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0				
LSL <i>opr8a</i> LSLA LSLX LSL <i>opr8,X</i> LSL ,X LSL <i>opr8,SP</i>	Logical Shift Left  (Same as ASL)	DIR INH INH IX1 IX SP1	38 dd 48 58 68 ff 78 9E 68 ff	5 1 1 5 4 6	r fwpp p p r fwpp r fwp p rfwpp					
LSR <i>opr8a</i> LSRA LSRX LSR <i>opr8,X</i> LSR ,X LSR <i>opr8,SP</i>	Logical Shift Right 	DIR INH INH IX1 IX SP1	34 dd 44 54 64 ff 74 9E 64 ff	5 1 1 5 4 6	r fwpp p p r fwpp r fwp p rfwpp					

Table 7-2. Instruction Set Summary (Sheet 7 of 9)

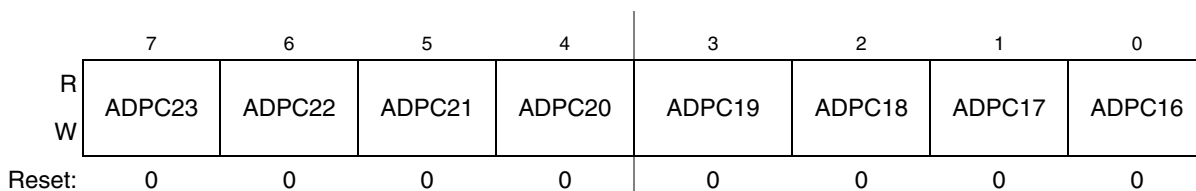
Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR			
						VH	I	N	Z C
RSP	Reset Stack Pointer (Low Byte) SPL ← 0xFF (High Byte Not Affected)	INH	9C	1	p	--	----		
RTI	Return from Interrupt SP ← (SP) + 0x0001; Pull (CCR) SP ← (SP) + 0x0001; Pull (A) SP ← (SP) + 0x0001; Pull (X) SP ← (SP) + 0x0001; Pull (PCH) SP ← (SP) + 0x0001; Pull (PCL)	INH	80	9	uuuuufppp	▯▯	▯▯▯▯		
RTS	Return from Subroutine SP ← SP + 0x0001; Pull (PCH) SP ← SP + 0x0001; Pull (PCL)	INH	81	5	ufppp	--	----		
SBC #opr8i SBC opr8a SBC opr16a SBC oprx16,X SBC oprx8,X SBC ,X SBC oprx16,SP SBC oprx8,SP	Subtract with Carry A ← (A) – (M) – (C)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A2 ii B2 dd C2 hh ll D2 ee ff E2 ff F2 9E D2 ee ff 9E E2 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rpp pprpp prpp	▯–	–▯▯▯		
SEC	Set Carry Bit (C ← 1)	INH	99	1	p	--	----		1
SEI	Set Interrupt Mask Bit (I ← 1)	INH	9B	1	p	--	1----		
STA opr8a STA opr16a STA oprx16,X STA oprx8,X STA ,X STA oprx16,SP STA oprx8,SP	Store Accumulator in Memory M ← (A)	DIR EXT IX2 IX1 IX SP2 SP1	B7 dd C7 hh ll D7 ee ff E7 ff F7 9E D7 ee ff 9E E7 ff	3 4 4 3 2 5 4	wpp pwpp pwpp wpp wp ppwpp pwpp	0–	–▯▯–		
STHX opr8a STHX opr16a STHX oprx8,SP	Store H:X (Index Reg.) (M:M + 0x0001) ← (H:X)	DIR EXT SP1	35 dd 96 hh ll 9E FF ff	4 5 5	wpp pwpp pwpp	0–	–▯▯–		
STOP	Enable Interrupts: Stop Processing Refer to MCU Documentation I bit ← 0; Stop Processing	INH	8E	2	fp...	--	0----		
STX opr8a STX opr16a STX oprx16,X STX oprx8,X STX ,X STX oprx16,SP STX oprx8,SP	Store X (Low 8 Bits of Index Register) in Memory M ← (X)	DIR EXT IX2 IX1 IX SP2 SP1	BF dd CF hh ll DF ee ff EF ff FF 9E DF ee ff 9E EF ff	3 4 4 3 2 5 4	wpp pwpp pwpp wpp wp ppwpp pwpp	0–	–▯▯–		

**Table 9-10. APCTL2 Register Field Descriptions (continued)**

Field	Description
1 ADPC9	<b>ADC Pin Control 9</b> — ADPC9 is used to control the pin associated with channel AD9. 0 AD9 pin I/O control enabled 1 AD9 pin I/O control disabled
0 ADPC8	<b>ADC Pin Control 8</b> — ADPC8 is used to control the pin associated with channel AD8. 0 AD8 pin I/O control enabled 1 AD8 pin I/O control disabled

### 9.3.10 Pin Control 3 Register (APCTL3)

APCTL3 is used to control channels 16–23 of the ADC module.


**Figure 9-13. Pin Control 3 Register (APCTL3)**
**Table 9-11. APCTL3 Register Field Descriptions**

Field	Description
7 ADPC23	<b>ADC Pin Control 23</b> — ADPC23 is used to control the pin associated with channel AD23. 0 AD23 pin I/O control enabled 1 AD23 pin I/O control disabled
6 ADPC22	<b>ADC Pin Control 22</b> — ADPC22 is used to control the pin associated with channel AD22. 0 AD22 pin I/O control enabled 1 AD22 pin I/O control disabled
5 ADPC21	<b>ADC Pin Control 21</b> — ADPC21 is used to control the pin associated with channel AD21. 0 AD21 pin I/O control enabled 1 AD21 pin I/O control disabled
4 ADPC20	<b>ADC Pin Control 20</b> — ADPC20 is used to control the pin associated with channel AD20. 0 AD20 pin I/O control enabled 1 AD20 pin I/O control disabled
3 ADPC19	<b>ADC Pin Control 19</b> — ADPC19 is used to control the pin associated with channel AD19. 0 AD19 pin I/O control enabled 1 AD19 pin I/O control disabled
2 ADPC18	<b>ADC Pin Control 18</b> — ADPC18 is used to control the pin associated with channel AD18. 0 AD18 pin I/O control enabled 1 AD18 pin I/O control disabled



2. Update status and control register 2 (ADCSC2) to select the conversion trigger (hardware or software) and compare function options, if enabled.
3. Update status and control register 1 (ADCSC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

### 9.5.1.2 Pseudo — Code Example

In this example, the ADC module will be set up with interrupts enabled to perform a single 10-bit conversion at low power with a long sample time on input channel 1, where the internal ADCK clock will be derived from the bus clock divided by 1.

#### **ADCCFG = 0x98 (%10011000)**

Bit 7	ADLPC	1	Configures for low power (lowers maximum clock speed)
Bit 6:5	ADIV	00	Sets the ADCK to the input clock ÷ 1
Bit 4	ADLSMP	1	Configures for long sample time
Bit 3:2	MODE	10	Sets mode at 10-bit conversions
Bit 1:0	ADICLK	00	Selects bus clock as input clock source

#### **ADCSC2 = 0x00 (%00000000)**

Bit 7	ADACT	0	Flag indicates if a conversion is in progress
Bit 6	ADTRG	0	Software trigger selected
Bit 5	ACFE	0	Compare function disabled
Bit 4	ACFGT	0	Not used in this example
Bit 3:2		00	Unimplemented or reserved, always reads zero
Bit 1:0		00	Reserved for Freescale's internal use; always write zero

#### **ADCSC1 = 0x41 (%01000001)**

Bit 7	COCO	0	Read-only flag which is set when a conversion completes
Bit 6	AIEN	1	Conversion complete interrupt enabled
Bit 5	ADCO	0	One conversion only (continuous conversions disabled)
Bit 4:0	ADCH	00001	Input channel 1 selected as ADC input channel

#### **ADCRH/L = 0xxx**

Holds results of conversion. Read high byte (ADCRH) before low byte (ADCRL) so that conversion data cannot be overwritten with data from the next conversion.

#### **ADCCVH/L = 0xxx**

Holds compare value when compare function enabled

#### **APCTL1=0x02**

AD1 pin I/O control disabled. All other AD pins remain general purpose I/O pins

#### **APCTL2=0x00**

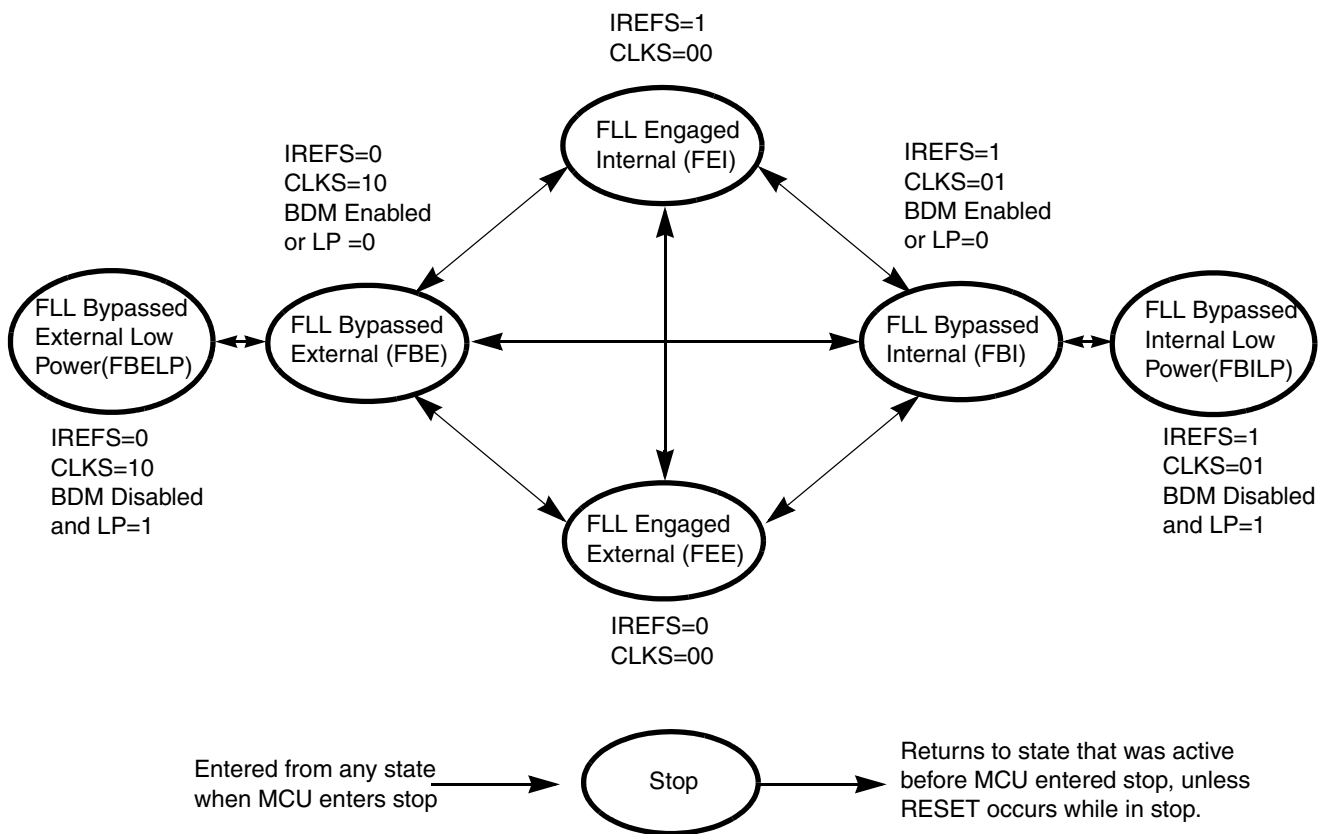
All other AD pins remain general purpose I/O pins

**Table 10-5. ICS Status and Control Register Field Descriptions (continued)**

Field	Description
1	<b>OSC Initialization</b> — If the external reference clock is selected by ERCLKEN or by the ICS being in FEE, FBE, or FBELP mode, and if EREFS is set, then this bit is set after the initialization cycles of the external oscillator clock have completed. This bit is only cleared when either ERCLKEN or EREFS are cleared.
0	<b>ICS Fine Trim</b> — The FTRIM bit controls the smallest adjustment of the internal reference clock frequency. Setting FTRIM will increase the period and clearing FTRIM will decrease the period by the smallest amount possible.

## 10.4 Functional Description

### 10.4.1 Operational Modes


**Figure 10-7. Clock Switching Modes**

The seven states of the ICS are shown as a state diagram and are described below. The arrows indicate the allowed movements between the states.

#### 10.4.1.1 FLL Engaged Internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all the following conditions occur:

## Internal Clock Source (S08ICSV2)

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

### 10.4.1.2 FLL Engaged External (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

### 10.4.1.3 FLL Bypassed Internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is active or LP bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

### 10.4.1.4 FLL Bypassed Internal Low Power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is not active and LP bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

The CLKS bits can also be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. The actual switch to the newly selected clock will not occur until after a few full cycles of the new clock. If the newly selected clock is not available, the previous clock will remain selected.

### 10.4.3 Bus Frequency Divider

The BDIV bits can be changed at anytime and the actual switch to the new frequency will occur immediately.

### 10.4.4 Low Power Bit Usage

The low power bit (LP) is provided to allow the FLL to be disabled and thus conserve power when it is not being used. However, in some applications it may be desirable to enable the FLL and allow it to lock for maximum accuracy before switching to an FLL engaged mode. Do this by writing the LP bit to 0.

### 10.4.5 Internal Reference Clock

When IRCLKEN is set the internal reference clock signal will be presented as ICSIRCLK, which can be used as an additional clock source. The ICSIRCLK frequency can be re-targeted by trimming the period of the internal reference clock. This can be done by writing a new value to the TRIM bits in the ICSTRM register. Writing a larger value will slow down the ICSIRCLK frequency, and writing a smaller value to the ICSTRM register will speed up the ICSIRCLK frequency. The TRIM bits will effect the ICSOUT frequency if the ICS is in FLL engaged internal (FEI), FLL bypassed internal (FBI), or FLL bypassed internal low power (FBILP) mode. The TRIM and FTRIM value will not be affected by a reset.

Until ICSIRCLK is trimmed, programming low reference divider (RDIV) factors may result in ICSOUT frequencies that exceed the maximum chip-level frequency and violate the chip-level clock timing specifications (see the [Device Overview](#) chapter).

If IREFSTEN is set and the IRCLKEN bit is written to 1, the internal reference clock will keep running during stop mode in order to provide a fast recovery upon exiting stop.

All MCU devices are factory programmed with a trim value in a reserved memory location. This value can be copied to the ICSTRM register during reset initialization. The factory trim value does not include the FTRIM bit. For finer precision, the user can trim the internal oscillator in the application and set the FTRIM bit accordingly.

### 10.4.6 Optional External Reference Clock

The ICS module can support an external reference clock with frequencies between 31.25 kHz to 5 MHz in all modes. When the ERCLKEN is set, the external reference clock signal will be presented as ICSECLK, which can be used as an additional clock source. When IREFS = 1, the external reference clock will not be used by the FLL and will only be used as ICSECLK. In these modes, the frequency can be equal to the maximum frequency the chip-level timing specifications will support (see the [Device Overview](#) chapter).

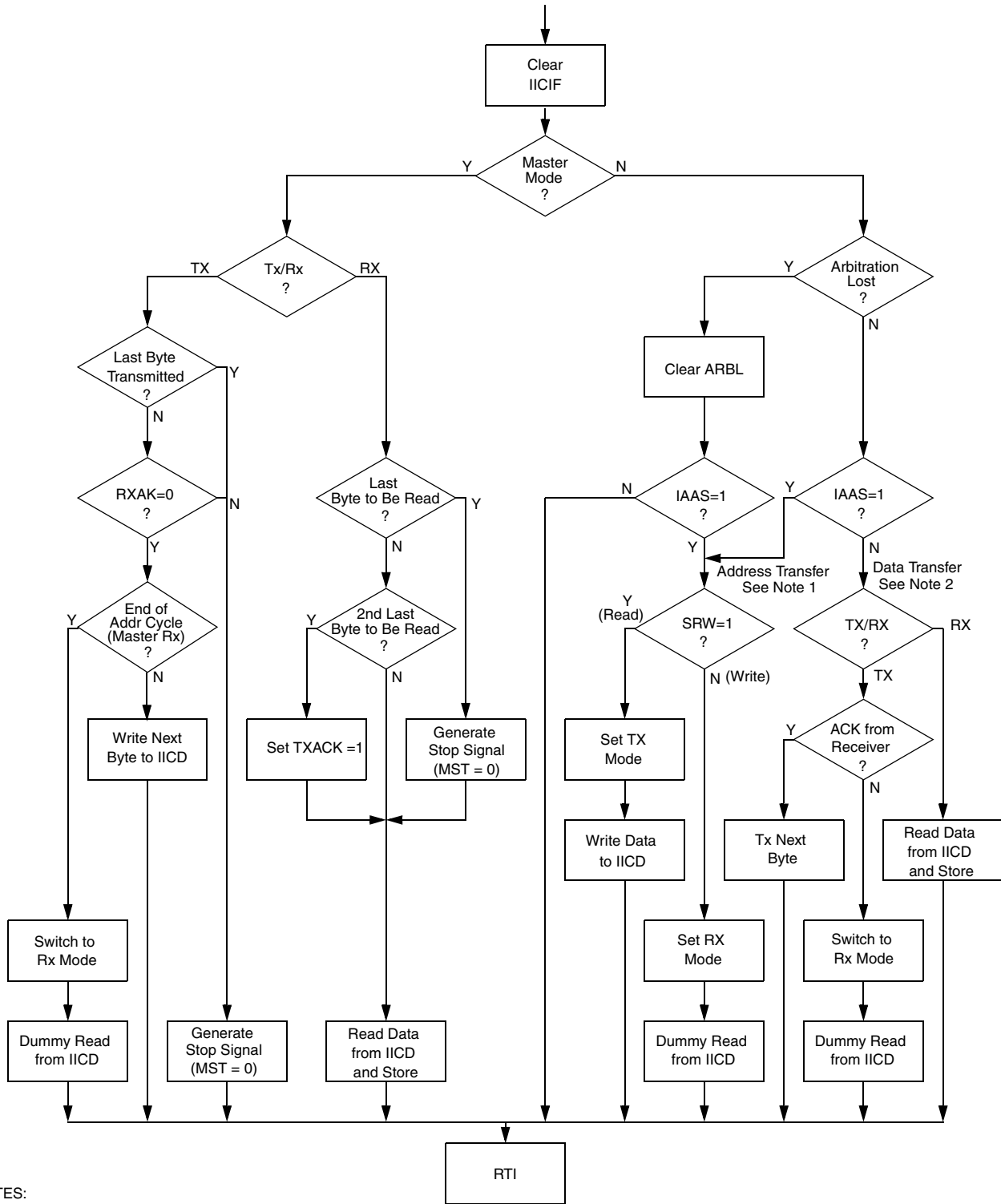
If EREFSTEN is set and the ERCLKEN bit is written to 1, the external reference clock will keep running during stop mode in order to provide a fast recovery upon exiting stop.

### 10.4.7 Fixed Frequency Clock

The ICS presents the divided FLL reference clock as ICSFFCLK for use as an additional clock source for peripheral modules. The ICS provides an output signal (ICSFFE) which indicates when the ICS is providing ICSOUT frequencies four times or greater than the divided FLL reference clock (ICSFFCLK). In FLL Engaged mode (FEI and FEE) this is always true and ICSFFE is always high. In ICS Bypass modes, ICSFFE will get asserted for the following combinations of BDIV and RDIV values:

- BDIV=00 (divide by 1), RDIV  $\geq$  010
- BDIV=01 (divide by 2), RDIV  $\geq$  011
- BDIV=10 (divide by 4), RDIV  $\geq$  100
- BDIV=11 (divide by 8), RDIV  $\geq$  101





NOTES:

- <sup>1</sup> If general call is enabled, a check must be done to determine whether the received address was a general call address (0x00). If the received address was a general call address, then the general call must be handled by user software.
- <sup>2</sup> When 10-bit addressing is used to address a slave, the slave sees an interrupt following the first byte of the extended address. User software must ensure that for this interrupt, the contents of IICD are ignored and not treated as a valid data transfer.

Figure 11-12. Typical IIC Interrupt Routine

### 12.3.3 MTIM Counter Register (MTIMCNT)

MTIMCNT is the read-only value of the current MTIM count of the 8-bit counter.

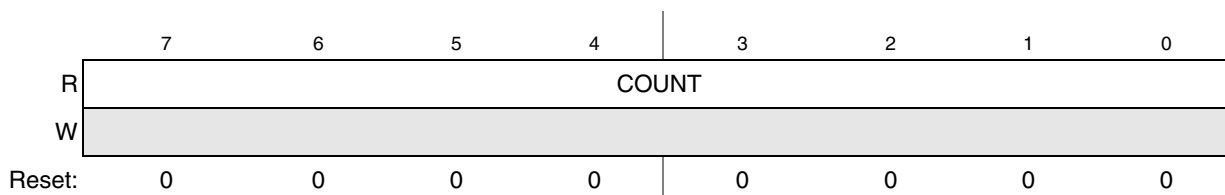


Figure 12-6. MTIM Counter Register

Table 12-4. MTIM Counter Register Field Description

Field	Description
7:0 COUNT	<b>MTIM Count</b> — These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset clears the count to \$00.

### 12.3.4 MTIM Modulo Register (MTIMMOD)

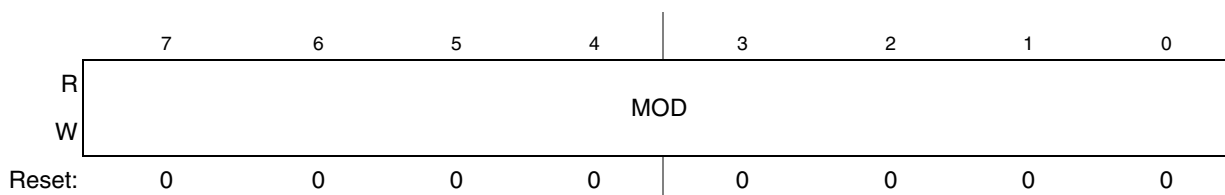


Figure 12-7. MTIM Modulo Register

Table 12-5. MTIM Modulo Register Field Descriptions

Field	Description
7:0 MOD	<b>MTIM Modulo</b> — These eight read/write bits contain the modulo value used to reset the count and set TOF. A value of \$00 puts the MTIM in free-running mode. Writing to MTIMMOD resets the COUNT to \$00 and clears TOF. Reset sets the modulo to \$00.



### 13.1.1 Features

Features of the RTC module include:

- 8-bit up-counter
  - 8-bit modulo match limit
  - Software controllable periodic interrupt on match
- Three software selectable clock sources for input to prescaler with selectable binary-based and decimal-based divider values
  - 1-kHz internal low-power oscillator (LPO)
  - External clock (ERCLK)
  - 32-kHz internal clock (IRCLK)

### 13.1.2 Modes of Operation

This section defines the operation in stop, wait and background debug modes.

#### 13.1.2.1 Wait Mode

The RTC continues to run in wait mode if enabled before executing the appropriate instruction. Therefore, the RTC can bring the MCU out of wait mode if the real-time interrupt is enabled. For lowest possible current consumption, the RTC should be stopped by software if not needed as an interrupt source during wait mode.

#### 13.1.2.2 Stop Modes

The RTC continues to run in stop2 or stop3 mode if the RTC is enabled before executing the STOP instruction. Therefore, the RTC can bring the MCU out of stop modes with no external components, if the real-time interrupt is enabled.

The LPO clock can be used in stop2 and stop3 modes. ERCLK and IRCLK clocks are only available in stop3 mode.

Power consumption is lower when all clock sources are disabled, but in that case, the real-time interrupt cannot wake up the MCU from stop modes.

#### 13.1.2.3 Active Background Mode

The RTC suspends all counting during active background mode until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as the RTCMOD register is not written and the RTCPS and RTCLKS bits are not altered.

### 14.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. . An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note, because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

### 14.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general-purpose port I/O pin.

### 14.3.5.4 Single-Wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general-purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

## A.8 External Oscillator (XOSC) Characteristics

**Table A-8. Oscillator Electrical Specifications (Temperature Range = -40 to 125°C Ambient)**

Num	C	Rating	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Temp Rated <sup>2</sup>					
								Standard	AEC Grade 0				
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)											
		Low range (RANGE = 0)	$f_{lo}$	32	—	38.4	kHz	x	x				
		High range (RANGE = 1) FEE or FBE mode <sup>3</sup>	$f_{hi}$	1	—	5	MHz	x	x				
		High range (RANGE = 1, HGO = 1) FBELP mode	$f_{hi-hgo}$	1	—	16	MHz	x	x				
		High range (RANGE = 1, HGO = 0) FBELP mode	$f_{hi-lp}$	1	—	8	MHz	x	x				
2	—	Load capacitors	$C_1, C_2$	See crystal or resonator manufacturer's recommendation.									
3	—	Feedback resistor	$R_F$	—	10	—	M $\Omega$	x	x				
		Low range (32 kHz to 100 kHz)						—	1	—	x	x	
4	—	Series resistor	$R_S$	—	0	—	k $\Omega$	x	x				
		Low range, low gain (RANGE = 0, HGO = 0)						—	100	—	x	x	
		Low range, high gain (RANGE = 0, HGO = 1)						—	0	—	x	x	
		High range, low gain (RANGE = 1, HGO = 0)						—	0	—	x	x	
		High range, high gain (RANGE = 1, HGO = 1)						—	0	0	x	x	
		$\geq 8$ MHz						—	0	10	x	x	
4 MHz	—	0	20	x	x								
5	T	Crystal start-up time <sup>4</sup>		—	200	—	ms	x	x				
		Low range, low gain (RANGE = 0, HGO = 0)						$t_{CSTL-LP}$	—	400	—	x	x
		Low range, high gain (RANGE = 0, HGO = 1)						$t_{CSTL-HGO}$	—	5	—	x	x
		High range, low gain (RANGE = 1, HGO = 0) <sup>5</sup>						$t_{CSTH-LP}$	—	20	—	x	x
		High range, high gain (RANGE = 1, HGO = 1) <sup>4</sup>	$t_{CSTH-HGO}$	—	20	—	x	x					
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	$f_{extal}$	0.03125	—	5	MHz	x					
		FEE or FBE mode <sup>2</sup>						0	—	40	MHz	x	
		FBELP mode						0	—	36	MHz		x

<sup>1</sup> Typical data was characterized at 5.0 V, 25°C or is recommended value.

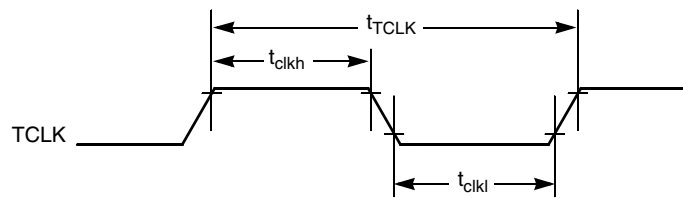
## A.12.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

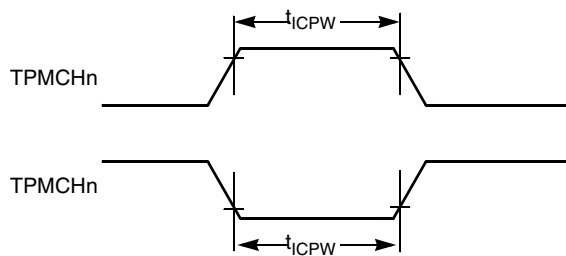
**Table A-14. TPM Input Timing**

Num	C	Rating	Symbol	Min	Max	Unit	Temp Rated <sup>1</sup>	
							Standard	AEC Grade 0
1	—	External clock frequency ( $1/t_{\text{TCLK}}$ )	$f_{\text{TCLK}}$	dc	$f_{\text{Bus}}/4$	MHz	x	x
2	—	External clock period	$t_{\text{TCLK}}$	4	—	$t_{\text{cyc}}$	x	x
3	—	External clock high time	$t_{\text{clkh}}$	1.5	—	$t_{\text{cyc}}$	x	x
4	—	External clock low time	$t_{\text{clkl}}$	1.5	—	$t_{\text{cyc}}$	x	x
5	—	Input capture pulse width	$t_{\text{ICPW}}$	1.5	—	$t_{\text{cyc}}$	x	x

<sup>1</sup> Electrical characteristics only apply to the temperature rated devices marked with x.



**Figure A-12. Timer External Clock**



**Figure A-13. Timer Input Capture Pulse**

