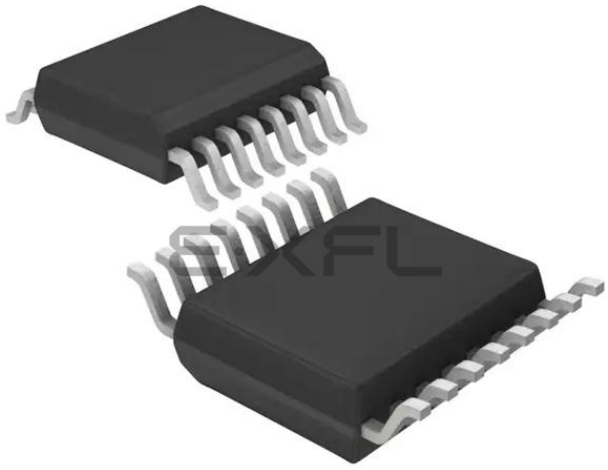

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg8e2mtgr

6.4.1 Edge Only Sensitivity 78
6.4.2 Edge and Level Sensitivity 78
6.4.3 Pull-up/Pull-down Resistors 79
6.4.4 Pin Interrupt Initialization 79
6.5 Pin Behavior in Stop Modes 79
6.6 Parallel I/O and Pin Control Registers 79
6.6.1 Port A Registers 80
6.6.2 Port B Registers 84
6.6.3 Port C Registers 88

Chapter 7
Central Processor Unit (S08CPUV2)

7.1 Introduction 91
7.1.1 Features 91
7.2 Programmer's Model and CPU Registers 92
7.2.1 Accumulator (A) 92
7.2.2 Index Register (H:X) 92
7.2.3 Stack Pointer (SP) 93
7.2.4 Program Counter (PC) 93
7.2.5 Condition Code Register (CCR) 93
7.3 Addressing Modes 94
7.3.1 Inherent Addressing Mode (INH) 95
7.3.2 Relative Addressing Mode (REL) 95
7.3.3 Immediate Addressing Mode (IMM) 95
7.3.4 Direct Addressing Mode (DIR) 95
7.3.5 Extended Addressing Mode (EXT) 95
7.3.6 Indexed Addressing Mode 95
7.4 Special Operations 96
7.4.1 Reset Sequence 97
7.4.2 Interrupt Sequence 97
7.4.3 Wait Mode Operation 98
7.4.4 Stop Mode Operation 98
7.4.5 BGND Instruction 98
7.5 HCS08 Instruction Set Summary 99

Chapter 8
5-V Analog Comparator (S08ACMPV2)

8.1 Introduction 111
8.1.1 ACMP Configuration Information 111
8.1.2 ACMP in Stop3 Mode 111
8.1.3 ACMP/TPM Configuration Information 111
8.1.4 Features 113

Table 3-2. Stop Mode Behavior

Peripheral	Mode	
	Stop2	Stop3
CPU	Off	Standby
RAM	Standby	Standby
FLASH	Off	Standby
Parallel Port Registers	Off	Standby
ADC	Off	Optionally On[1]
ACMP	Off	Optionally On[2]
BDM	Off[3]	Optionally On
ICS	Off	Optionally On[4]
IIC	Off	Standby
LVD/LVW	Off[5]	Optionally On
MTIM	Off	Standby
RTC	Optionally On	Optionally On
SCI	Off	Standby
SPI	Off	Standby
TPM	Off	Standby
Voltage Regulator	Standby	Optionally On[6]
XOSC	Off	Optionally On[7]
I/O Pins	States Held	States Held

1 Requires the asynchronous ADC clock and LVD to be enabled, else in standby.

2 Requires the LVD to be enabled when compare to internal bandgap reference option is enabled.

3 If ENBDM is set when entering stop2, the MCU will actually enter stop3.

4 IRCLKEN and IREFSTEN set in ICSC1, else in standby.

5 If LVDSE is set when entering stop2, the MCU will actually enter stop3.

6 Voltage regulator will be on if BDM is enabled or if LVD is enabled when entering stop3.

7 ERCLKEN and EREFSTEN set in ICSC2, else in standby. For high frequency range (RANGE in ICSC2 set) requires the LVD to also be enabled in stop3.

Chapter 4
Memory

4.1 MC9S08SG8 Memory Map

As shown in Figure 4-1, on-chip memory in the MC9S08SG8 series of MCUs consists of RAM, FLASH program memory for nonvolatile data storage, and I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers (0x0000 through 0x007F)
- High-page registers (0x1800 through 0x185F)
- Nonvolatile registers (0xFFB0 through 0xFFBF)

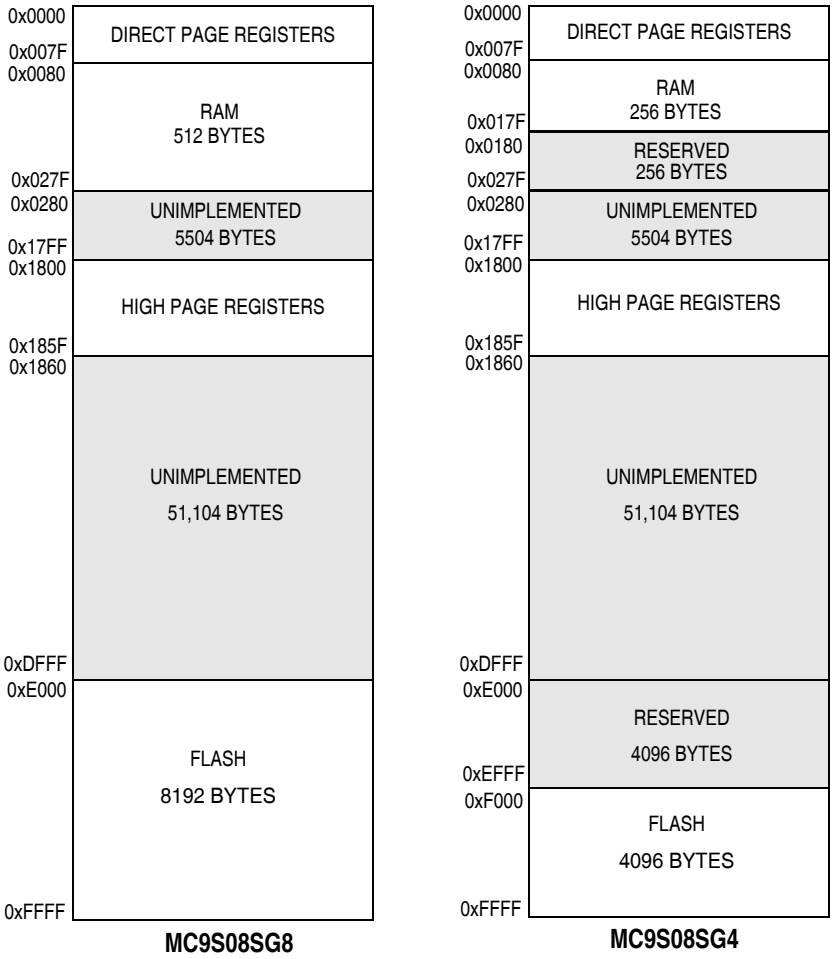


Figure 4-1. MC9S08SG8 Memory Map

4.5.3 Program and Erase Command Execution

The steps for executing any of the commands are listed below. The FCDIV register must be initialized and any error flags cleared before beginning command execution. The command execution steps are:

1. Write a data value to an address in the FLASH array. The address and data information from this write is latched into the FLASH interface. This write is a required first step in any command sequence. For erase and blank check commands, the value of the data is not important. For page erase commands, the address may be any address in the 512-byte page of FLASH to be erased. For mass erase and blank check commands, the address can be any address in the FLASH memory. Whole pages of 512 bytes are the smallest block of FLASH that may be erased.

   NOTE

   Do not program any byte in the FLASH more than once after a successful erase operation. Reprogramming bits to a byte that is already programmed is not allowed without first erasing the page in which the byte resides or mass erasing the entire FLASH memory. Programming without first erasing may disturb data stored in the FLASH.

2. Write the command code for the desired command to FCMD. The five valid commands are blank check (0x05), byte program (0x20), burst program (0x25), page erase (0x40), and mass erase (0x41). The command code is latched into the command buffer.
3. Write a 1 to the FCBEF bit in FSTAT to clear FCBEF and launch the command (including its address and data information).

A partial command sequence can be aborted manually by writing a 0 to FCBEF any time after the write to the memory array and before writing the 1 that clears FCBEF and launches the complete command. Aborting a command in this way sets the FACCERR access error flag, which must be cleared before starting a new command.

A strictly monitored procedure must be obeyed or the command will not be accepted. This minimizes the possibility of any unintended changes to the FLASH memory contents. The command complete flag (FCCF) indicates when a command is complete. The command sequence must be completed by clearing FCBEF to launch the command. Figure 4-2 is a flowchart for executing all of the commands except for burst programming. The FCDIV register must be initialized before using any FLASH commands. This must be done only once following a reset.

The status flag corresponding to the interrupt source must be acknowledged (cleared) before returning from the ISR. Typically, the flag is cleared at the beginning of the ISR so that if another interrupt is generated by this same source, it will be registered so it can be serviced after completion of the current ISR.

5.5.2 Interrupt Vectors, Sources, and Local Masks

Table 5-2 provides a summary of all interrupt sources. Higher-priority sources are located toward the bottom of the table. The high-order byte of the address for the interrupt service routine is located at the first address in the vector address column, and the low-order byte of the address for the interrupt service routine is located at the next higher address.

When an interrupt condition occurs, an associated flag bit becomes set. If the associated local interrupt enable is 1, an interrupt request is sent to the CPU. Within the CPU, if the global interrupt mask (I bit in the CCR) is 0, the CPU will finish the current instruction; stack the PCL, PCH, X, A, and CCR CPU registers; set the I bit; and then fetch the interrupt vector for the highest priority pending interrupt. Processing then continues in the interrupt service routine.

result of the conversion is transferred to ADCRH and ADCRL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADLSMP=0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADLSMP=1).

The maximum total conversion time for different conditions is summarized in Table 9-12.

Table 9-12. Total Conversion Time vs. Control Conditions

Conversion Type	ADICLK	ADLSMP	Max Total Conversion Time
Single or first continuous 8-bit	0x, 10	0	20 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit	0x, 10	0	23 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	0x, 10	1	40 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit	0x, 10	1	43 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	11	0	5 µs + 20 ADCK + 5 bus clock cycles
Single or first continuous 10-bit	11	0	5 µs + 23 ADCK + 5 bus clock cycles
Single or first continuous 8-bit	11	1	5 µs + 40 ADCK + 5 bus clock cycles
Single or first continuous 10-bit	11	1	5 µs + 43 ADCK + 5 bus clock cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	17 ADCK cycles
Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	20 ADCK cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}/11$	xx	1	37 ADCK cycles
Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}/11$	xx	1	40 ADCK cycles

The maximum total conversion time is determined by the clock source chosen and the divide ratio selected. The clock source is selectable by the ADICLK bits, and the divide ratio is specified by the ADIV bits. For example, in 10-bit mode, with the bus clock selected as the input clock source, the input clock divide-by-1 ratio selected, and a bus frequency of 8 MHz, then the conversion time for a single conversion is:

$$\text{Conversion time} = \frac{23 \text{ ADCK cyc}}{8 \text{ MHz}/1} + \frac{5 \text{ bus cyc}}{8 \text{ MHz}} = 3.5 \text{ µs}$$

$$\text{Number of bus cycles} = 3.5 \text{ µs} \times 8 \text{ MHz} = 28 \text{ cycles}$$

NOTE

The ADCK frequency must be between f_{ADCK} minimum and f_{ADCK} maximum to meet ADC specifications.

11.4.1.5 Repeated Start Signal

As shown in Figure 11-9, a repeated start signal is a start signal generated without first generating a stop signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

11.4.1.6 Arbitration Procedure

The IIC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case, the transition from master to slave mode does not generate a stop condition. Meanwhile, a status bit is set by hardware to indicate loss of arbitration.

11.4.1.7 Clock Synchronization

Because wire-AND logic is performed on the SCL line, a high-to-low transition on the SCL line affects all the devices connected on the bus. The devices start counting their low period and after a device's clock has gone low, it holds the SCL line low until the clock high state is reached. However, the change of low to high in this device clock may not change the state of the SCL line if another device clock is still within its low period. Therefore, synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time (see Figure 11-10). When all devices concerned have counted off their low period, the synchronized clock SCL line is released and pulled high. There is then no difference between the device clocks and the state of the SCL line and all the devices start counting their high periods. The first device to complete its high period pulls the SCL line low again.

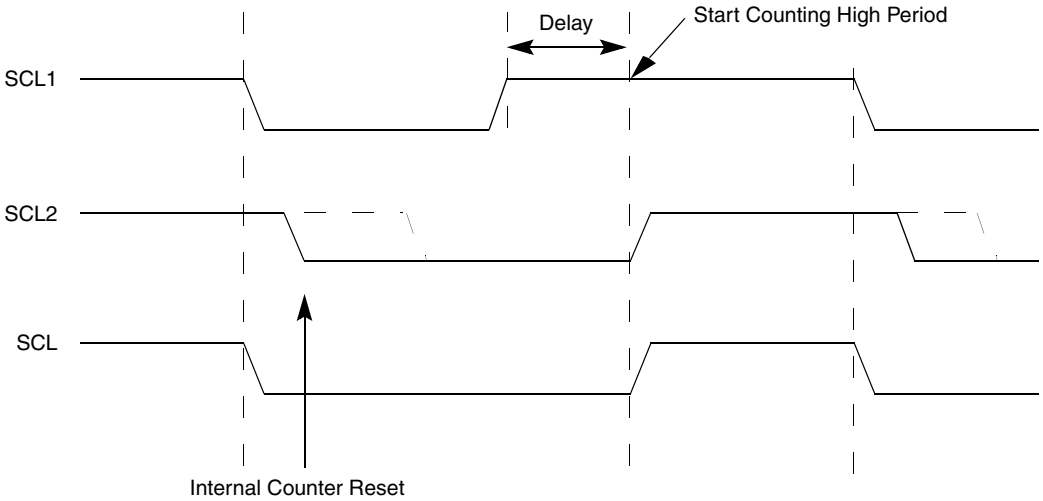


Figure 11-10. IIC Clock Synchronization

After a repeated start condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them are addressed because R/$\overline{W}$ = 1 (for 10-bit devices) or the 11110XX slave address (for 7-bit devices) does not match.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Sr	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 1	A3	Data	A	...	Data	A	P

Table 11-11. Master-Receiver Addresses a Slave-Transmitter with a 10-bit Address

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

11.4.3 General Call Address

General calls can be requested in 7-bit address or 10-bit address. If the GCAEN bit is set, the IIC matches the general call address as well as its own slave address. When the IIC responds to a general call, it acts as a slave-receiver and the IAAS bit is set after the address cycle. Software must read the IICD register after the first byte transfer to determine whether the address matches is its own slave address or a general call. If the value is 00, the match is a general call. If the GCAEN bit is clear, the IIC ignores any data supplied from a general call address by not issuing an acknowledgement.

11.5 Resets

The IIC is disabled after reset. The IIC cannot cause an MCU reset.

11.6 Interrupts

The IIC generates a single interrupt.

An interrupt from the IIC is generated when any of the events in Table 11-12 occur, provided the IICIE bit is set. The interrupt is driven by bit IICIF (of the IIC status register) and masked with bit IICIE (of the IIC control register). The IICIF bit must be cleared by software by writing a 1 to it in the interrupt routine. You can determine the interrupt type by reading the status register.

Table 11-12. Interrupt Summary

Interrupt Source	Status	Flag	Local Enable
Complete 1-byte transfer	TCF	IICIF	IICIE
Match of received calling address	IAAS	IICIF	IICIE
Arbitration Lost	ARBL	IICIF	IICIE

11.6.1 Byte Transfer Interrupt

The TCF (transfer complete flag) bit is set at the falling edge of the ninth clock to indicate the completion of byte transfer.

13.1.3 Block Diagram

The block diagram for the RTC module is shown in Figure 13-2.

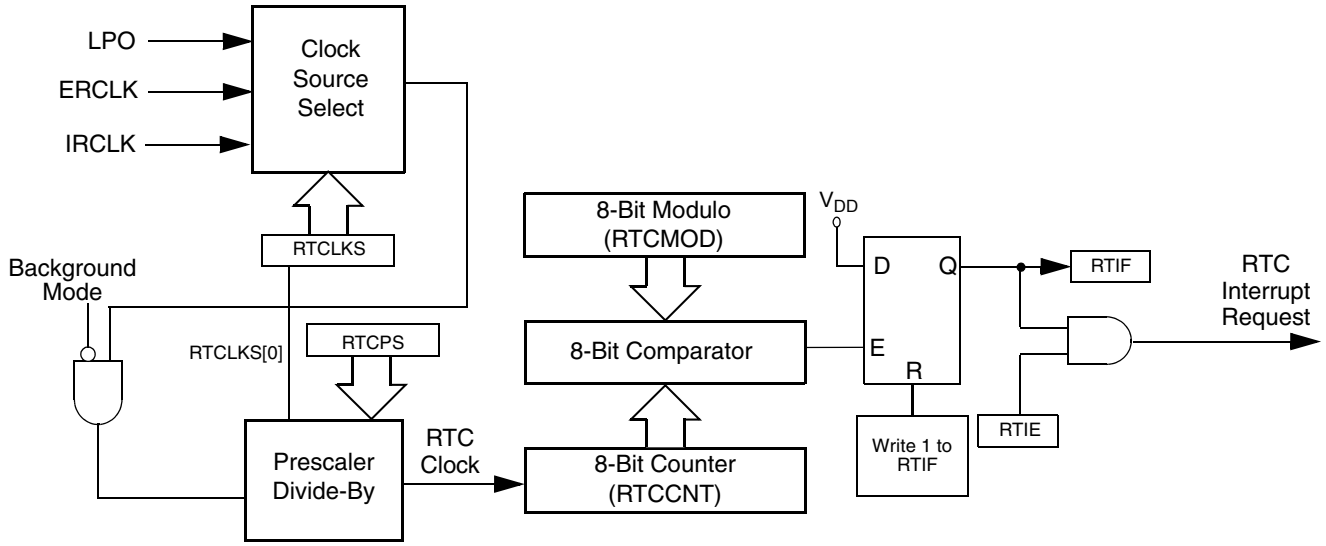


Figure 13-2. Real-Time Counter (RTC) Block Diagram

13.2 External Signal Description

The RTC does not include any off-chip signals.

13.3 Register Definition

The RTC includes a status and control register, an 8-bit counter register, and an 8-bit modulo register.

Refer to the direct-page register summary in the memory section of this document for the absolute address assignments for all RTC registers.This section refers to registers and control bits only by their names and relative address offsets.

Table 13-1 is a summary of RTC registers.

Table 13-1. RTC Register Summary

Name		7	6	5	4	3	2	1	0
RTCSC	R	RTIF	RTCLKS		RTIE	RTCPS			
	W								
RTCCNT	R	RTCCNT							
	W								
RTCMOD	R	RTCMOD							
	W								

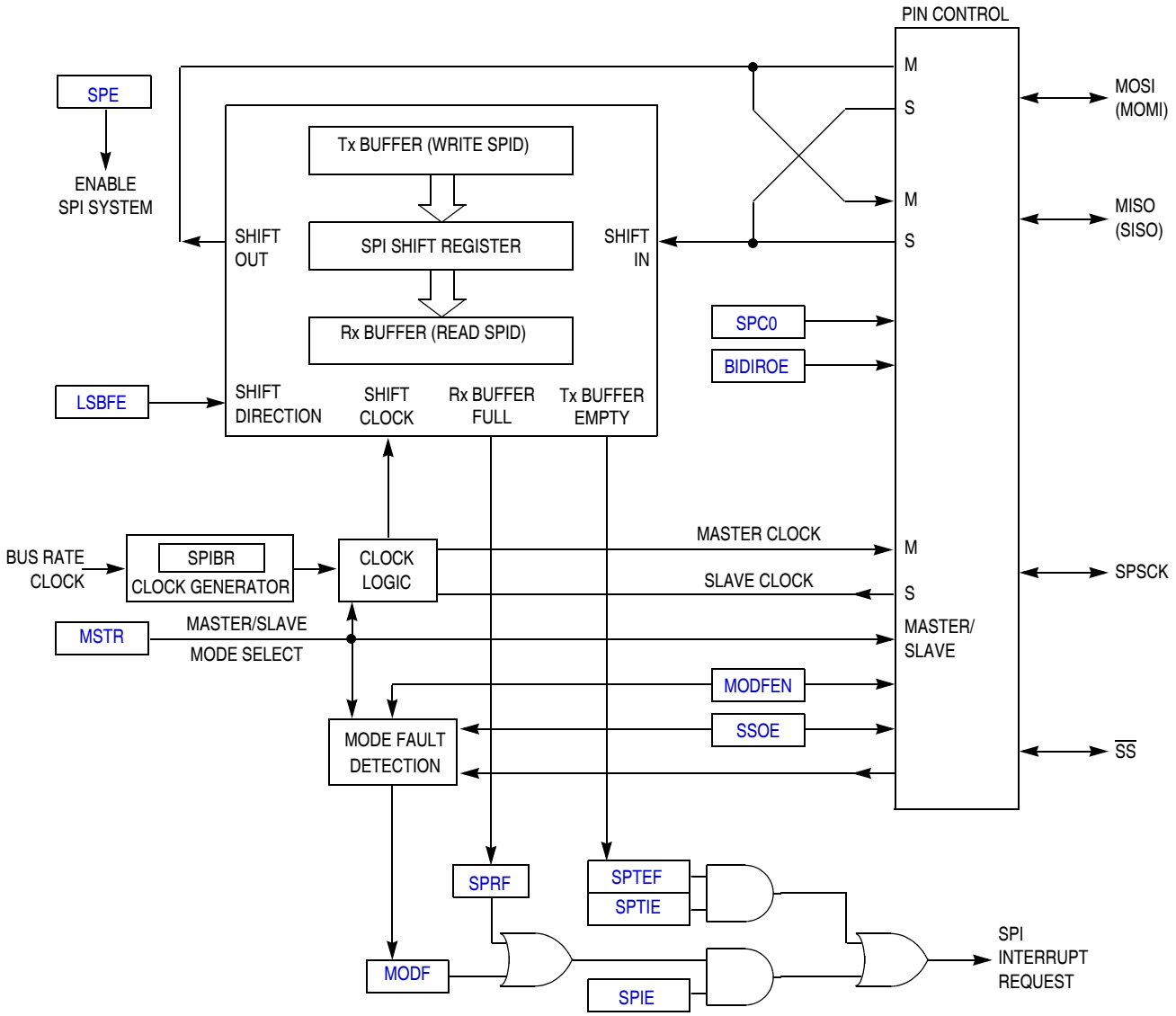


Figure 15-3. SPI Module Block Diagram

15.1.3 SPI Baud Rate Generation

As shown in Figure 15-4, the clock source for the SPI baud rate generator is the bus clock. The three prescale bits (SPPR2:SPPR1:SPPR0) choose a prescale divisor of 1, 2, 3, 4, 5, 6, 7, or 8. The three rate select bits (SPR2:SPR1:SPR0) divide the output of the prescaler stage by 2, 4, 8, 16, 32, 64, 128, or 256 to get the internal SPI master mode bit-rate clock.

MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

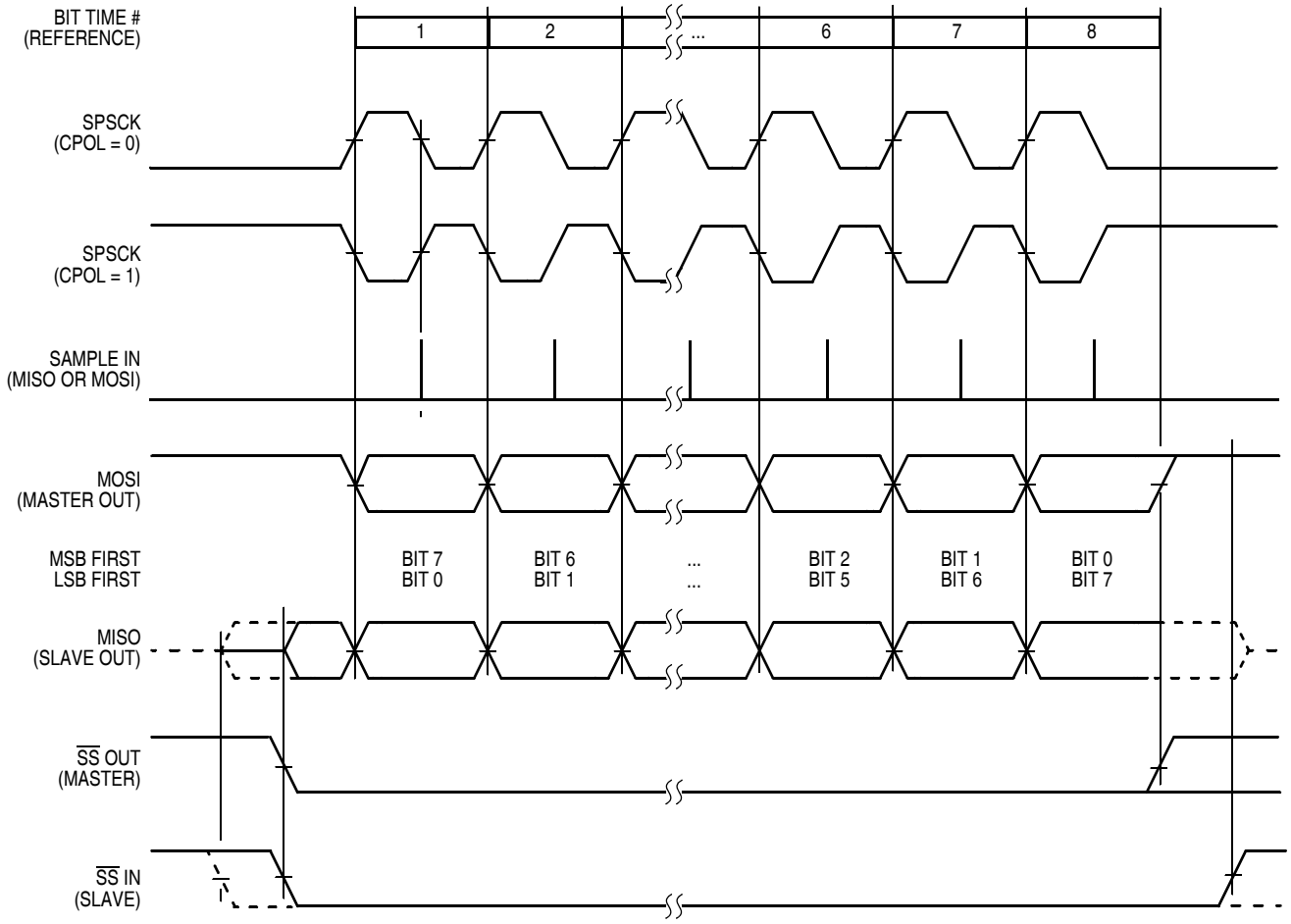


Figure 15-10. SPI Clock Formats (CPHA = 1)

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CHPA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers.

Figure 15-11 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected ($\overline{SS}$ IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting

16.1.5 Features

The TPM includes these distinctive features:

- One to eight channels:
  - Each channel may be input capture, output compare, or edge-aligned PWM
  - Rising-Edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs
- Module may be configured for buffered, center-aligned pulse-width-modulation (CPWM) on all channels
- Timer clock source selectable as prescaled bus clock, fixed system clock, or an external clock pin
  - Prescale taps for divide-by 1, 2, 4, 8, 16, 32, 64, or 128
  - Fixed system clock source are synchronized to the bus clock by an on-chip synchronization circuit
  - External clock pin may be shared with any timer channel pin or a separated input pin
- 16-bit free-running or modulo up/down count operation
- Timer system enable
- One interrupt per channel plus terminal count interrupt

16.1.6 Modes of Operation

In general, TPM channels may be independently configured to operate in input capture, output compare, or edge-aligned PWM modes. A control bit allows the whole TPM (all channels) to switch to center-aligned PWM mode. When center-aligned PWM mode is selected, input capture, output compare, and edge-aligned PWM functions are not available on any channels of this TPM module.

When the microcontroller is in active BDM background or BDM foreground mode, the TPM temporarily suspends all counting until the microcontroller returns to normal user operating mode. During stop mode, all system clocks, including the main oscillator, are stopped; therefore, the TPM is effectively disabled until clocks resume. During wait mode, the TPM continues to operate normally. Provided the TPM does not need to produce a real time reference or provide the interrupt source(s) needed to wake the MCU from wait mode, the user can save power by disabling TPM functions before entering wait mode.

- Input capture mode

  When a selected edge event occurs on the associated MCU pin, the current value of the 16-bit timer counter is captured into the channel value register and an interrupt flag bit is set. Rising edges, falling edges, any edge, or no edge (disable channel) may be selected as the active edge which triggers the input capture.
- Output compare mode

  When the value in the timer counter register matches the channel value register, an interrupt flag bit is set, and a selected output action is forced on the associated MCU pin. The output compare action may be selected to force the pin to zero, force the pin to one, toggle the pin, or ignore the pin (used for software timing functions).

Chapter 17
Development Support

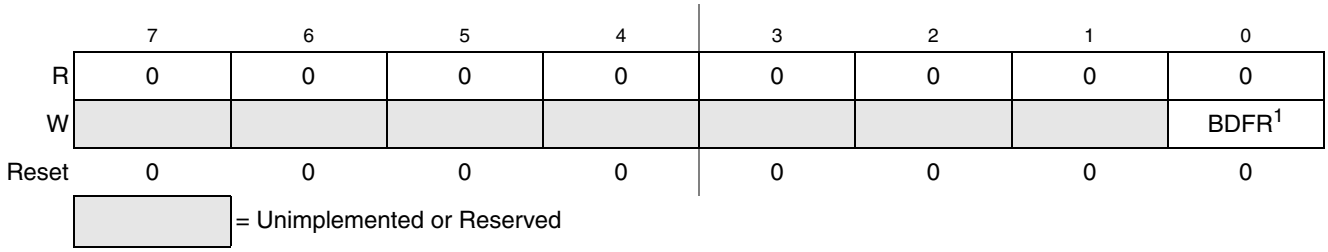
17.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip FLASH and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

17.1.1 Forcing Active Background

The method for forcing active background mode depends on the specific HCS08 derivative. For the MC9S08SG8, you can force active background after a power-on reset by holding the BKGD pin low as the device exits the reset condition. You can also force active background by driving BKGD low immediately after a serial background command that writes a one to the BDFR bit in the SBDFR register. Other causes of reset including an external pin reset or an internally generated error reset ignore the state of the BKGD pin and reset into normal user mode. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.



	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								BDFR[1]
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

1 BDFR is writable only through serial background mode debug commands, not from user programs.

Figure 17-6. System Background Debug Force Reset Register (SBDFR)

Table 17-3. SBDFR Register Field Description

Field	Description
0 BDFR	**Background Debug Force Reset** — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

17.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

17.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

A.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table A-6. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit	Temp Rated[2]	
									Standard	AEC Grade 0
1	—	Operating voltage	V_{DD}	—	2.7	—	5.5	V	x	x
2	C	Output high voltage — All I/O pins, low-drive strength	V_{OH}	5 V, I_{Load} = –4 mA	V_{DD} – 1.5	—	—	V	x	x
	P			5 V, I_{Load} = –2 mA	V_{DD} – 0.8	—	—		x	x
	C			3 V, I_{Load} = –1 mA	V_{DD} – 0.8	—	—		x	x
	C			5 V, I_{Load} = –20 mA	V_{DD} – 1.5	—	—		x	x
	P	Output high voltage — All I/O pins, high-drive strength		5 V, I_{Load} = –10 mA	V_{DD} – 0.8	—	—		x	x
	C			3 V, I_{Load} = –5 mA	V_{DD} – 0.8	—	—		x	x
3	C	Output high current — Max total I_{OH} for all ports	I_{OHT}	$V_{OUT} < V_{DD}$	0	—	–100	mA	x	
							–50			x
4	C	Output low voltage — All I/O pins, low-drive strength	V_{OL}	5 V, I_{Load} = 4 mA	—	—	1.5	V	x	x
	P			5 V, I_{Load} = 2 mA	—	—	0.8		x	x
	C			3 V, I_{Load} = 1 mA	—	—	0.8		x	x
	C			5 V, I_{Load} = 20 mA	—	—	1.5		x	x
	P	Output low voltage — All I/O pins, high-drive strength		5 V, I_{Load} = 10 mA	—	—	0.8		x	x
	C			3 V, I_{Load} = 5 mA	—	—	0.8		x	x
5	C	Output low current — Max total I_{OL} for all ports	I_{OLT}	$V_{OUT} > V_{SS}$	0	—	100	mA	x	
							50			x
6	P	Input high voltage; all digital inputs	V_{IH}	5V	0.65 x V_{DD}	—	—	V	x	x
	C			3V	0.7 x V_{DD}	—	—		x	x
7	P	Input low voltage; all digital inputs	V_{IL}	5V	—	—	0.35 x V_{DD}	V	x	x
	C			3V	—	—	0.35 x V_{DD}		x	x
8	C	Input hysteresis	V_{hys}		0.06 x V_{DD}			V	x	x
									x	x
9	P	Input leakage current (per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA	x	
				temperature > 125 °C		—	2			x
10	P	Hi-Z (off-state) leakage current (per pin) — input/output port pins	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS},	—	0.1	1	µA	x	
		PTB6/SDA/XTAL, $\overline{\text{RESET}}$		V_{In} = V_{DD} or V_{SS}	—	0.2	2	µA	x	
		input/output port pins		V_{In} = V_{DD} or V_{SS} temperature > 125 °C	—	0.2	2	µA		x

Table A-6. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit	Temp Rated[2]	
									Standard	AEC Grade 0
11	P	Pullup or Pulldown[3] resistors; when enabled I/O pins	R_{PU},R_{PD}		17	37	52	kΩ	x	x
	C	$\overline{\text{RESET}}$[4]	R_{PU}		17	37	52	kΩ	x	x
12	D	DC injection current [5, 6, 7, 8] Single pin limit	I_{IC}	$V_{IN} > V_{DD}$	0	—	2	mA	x	x
				$V_{IN} < V_{SS}$	0	—	–0.2	mA	x	x
		Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA	x	x
				$V_{IN} < V_{SS}$	0	—	–5	mA	x	x
13	D	Input Capacitance, all pins	C_{In}		—	—	8	pF	x	x
14	D	RAM retention voltage	V_{RAM}		—	0.6	1.0	V	x	x
15	D	POR re-arm voltage[9]	V_{POR}		0.9	1.4	2.0	V	x	x
16	D	POR re-arm time[10]	t_{POR}		10	—	—	µs	x	x
17	P	Low-voltage detection threshold — high range V_{DD} falling	V_{LVD1}		3.9 3.88	4.0 4.0	4.1 4.12	V	x	x
		V_{DD} rising			4.0 3.98	4.1 4.1	4.2 4.22		x	x
18	P	Low-voltage detection threshold — low range[11, 12] V_{DD} falling V_{DD} rising	V_{LVD0}		2.48 2.54	2.56 2.62	2.64 2.70	V	x x	x x
19	P	Low-voltage warning threshold — high range 1 V_{DD} falling	V_{LVW3}		4.5 4.48	4.6 4.6	4.7 4.72	V	x	x
		V_{DD} rising			4.6 4.58	4.7 4.7	4.8 4.82		x	x
20	P	Low-voltage warning threshold — high range 0 V_{DD} falling	V_{LVW2}		4.2 4.18	4.3 4.3	4.4 4.42	V	x	x
		V_{DD} rising			4.3 4.28	4.4 4.4	4.5 4.52		x	x
21	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}		2.84 2.90	2.92 2.98	3.00 3.06	V	x x	x x
22	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}		2.66 2.72	2.74 2.80	2.82 2.88	V	x x	x x

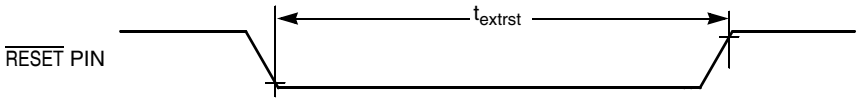


Figure A-10. Reset Timing

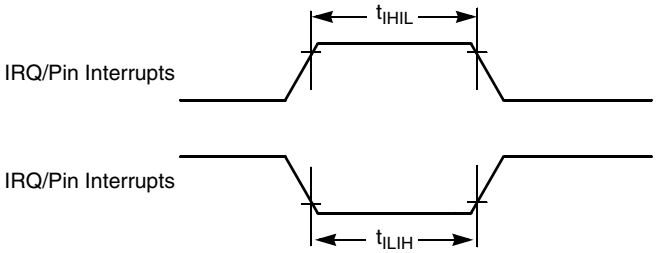


Figure A-11. IRQ/Pin Interrupt Timing

A.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

A.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table A-17. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level (Max)	Unit	Temp Rated[1]	
							Standard	AEC Grade 0
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5 V T_A = +25°C package type 16-TSSOP	0.15 – 50 MHz	4 MHz crystal 16 MHzbus	0	dBμV	x	x
			50 – 150 MHz		0		x	x
			150 – 500 MHz		–6		x	x
			500 – 1000 MHz		–9		x	x
			IEC Level		N	—	x	x
			SAE Level		1	—	x	x

[1] Electrical characteristics only apply to the temperature rated devices marked with x.

B.2 Mechanical Drawings

The following pages are mechanical specifications for MC9S08SG8 package options. See Table B-2 for the document number for each package type.

Table B-2. Package Information

Pin Count	Type	Designator	Document No.
20	TSSOP	TJ	98ASH70169A
16	TSSOP	TG	98ASH70247A
8	NB SOIC	SC	98ASB42564B