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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sl8f1ctjr

Chapter 7
Central Processor Unit (S08CPUV2)

Chapter 8
5-V Analog Comparator (S08ACMPV2)

Chapter 9
Analog-to-Digital Converter (S08ADCV1)

Chapter 10
Internal Clock Source (S08ICSV2)

Chapter 11
Inter-Integrated Circuit (S08IICV2)

Table 4-3. High-Page Register Summary (Sheet 2 of 2)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x1845	**PTAPS**	0	0	0	0	PTAPS3	PTAPS2	PTAPS1	PTAPS0
0x1846	**PTAES**	0	0	0	0	PTAES3	PTAES2	PTAES1	PTAES0
0x1847	Reserved	—	—	—	—	—	—	—	—
0x1848	**PTBPE**	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
0x1849	**PTBSE**	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0
0x184A	**PTBDS**	PTBDS7	PTBDS6	PTBDS5	PTBDS4	PTBDS3	PTBDS2	PTBDS1	PTBDS0
0x184B	Reserved	—	—	—	—	—	—	—	—
0x184C	**PTBSC**	0	0	0	0	PTBIF	PTBACK	PTBIE	PTBMOD
0x184D	**PTBPS**	0	0	0	0	PTBPS3	PTBPS2	PTBPS1	PTBPS0
0x184E	**PTBES**	0	0	0	0	PTBES3	PTBES2	PTBES1	PTBES0
0x184F	Reserved	—	—	—	—	—	—	—	—
0x1850	**PTCPE**	0	0	0	0	PTCPE3	PTCPE2	PTCPE1	PTCPE0
0x1851	**PTCSE**	0	0	0	0	PTCSE3	PTCSE2	PTCSE1	PTCSE0
0x1852	**PTCDS**	0	0	0	0	PTCDS3	PTCDS2	PTCDS1	PTCDS0
0x1853	**GNGC**	GNGPS7	GNGPS6	GNGPS5	GNGPS4	GNGPS3	GNGPS2	GNGPS1	GNGEN
0x1854–0x185F	Reserved	—	—	—	—	—	—	—	—

4.5.3   Program and Erase Command Execution

The steps for executing any of the commands are listed below. The FCDIV register must be initialized and any error flags cleared before beginning command execution. The command execution steps are:

1. Write a data value to an address in the FLASH array. The address and data information from this write is latched into the FLASH interface. This write is a required first step in any command sequence. For erase and blank check commands, the value of the data is not important. For page erase commands, the address may be any address in the 512-byte page of FLASH to be erased. For mass erase and blank check commands, the address can be any address in the FLASH memory. Whole pages of 512 bytes are the smallest block of FLASH that may be erased.

NOTE

Do not program any byte in the FLASH more than once after a successful erase operation. Reprogramming bits to a byte that is already programmed is not allowed without first erasing the page in which the byte resides or mass erasing the entire FLASH memory. Programming without first erasing may disturb data stored in the FLASH.

2. Write the command code for the desired command to FCMD. The five valid commands are blank check (0x05), byte program (0x20), burst program (0x25), page erase (0x40), and mass erase (0x41). The command code is latched into the command buffer.

3. Write a 1 to the FCBEF bit in FSTAT to clear FCBEF and launch the command (including its address and data information).

A partial command sequence can be aborted manually by writing a 0 to FCBEF any time after the write to the memory array and before writing the 1 that clears FCBEF and launches the complete command. Aborting a command in this way sets the FACCERR access error flag, which must be cleared before starting a new command.

A strictly monitored procedure must be obeyed or the command will not be accepted. This minimizes the possibility of any unintended changes to the FLASH memory contents. The command complete flag (FCCF) indicates when a command is complete. The command sequence must be completed by clearing FCBEF to launch the command. Figure 4-2 is a flowchart for executing all of the commands except for burst programming. The FCDIV register must be initialized before using any FLASH commands. This must be done only once following a reset.

the MCU secure. During development, whenever the FLASH is erased, it is good practice to immediately program the SEC00 bit to 0 in NVOPT so SEC01:SEC00 = 1:0. This would allow the MCU to remain unsecured after a subsequent reset.

The on-chip debug module cannot be enabled while the MCU is secure. The separate background debug controller can still be used for background memory access commands of unsecured resources.

A user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. If the nonvolatile KEYEN bit in NVOPT/FOPT is 0, the backdoor key is disabled and there is no way to disengage security without completely erasing all FLASH locations. If KEYEN is 1, a secure user program can temporarily disengage security by:

1. Writing 1 to KEYACC in the FCNFG register. This makes the FLASH module interpret writes to the backdoor comparison key locations (NVBACKKEY through NVBACKKEY+7) as values to be compared against the key rather than as the first step in a FLASH program or erase command.

2. Writing the user-entered key values to the NVBACKKEY through NVBACKKEY+7 locations. These writes must be done in order starting with the value for NVBACKKEY and ending with NVBACKKEY+7. STHX should not be used for these writes because these writes cannot be done on adjacent bus cycles. User software normally would get the key codes from outside the MCU system through a communication interface such as a serial I/O.

3. Writing 0 to KEYACC in the FCNFG register. If the 8-byte key that was just written matches the key stored in the FLASH locations, SEC01:SEC00 are automatically changed to 1:0 and security will be disengaged until the next reset.

The security key can be written only from secure memory (either RAM or FLASH), so it cannot be entered through background commands without the cooperation of a secure user program.

The backdoor comparison key (NVBACKKEY through NVBACKKEY+7) is located in FLASH memory locations in the nonvolatile register space so users can program these locations exactly as they would program any other FLASH memory location. The nonvolatile registers are in the same 512-byte block of FLASH as the reset and interrupt vectors, so block protecting that space also block protects the backdoor comparison key. Block protects cannot be changed from user application programs, so if the vector space is block protected, the backdoor security key mechanism cannot permanently change the block protect, security settings, or the backdoor key.

Security can always be disengaged through the background debug interface by taking these steps:

1. Disable any block protections by writing FPROT. FPROT can be written only with background debug commands, not from application software.

2. Mass erase FLASH if necessary.

3. Blank check FLASH. Provided FLASH is completely erased, security is disengaged until the next reset.

   To avoid returning to secure mode after the next reset, program NVOPT so SEC01:SEC00 = 1:0.

4.7 FLASH Registers and Control Bits

The FLASH module has nine 8-bit registers in the high-page register space, two locations (NVOPT, NVPROT) in the nonvolatile register space in FLASH memory are copied into corresponding high-page

Table 5-2. Vector Summary

Vector Priority	Vector Number	Address (High/Low)	Vector Name	Module	Source	Enable	Description
Lowest	31	0xFFC0/0xFFC1	—	—	—	—	—
	30	0xFFC2/0xFFC3	Vacmp	ACMP	ACF	ACIE	Analog comparator
	29	0xFFC4/0xFFC5	—	—	—	—	—
	28	0xFFC6/0xFFC7	—	—	—	—	—
	27	0xFFC8/0xFFC9	—	—	—	—	—
	26	0xFFCA/0xFFCB	Vmtim	MTIM	TOF	TOIE	MTIM overflow
	25	0xFFCC/0xFFCD	Vrtc	RTC	RTIF	RTIE	Real-time interrupt
	24	0xFFCE/0xFFCF	Viic	IIC	IICIF	IICIE	IIC control
	23	0xFFD0/0xFFD1	Vadc	ADC	COCO	AIEN	ADC
	22	0xFFD2/0xFFD3	—	—	—	—	—
	21	0xFFD4/0xFFD5	Vportb	Port B	PTBIF	PTBIE	Port B Pins
	20	0xFFD6/0xFFD7	Vporta	Port A	PTAIF	PTAIE	Port A Pins
	19	0xFFD8/0xFFD9	—	—	—	—	—
	18	0xFFDA/0xFFDB	Vscitx	SCI	TDRE, TC	TIE, TCIE	SCI transmit
	17	0xFFDC/0xFFDD	Vscirx	SCI	IDLE, RDRF, LBKDIF, RXEDGIF	ILIE, RIE, LBKDIE, RXEDGIE	SCI receive
	16	0xFFDE/0xFFDF	Vscierr	SCI	OR, NF, FE, PF	ORIE, NFIE, FEIE, PFIE	SCI error
	15	0xFFE0/0xFFE1	Vspi	SPI	SPIF, MODF, SPTEF	SPIE, SPIE, SPTIE	SPI
	14	0xFFE2/0xFFE3	Vtpm2ovf	TPM2	TOF	TOIE	TPM2 overflow
	13	0xFFE4/0xFFE5	Vtpm2ch1	TPM2	CH1F	CH1IE	TPM2 channel 1
	12	0xFFE6/0xFFE7	Vtpm2ch0	TPM2	CH0F	CH0IE	TPM2 channel 0
	11	0xFFE8/0xFFE9	Vtpm1ovf	TPM1	TOF	TOIE	TPM1 overflow
	10	0xFFEA/0xFFEB	—	—	—	—	—
	9	0xFFEC/0xFFED	—	—	—	—	—
	8	0xFFEE/0xFFEF	—	—	—	—	—
	7	0xFFF0/0xFFF1	—	—	—	—	—
	6	0xFFF2/0xFFF3	Vtpm1ch1	TPM1	CH1F	CH1IE	TPM1 channel 1
	5	0xFFF4/0xFFF5	Vtpm1ch0	TPM1	CH0F	CH0IE	TPM1 channel 0
	4	0xFFF6/0xFFF7	—	—	—	—	—
	3	0xFFF8/0xFFF9	Vlvd	System control	LVWF	LVWIE	Low-voltage warning
	2	0xFFFA/0xFFFB	—	—	—	—	—
	1	0xFFFC/0xFFFD	Vswi	Core	SWI Instruction	—	Software interrupt
Highest	0	0xFFFE/0xFFFF	Vreset	System control	COP, LVD, $\overline{\text{RESET}}$ pin, Illegal opcode, Illegal address	COPT LVDRE — — —	Watchdog timer Low-voltage detect External pin Illegal opcode Illegal address

5.7.1 System Reset Status Register (SRS)

This high page register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to BDFR in the SBDFR register, none of the status bits in SRS will be set. Writing any value to this register address causes a COP reset when the COP is enabled except the values 0x55 and 0xAA. Writing a 0x55-0xAA sequence to this address clears the COP watchdog timer without affecting the contents of this register. The reset state of these bits depends on what caused the MCU to reset.

	7	6	5	4	3	2	1	0
R	POR	PIN	COP	ILOP	ILAD	0	LVD	0
W	Writing 0x55, 0xAA to SRS address clears COP watchdog timer.							
POR:	1	0	0	0	0	0	1	0
LVR:	u[1]	0	0	0	0	0	1	0
Any other reset:	0	Note[2]	Note[2]	Note[2]	Note[2]	0	0	0

[1] u = unaffected

[2] Any of these reset sources that are active at the time of reset entry will cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset entry will be cleared.

Figure 5-2. System Reset Status (SRS)

Table 5-3. SRS Register Field Descriptions

Field	Description
7 POR	**Power-On Reset** — Reset was caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVR) status bit is also set to indicate that the reset occurred while the internal supply was below the LVR threshold. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	**External Reset Pin** — Reset was caused by an active-low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 COP	**Computer Operating Properly (COP) Watchdog** — Reset was caused by the COP watchdog timer timing out. This reset source can be blocked by COPT bits = 0:0. 0 Reset not caused by COP timeout. 1 Reset caused by COP timeout.
4 ILOP	**Illegal Opcode** — Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.

Chapter 6
Parallel Input/Output Control

This section explains software controls related to parallel input/output (I/O) and pin control. The MC9S08SG8 has three parallel I/O ports which include a total of 16 I/O pins. See Chapter 2, "Pins and Connections," for more information about pin assignments and external hardware considerations of these pins.

Many of these pins are shared with on-chip peripherals such as timer systems, communication systems, or pin interrupts as shown in Table 2-1. The peripheral modules have priority over the general-purpose I/O functions so that when a peripheral is enabled, the I/O functions associated with the shared pins are disabled.

After reset, the shared peripheral functions are disabled and the pins are configured as inputs (PTxDDn = 0). The pin control functions for each pin are configured as follows: slew rate disabled (PTxSEn = 0), low drive strength selected (PTxDSn = 0), and internal pull-ups disabled (PTxPEn = 0).

NOTE

Not all general-purpose I/O pins are available on all packages. To avoid extra current drain from floating input pins, the user's reset initialization routine in the application program must either enable on-chip pull-up devices or change the direction of unconnected pins to outputs so the pins do not float.

6.1 Port Data and Data Direction

Reading and writing of parallel I/Os are performed through the port data registers. The direction, either input or output, is controlled through the port data direction registers. The parallel I/O port function for an individual pin is illustrated in the block diagram shown in Figure 6-1.

The data direction control bit (PTxDDn) determines whether the output buffer for the associated pin is enabled, and also controls the source for port data register reads. The input buffer for the associated pin is always enabled unless the pin is enabled as an analog function or is an output-only pin.

When a shared digital function is enabled for a pin, the output buffer is controlled by the shared function. However, the data direction register bit will continue to control the source for reads of the port data register.

When a shared analog function is enabled for a pin, both the input and output buffers are disabled. A value of 0 is read for any port data bit where the bit is an input (PTxDDn = 0) and the input buffer is disabled. In general, whenever a pin is shared with both an alternate digital function and an analog function, the analog function has priority such that if both the digital and analog functions are enabled, the analog function controls the pin.
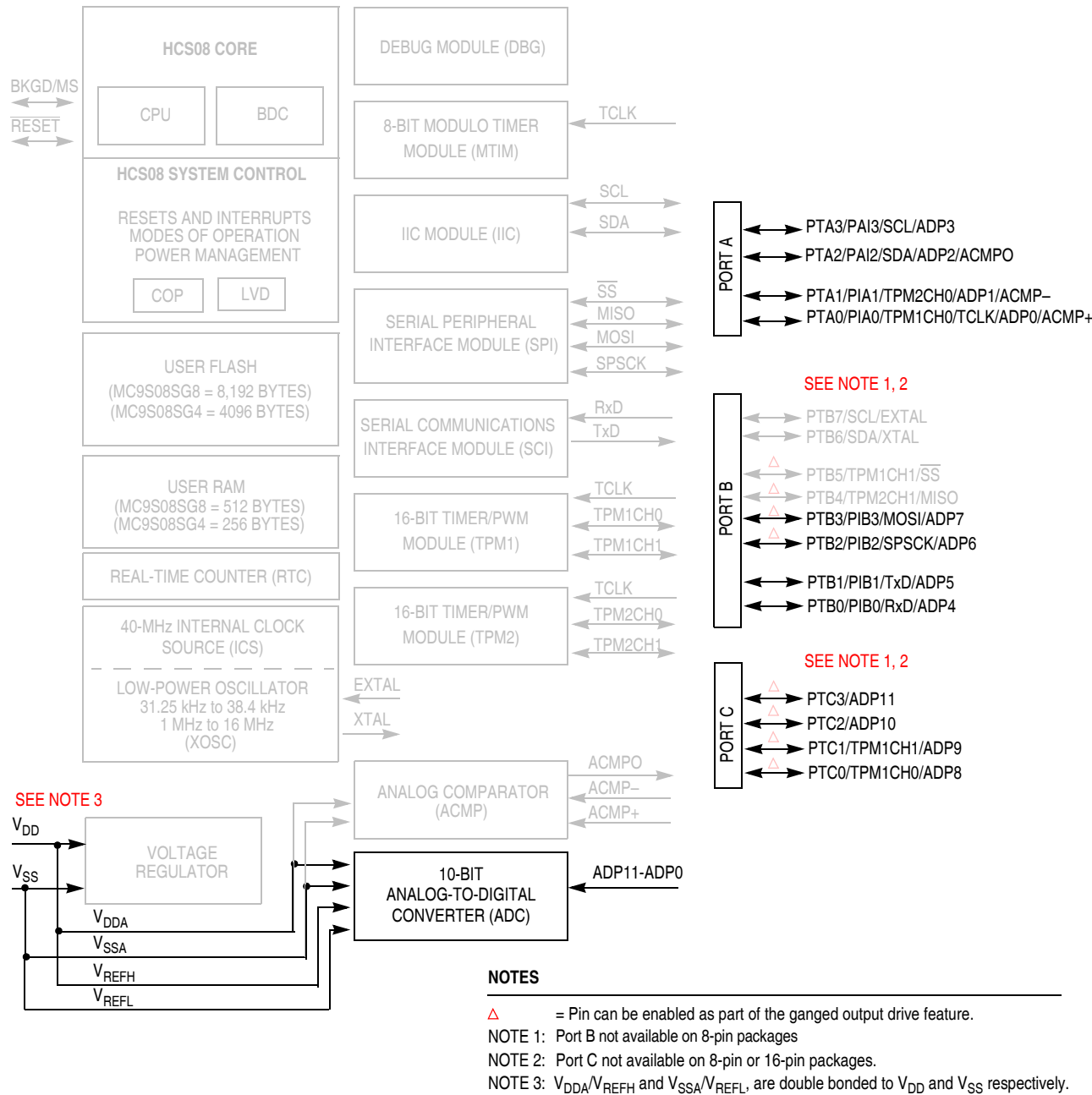
Figure 9-1. MC9S08SG8 Block Diagram with ADC Module Highlighted

NOTES

△ = Pin can be enabled as part of the ganged output drive feature.

NOTE 1: Port B not available on 8-pin packages

NOTE 2: Port C not available on 8-pin or 16-pin packages.

NOTE 3: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL}, are double bonded to V_{DD} and V_{SS} respectively.

- Average the result by converting the analog input many times in succession and dividing the sum of the results. Four samples are required to eliminate the effect of a 1LSB, one-time error.
- Reduce the effect of synchronous noise by operating off the asynchronous clock (ADACK) and averaging. Noise that is synchronous to ADCK cannot be averaged out.

9.6.2.4   Code Width and Quantization Error

The ADC quantizes the ideal straight-line transfer function into 1024 steps (in 10-bit mode). Each step ideally has the same height (1 code) and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N bit converter (in this case N can be 8 or 10), defined as 1LSB, is:

$$1LSB = (V_{REFH} - V_{REFL}) / 2^N \qquad \textit{Eqn. 9-2}$$

There is an inherent quantization error due to the digitization of the result. For 8-bit or 10-bit conversions the code will transition when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2LSB in 8- or 10-bit mode. As a consequence, however, the code width of the first ($000) conversion is only 1/2LSB and the code width of the last ($FF or $3FF) is 1.5LSB.

9.6.2.5   Linearity Errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system should be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error (E_{ZS}) (sometimes called offset) — This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2LSB). Note, if the first conversion is $001, then the difference between the actual $001 code width and its ideal (1LSB) is used.
- Full-scale error (E_{FS}) — This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5LSB). Note, if the last conversion is $3FE, then the difference between the actual $3FE code width and its ideal (1LSB) is used.
- Differential non-linearity (DNL) — This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.
- Integral non-linearity (INL) — This error is defined as the highest-value the (absolute value of the) running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE) — This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function, and therefore includes all forms of error.

9.6.2.6   Code Jitter, Non-Monotonicity and Missing Codes

Analog-to-digital converters are susceptible to three special forms of error. These are code jitter, non-monotonicity, and missing codes.

Code jitter is when, at certain points, a given input voltage converts to one of two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the

converter yields the lower code (and vice-versa). However, even very small amounts of system noise can cause the converter to be indeterminate (between two codes) for a range of input voltages around the transition voltage. This range is normally around ±1/2 LSB and will increase with noise. This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Section 9.6.2.3 will reduce this error.

Non-monotonicity is defined as when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values which are never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and to have no missing codes.

10.1.2 Features

Key features of the ICS module follow. For device specific information, refer to the ICS Characteristics in the Electricals section of the documentation.

- Frequency-locked loop (FLL) is trimmable for accuracy
  - 0.2% resolution using internal 32kHz reference
  - 1.5% deviation over voltage and temperature using internal 32kHz reference
- Internal or external reference clocks up to 5MHz can be used to control the FLL
  - 3 bit select for reference divider is provided
- Internal reference clock has 9 trim bits available
- Internal or external reference clocks can be selected as the clock source for the MCU
- Whichever clock is selected as the source can be divided down
  - 2 bit select for clock divider is provided
    - Allowable dividers are: 1, 2, 4, 8
    - BDC clock is provided as a constant divide by 2 of the DCO output
- Control signals for a low power oscillator as the external reference clock are provided
  - HGO, RANGE, EREFS, ERCLKEN, EREFSTEN
- FLL Engaged Internal mode is automatically selected out of reset

10.1.3 Block Diagram

Figure 10-2 is the ICS block diagram.

Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

11.3.1 IIC Address Register (IICA)

	7	6	5	4	3	2	1	0
R	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved
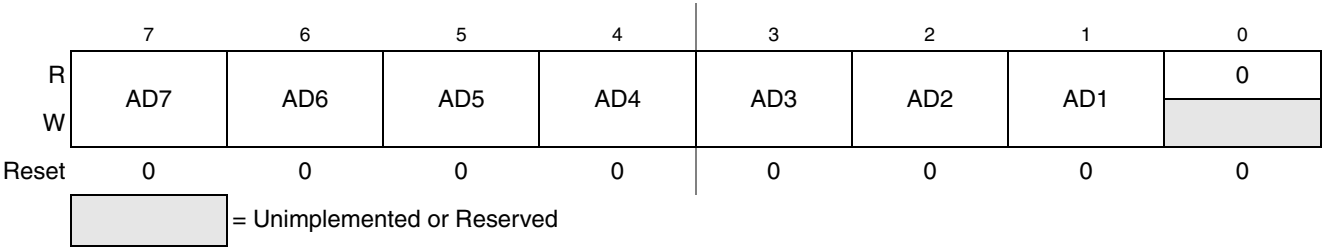
Figure 11-3. IIC Address Register (IICA)

Table 11-2. IICA Field Descriptions

Field	Description
7–1 AD[7:1]	**Slave Address.** The AD[7:1] field contains the slave address to be used by the IIC module. This field is used on the 7-bit address scheme and the lower seven bits of the 10-bit address scheme.

11.3.2 IIC Frequency Divider Register (IICF)

	7	6	5	4	3	2	1	0
R	MULT		ICR					
W								
Reset	0	0	0	0	0	0	0	0
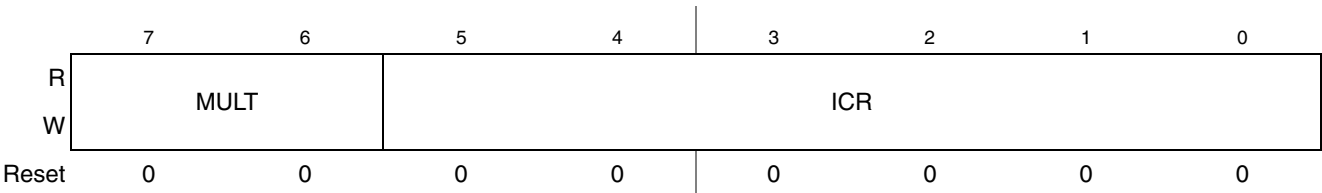
Figure 11-4. IIC Frequency Divider Register (IICF)

11.7 Initialization/Application Information

Module Initialization (Slave)

1. Write: IICC2
   — to enable or disable general call
   — to select 10-bit or 7-bit addressing mode
2. Write: IICA
   — to set the slave address
3. Write: IICC1
   — to enable IIC and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in Figure 11-12

Module Initialization (Master)

1. Write: IICF
   — to set the IIC baud rate (example provided in this chapter)
2. Write: IICC1
   — to enable IIC and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in Figure 11-12
5. Write: IICC1
   — to enable TX

Register Model

IICA	AD[7:1]						0

When addressed as a slave (in slave mode), the module responds to this address

IICF	MULT	ICR

Baud rate = BUSCLK / (2 x MULT x (SCL DIVIDER))

IICC1	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0

Module configuration

IICS	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK

Module status flags

IICD	DATA

Data register; Write to transmit IIC data read to read IIC data

IICC2	GCAEN	ADEXT	0	0	0	AD10	AD9	AD8

Address configuration

Figure 11-11. IIC Module Quick Start

NOTES

△   = Pin can be enabled as part of the ganged output drive feature.
NOTE 1: Port B not available on 8-pin packages
NOTE 2: Port C not available on 8-pin or 16-pin packages.
NOTE 3: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL}, are double bonded to V_{DD} and V_{SS} respectively.
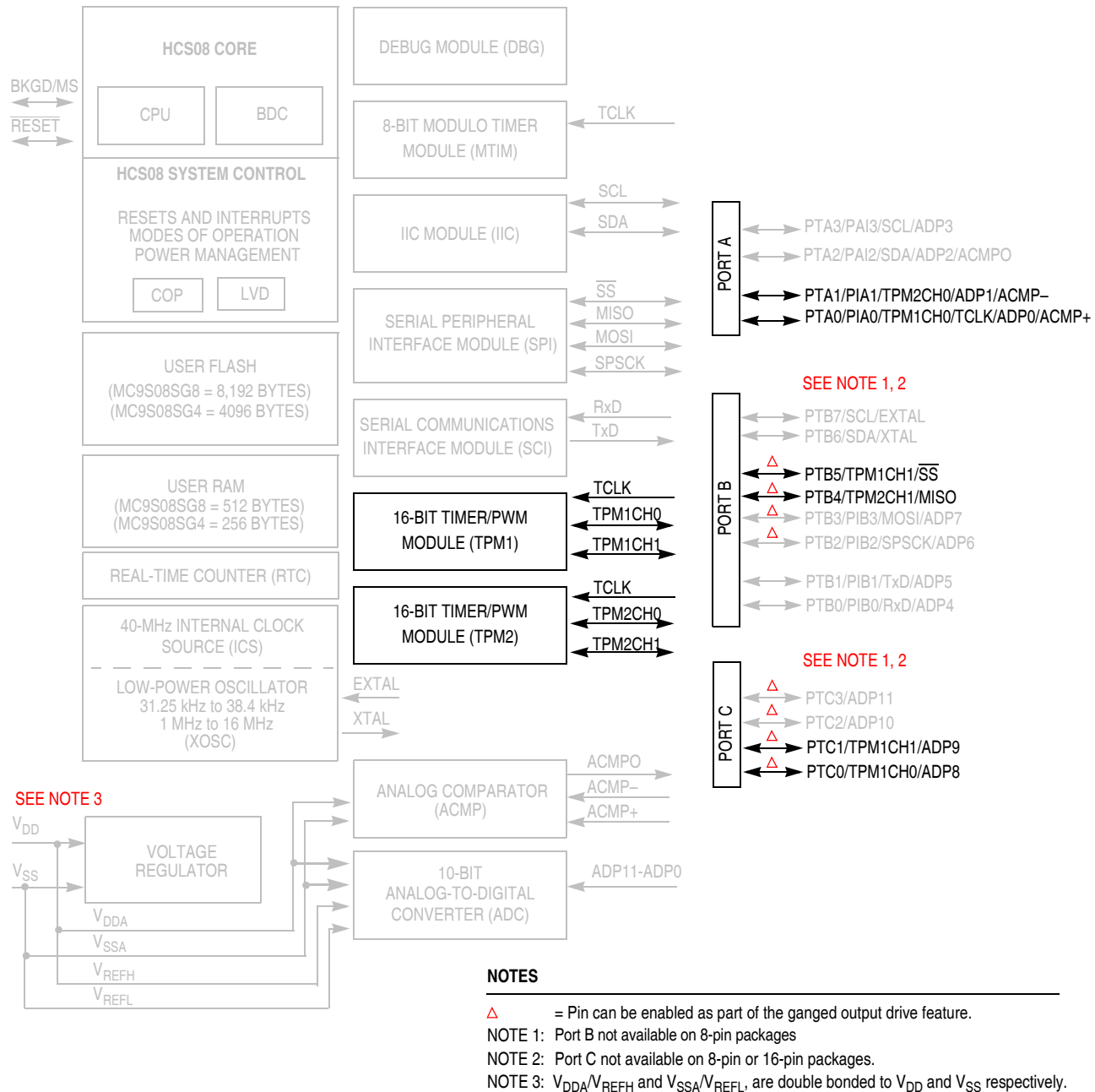
Figure 16-1. MC9S08SG8 Block Diagram with TPM Modules Highlighted

16.1.3   TPMV3 Differences from Previous Versions

The TPMV3 is the latest version of the Timer/PWM module that addresses errata found in previous versions. The following section outlines the differences between TPMV3 and TPMV2 modules, and any considerations that should be taken when porting code.

Table 16-8. TPMxCnSC Field Descriptions (continued)

Field	Description
4 MSnA	Mode select A for TPM channel n. When CPWMS=0 and MSnB=0, MSnA configures TPM channel n for input-capture mode or output compare mode. Refer to Table 16-9 for a summary of channel mode and setup controls. **Note:** If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger.
3–2 ELSnB ELSnA	Edge/level select bits. Depending upon the operating mode for the timer channel as set by CPWMS:MSnB:MSnA and shown in Table 16-9, these bits select the polarity of the input edge that triggers an input capture event, select the level that will be driven in response to an output compare match, or select the polarity of the PWM output. Setting ELSnB:ELSnA to 0:0 configures the related timer pin as a general purpose I/O pin not related to any timer functions. This function is typically used to temporarily disable an input capture channel or to make the timer pin available as a general purpose I/O pin when the associated timer channel is set up as a software timer that does not require the use of a pin.

Table 16-9. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	XX	00	Pin not used for TPM - revert to general purpose I/O or other peripheral control	
0	00	01	Input capture	Capture on rising edge only
		10		Capture on falling edge only
		11		Capture on rising or falling edge
	01	01	Output compare	Toggle output on compare
		10		Clear output on compare
		11		Set output on compare
	1X	10	Edge-aligned PWM	High-true pulses (clear output on compare)
		X1		Low-true pulses (set output on compare)
1	XX	10	Center-aligned PWM	High-true pulses (clear output on compare-up)
		X1		Low-true pulses (set output on compare-up)

16.3.5   TPM Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel registers are cleared by reset.

Table A-7. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit	Temp Rated[3] Standard	Temp Rated[3] AEC Grade 0
6	C	RTC adder to stop2 or stop3[7]	S23I$_{DDRTI}$	5	300	500	nA	x	
				3	300	500	nA	x	
7	C	LVD adder to stop3 (LVDE = LVDSE = 1)	S3I$_{DDLVD}$	5	110	180	µA	x	
				3	90	160	µA	x	
8	C	Adder to stop3 for oscillator enabled[8] (EREFSTEN =1)	S3I$_{DDOSC}$	5, 3	5	8	µA	x	
								x	

[1] Typical values are based on characterization data at 25°C. See Figure A-5 through Figure A-7 for typical curves across voltage/temperature.

[2] Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

[3] Electrical characteristics only apply to the temperature rated devices marked with x.

[4] All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

[5] All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins.

[6] Stop currents are tested in production for 25°C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

[7] Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

[8] Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal and low power mode (HGO = 0).
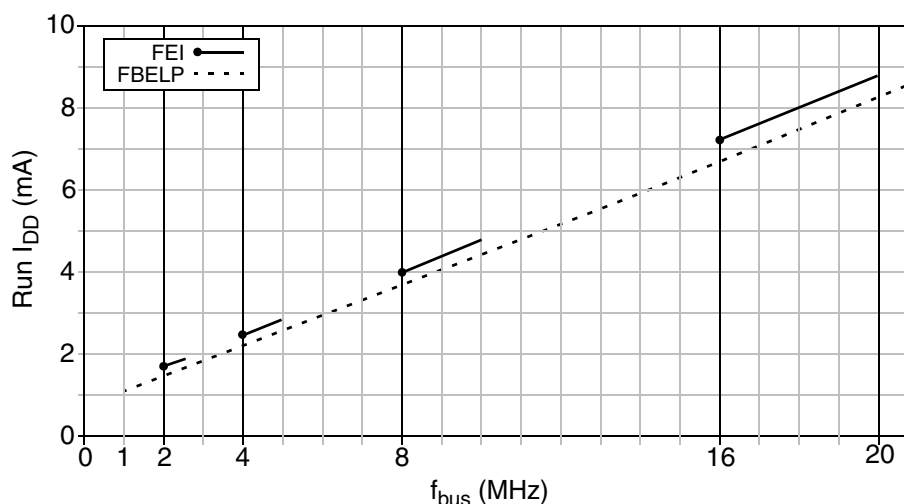
Figure A-5. Typical Run I$_{DD}$ vs. Bus Frequency (V$_{DD}$ = 5V)

A.10 Analog Comparator (ACMP) Electricals

Table A-10. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typ	Max	Unit	Temp Rated[1]	
								Standard	**AEC Grade 0**
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V	x	x
2	D	Supply current (active)	I_{DDAC}	—	20	35	μA	x	x
3	D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V	x	x
4	D	Analog input offset voltage	V_{AIO}		20	40	mV	x	x
5	D	Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV	x	x
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	μA	x	x
7	D	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs	x	x

[1] Electrical characteristics only apply to the temperature rated devices marked with x.

Table A-12. ADC Characteristics (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Temp Rated[2] Standard	Temp Rated[2] AEC Grade 0	Comment
Conversion time (including sample time)	Short sample (ADLSMP=0)	D	t_{ADC}	—	20	—	ADCK cycles	x	x	See ADC Chapter for conversion time variances
	Long sample (ADLSMP=1)			—	40	—		x	x	
Sample time	Short sample (ADLSMP=0)	D	t_{ADS}	—	3.5	—	ADCK cycles	x	x	
	Long sample (ADLSMP=1)			—	23.5	—		x	x	
Total unadjusted error (Includes quantization)	10 bit mode	P	E_{TUE}	—	±1.5	±3.5	LSB[2]	x	x	
	8 bit mode			—	±0.7	±1.5	LSB[3]	x	x	
Differential Non-Linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB[3]	x	x	
	8 bit mode			—	±0.3	±0.5		x	x	
	Monotonicity and No-Missing-Codes guaranteed									
Integral non-linearity	10 bit mode	T	INL	—	±0.5	±1.0	LSB[3]	x	x	
	8 bit mode			—	±0.3	±0.5		x	x	
Zero-scale error	10 bit mode	P	E_{ZS}	—	±1.5	±2.5	LSB[3]	x	x	
	8 bit mode			—	±0.5	±0.7		x	x	
Full-scale error ($V_{ADIN} = V_{DD}$)	10 bit mode	T	E_{FS}	0	±1.0	±1.5	LSB[3]	x	x	
	8 bit mode			0	±0.5	±0.5		x	x	
Quantization error	10 bit mode	D	E_Q	—	—	±0.5	LSB[3]	x	x	
	8 bit mode			—	—	±0.5		x	x	
Input leakage error	10 bit mode	D	E_{IL}	0	±0.2	±2.5	LSB[3]	x	x	Pad leakage[3] * R_{AS}
	8 bit mode			0	±0.1	±1		x	x	
Temp sensor slope	−40°C to 25°C	D	m	—	3.266	—	mV/°C	x	x	
	25°C to 125°C			—	3.638	—		x	x	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	x	x	

[1] Typical values assume V_{DD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Electrical characteristics only apply to the temperature rated devices marked with x.

[3] Based on input pad leakage current. Refer to pad electricals.

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