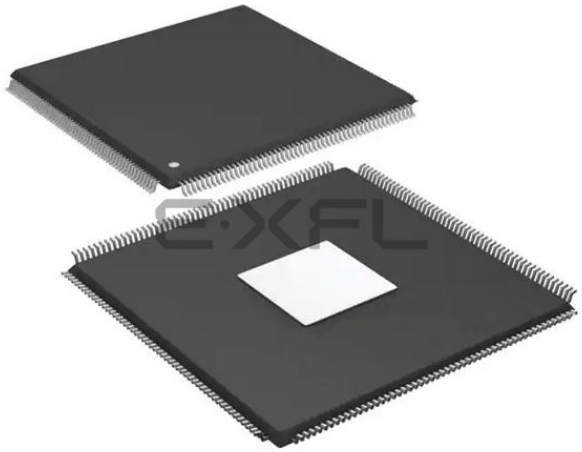

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	266MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21369wbswz102

GENERAL DESCRIPTION

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. These processors are source code-compatible with the ADSP-2126x and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with its large on-chip SRAM, mask programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features[1]

Feature	ADSP-21367	ADSP-21368	ADSP-21369/ ADSP-21369W
Frequency	400 MHz		
RAM	2M bits		
ROM[2]	6M bits		
Audio Decoders in ROM	Yes		
Pulse-Width Modulation	Yes		
S/PDIF	Yes		
SDRAM Memory Bus Width	32/16 bits		
Serial Ports	8		
IDP	Yes		
DAI	Yes		
UART	2		
DAI	Yes		
DPI	Yes		
S/PDIF Transceiver	1		
AMI Interface Bus Width	32/16/8 bits		
SPI	2		
TWI	Yes		
SRC Performance	128 dB		
Package	256 Ball-BGA, 208-Lead LQFP_EP	256 Ball-BGA	256 Ball-BGA, 208-Lead LQFP_EP

[1] W = Automotive grade product. See Automotive Products on Page 61 for more information.

[2] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-21367/ADSP-21368/ADSP-21369 processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (2M bit)
- On-chip mask-programmable ROM (6M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Port

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports of the ADSP-21367/8/9 processors are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 14M words of external memory in bank 0 and 16M words of external memory in bank 1, bank 2, and bank 3.
- An SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3.
- Arbitration Logic to coordinate core and DMA transfers between internal and external memory over the external port.
- A Shared Memory Interface that allows the connection of up to four ADSP-21368 processors to create shared external bus systems (ADSP-21368 only).

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 4.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as either 32 bits wide for maximum performance and bandwidth or 16 bits wide for minimum device count and lower system cost.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF loads. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

External Memory

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus can be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 5.

Table 4. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000–0x00FF FFFF
Bank 1	16M	0x0400 0000–0x04FF FFFF
Bank 2	16M	0x0800 0000–0x08FF FFFF
Bank 3	16M	0x0C00 0000–0x0CFF FFFF

Shared External Memory

The ADSP-21368 processor supports connecting to common shared external memory with other ADSP-21368 processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to four processors.

Bus arbitration is accomplished through the $\overline{BR1–4}$ signals and the priority scheme for bus arbitration is determined by the setting of the RPBA pin. Table 8 on Page 13 provides descriptions of the pins used in multiprocessor systems.

External Port Throughput

The throughput for the external port, based on 166 MHz clock and 32-bit data bus, is 221M bytes/s for the AMI and 664M bytes/s for SDRAM.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and Banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit, 16-bit, or 32-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 2-phase PWM inverters.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provide the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU1), shown in Figure 1.

The SRU is amatrix routing unit (or group of multiplexers) that enable the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI include eight serial ports, an S/PDIF receiver/transmitter, four precision clock generators (PCG), eight channels of synchronous sample rate converters, and an input data port (IDP). The IDP provides an additional input path to the processor core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

For complete information on using the DAI, see the *ADSP-21368 SHARC Processor Hardware Reference*.

Serial Ports

The processors feature eight synchronous serial ports (SPORTs) that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 16 programmable and simultaneous receive or transmit pins that support up to 32 transmit or 32 receive channels of audio data when all eight SPORTs are enabled, or eight full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50 Mbps. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I^2S mode
- I^2S mode
- Packed I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 8: A = asynchronous, G = ground, I = input, O = output, O/T = output three-state, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, (pd) = pull-down resistor, (pu) = pull-up resistor.

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors use extensive pin multiplexing to achieve a lower pin count. For complete information on the multiplexing scheme, see the *ADSP-21368 SHARC Processor Hardware Reference*, "System Design" chapter.

Table 8. Pin Descriptions

Name	Type	State During/ After Reset (ID = 00x)	Description
$ADDR_{23-0}$	O/T (pu)[1]	Pulled high/ driven low	**External Address.** The processors output addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)[1]	Pulled high/ pulled high	**External Data.** Data pins can be multiplexed to support external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default). When configured using the IDP_PDAP_CTL register, IDP Channel 0 scans the external port data pins for parallel input data.
ACK	I (pu)[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (pu)[1]	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. See the processor hardware reference for more information.
$\overline{RD}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processors read a word from external memory.
$\overline{WR}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processors write a word to external memory.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request 0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request 1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS}_2$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/Memory Select 2.**
FLAG[3]/ TMREXP/$\overline{MS}_3$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select 3.**

Table 8. Pin Descriptions (Continued)

Name	Type	State During/ After Reset (ID = 00x)	Description
$\overline{EMU}$	O (O/D, pu)		**Emulation Status.** Must be connected to the ADSP-21367/ADSP-21368/ ADSP-21369 Analog Devices DSP Tools product line of JTAG emulator target board connectors only.
CLK_CFG_{1-0}	I		**Core/CLKIN Ratio Control.** These pins set the start-up clock frequency. See the processor hardware reference for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
CLKIN	I		**Local Clock In.** Used with XTAL. CLKIN is the processor's clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use an external clock such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{RESET}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{RESET}$ input must be asserted (low) at power-up.
$\overline{RESETOUT}$	O	Driven low/ driven high	**Reset Out.** Drives out the core reset signal to an external device.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the processor hardware reference for a description of the boot modes.
$\overline{BR}_{4-1}$	I/O (pu)[1]	Pulled high/ pulled high	**External Bus Request.** Used by the ADSP-21368 processor to arbitrate for bus mastership. A processor only drives its own $\overline{BR}_x$ line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a system with less than four processors, the unused $\overline{BR}_x$ pins should be tied high; the processor's own $\overline{BR}_x$ line must not be tied high or low because it is an output.
ID_{2-0}	I (pd)		**Processor ID.** Determines which bus request ($\overline{BR}_{4-1}$) is used by the ADSP-21368 processor. ID = 001 corresponds to $\overline{BR}_1$, ID = 010 corresponds to $\overline{BR}_2$, and so on. Use ID = 000 or 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset. ID = 101,110, and 111 are reserved.
RPBA	I (pu)[1]		**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for the ADSP-21368 external bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every processor in the system.

[1] The pull-up is always enabled on the ADSP-21367 and ADSP-21369 processors. The pull-up on the ADSP-21368 processor is only enabled on the processor with ID_{2-0} = 00x
[2] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	400 MHz		366 MHz 350 MHz		333 MHz 266 MHz		Unit
		Min	Max	Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.1	–0.5	+1.1	–0.5	+1.1	V
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to 70°C	0	95	0	110	0	110	°C
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+120	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ 0°C to 70°C	0	95	N/A	N/A	0	105	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+105	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: DATAx, ACK, RPBA, $\overline{BRx}$, IDx, FLAGx, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]			0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{IL}[3, 5, 6]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{IHPD}[5]	High Level Input Current Pull-Down	@ V_{DDEXT} = Max, V_{IN} = 0 V			250	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
$I_{DD-INTYP}$[10]	Supply Current (Internal)	t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25°C		700		mA
		t_{CCLK} = 3.00 ns, V_{DDINT} = 1.2 V, 25°C		900		mA
		t_{CCLK} = 2.85 ns, V_{DDINT} = 1.3 V, 25°C		1050		mA
		t_{CCLK} = 2.73 ns, V_{DDINT} = 1.3 V, 25°C		1080		mA
		t_{CCLK} = 2.50 ns, V_{DDINT} = 1.3 V, 25°C		1100		mA
AI_{DD}[11]	Supply Current (Analog)	A_{VDD} = Max			11	mA
C_{IN}[12, 13]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.3 V			4.7	pF

[1] Applies to output and bidirectional pins: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, FLAGx, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDCLKx, $\overline{EMU}$, TDO.
[2] See Output Drive Currents on Page 51 for typical drive current capabilities.
[3] Applies to input pins without internal pull-ups: BOOT_CFGx, CLK_CFGx, CLKIN, $\overline{RESET}$, TCK.
[4] Applies to input pins with internal pull-ups: ACK, RPBA, TMS, TDI, $\overline{TRST}$.
[5] Applies to input pins with internal pull-downs: IDx.
[6] Applies to input pins with internal pull-ups disabled: ACK, RPBA.
[7] Applies to three-statable pins without internal pull-ups: FLAGx, SDCLKx, TDO.
[8] Applies to three-statable pins with internal pull-ups: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, $\overline{EMU}$.
[9] Applies to three-statable pins with internal pull-ups disabled: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10
[10] See the Engineer-to-Engineer Note "*Estimating Power Dissipation for ADSP-21368 SHARC Processors*" (EE-299) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 13 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = Divider value 1, 2, 4, or 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 11. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. See the peripheral specific timing section for each peripheral's timing information.

Table 11. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the processor hardware reference.

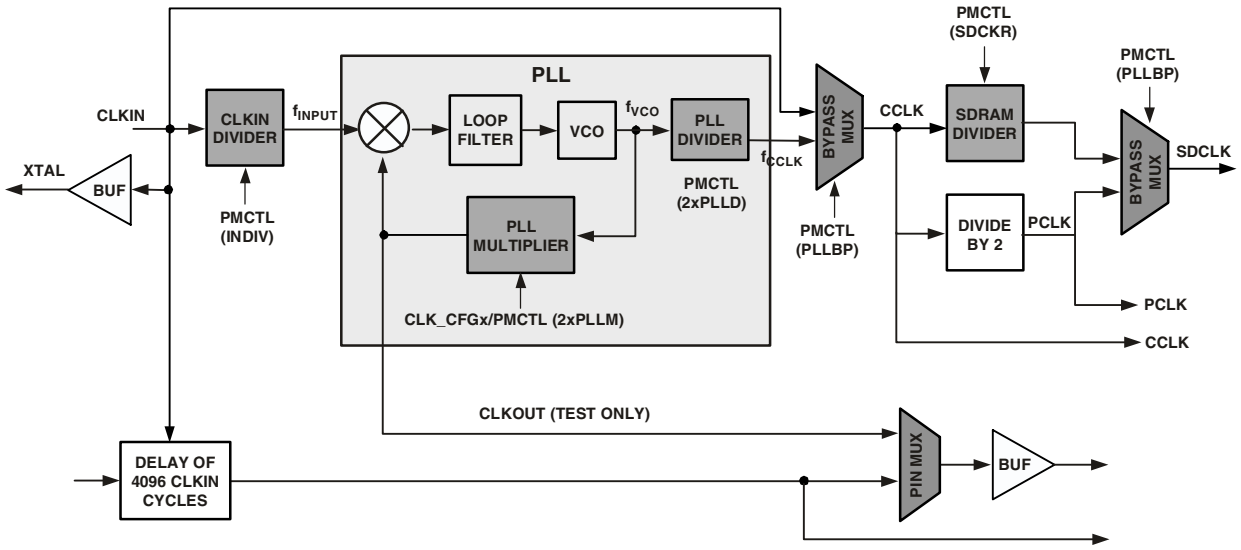

Figure 5. Core Clock and System Clock Relationship to CLKIN

Clock Input

Table 13. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	366 MHz[2] Min	366 MHz[2] Max	350 MHz[3] Min	350 MHz[3] Max	333 MHz[4] Min	333 MHz[4] Max	266 MHz[5] Min	266 MHz[5] Max	Unit
Timing Requirements												
t_{CK}	CLKIN Period	15[6]	100	16.39[6]	100	17.14[6]	100	18[6]	100	22.5[6]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3		3	ns
t_{CCLK}[7]	CCLK Period	2.5[6]	10	2.73[6]	10	2.85[6]	10	3.0[6]	10	3.75[6]	10	ns
f_{VCO}[8]	VCO Frequency	100	800	100	800	100	800	100	800	100	600	MHz
t_{CKJ}[9, 10]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 61.
[2] Applies to all 366 MHz models. See Ordering Guide on Page 61.
[3] Applies to all 350 MHz models. See Ordering Guide on Page 61.
[4] Applies to all 333 MHz models. See Ordering Guide on Page 61.
[5] Applies to all 266 MHz models. See Ordering Guide on Page 61.
[6] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[7] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[8] See Figure 5 on Page 19 for VCO diagram.
[9] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[10] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

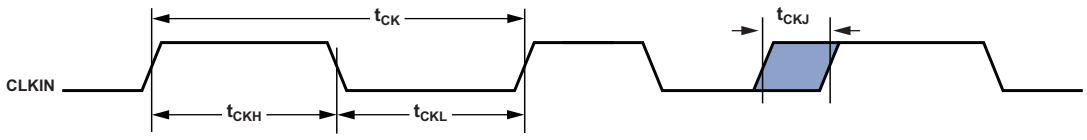

Figure 7. Clock Input

Timer WDTH_CAP Timing

The following specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specification provided in Table 18 is valid at the DPI_P14–1 pins.

Table 18. Timer Width Capture Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

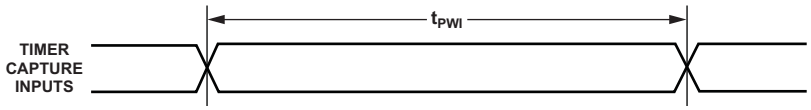

Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 19. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

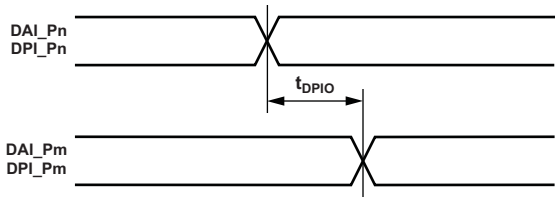

Figure 14. DAI/DPI Pin to Pin Direct Routing

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

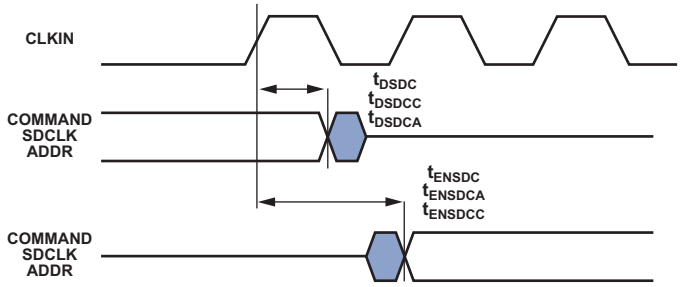

Figure 18. SDRAM Interface Enable/Disable Timing

Memory Write

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus masters, accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

Table 25. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 9.7 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 4.9	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 4.11		ns
t_{WDE}	Data Enabled to $\overline{WR}$ Low	t_{SDCLK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

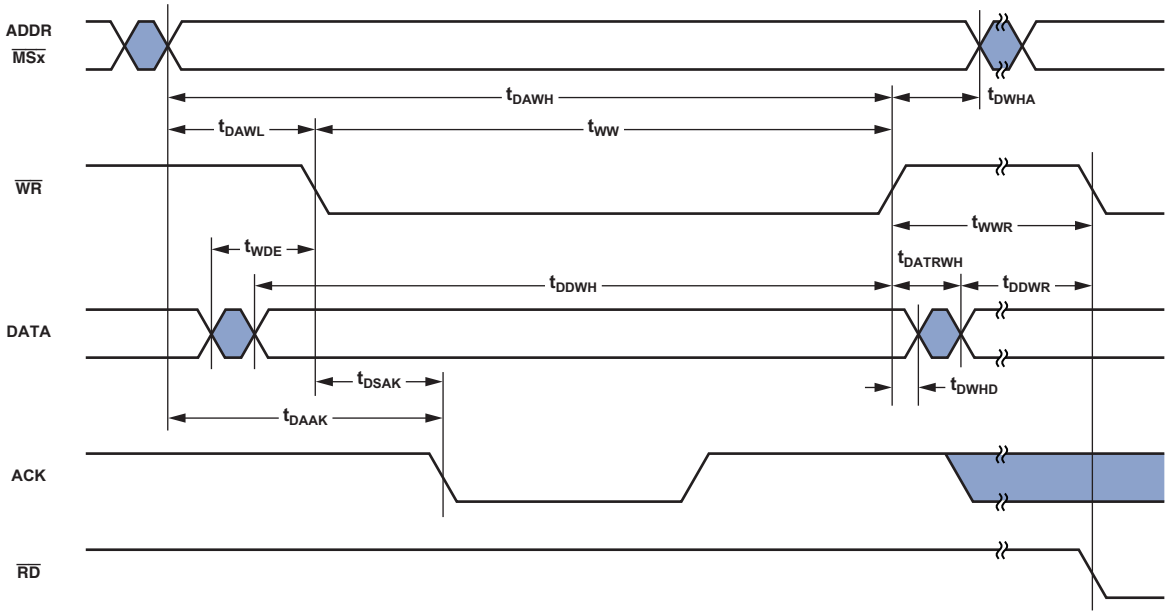

Figure 20. Memory Write

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

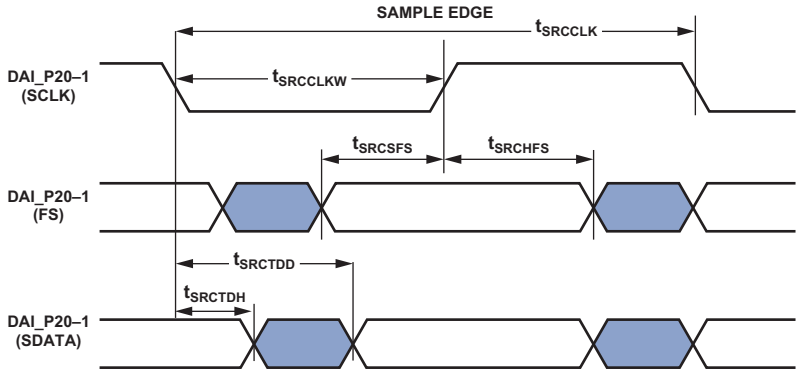

Figure 30. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

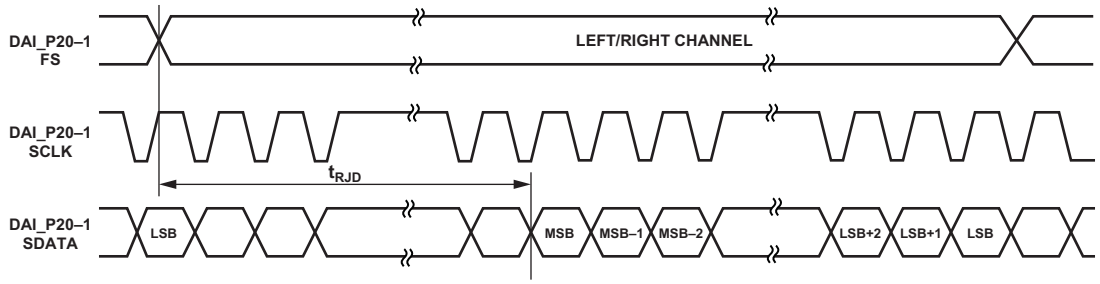

Figure 31. Right-Justified Mode

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

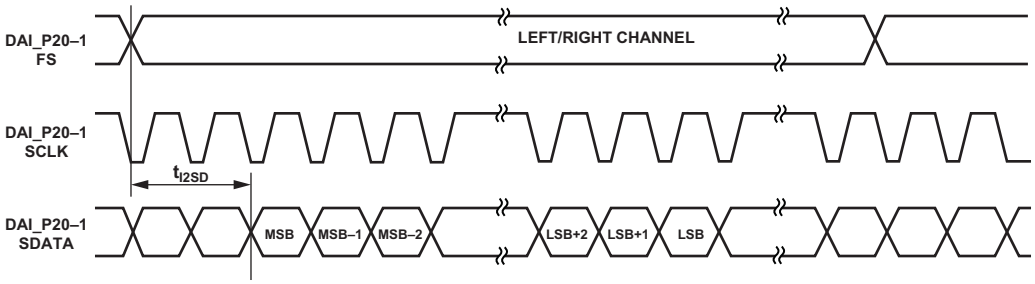

Figure 32. I²S-Justified Mode

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphase clock.

Table 38. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = 384 × FS		Oversampling Ratio × FS <= $1/t_{SITXCLK}$	MHz
TxCLK Frequency for TxCLK = 256 × FS		49.2	MHz
Frame Rate (FS)		192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 39. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK		5	ns
t_{HOFSI}	LRCLK Hold After SCLK	–2		ns
t_{DDTI}	Transmit Data Delay After SCLK		5	ns
t_{HDTI}	Transmit Data Hold After SCLK	–2		ns
t_{SCLKIW}[1]	Transmit SCLK Width	40		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of LRCLK.

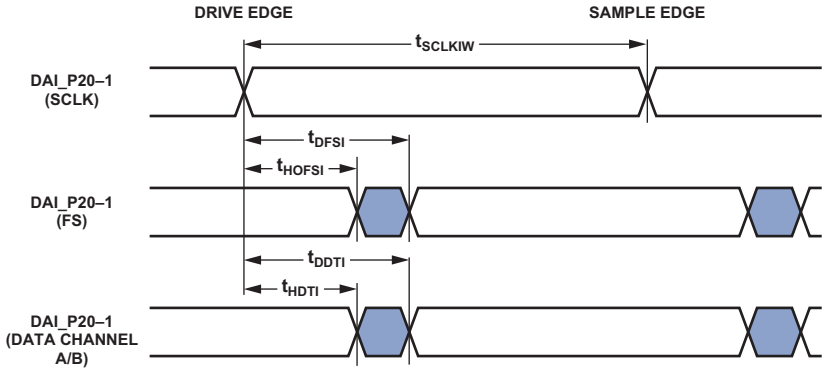

Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

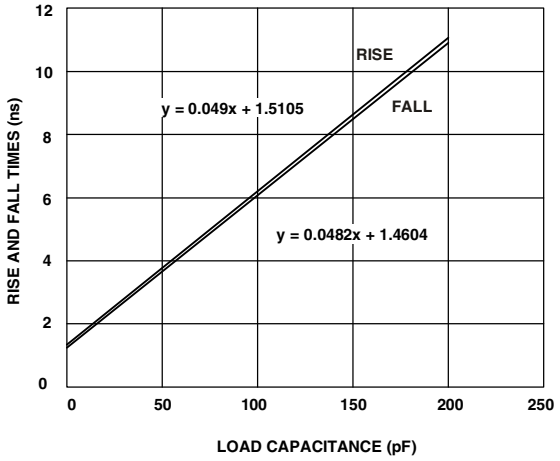

Figure 43. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

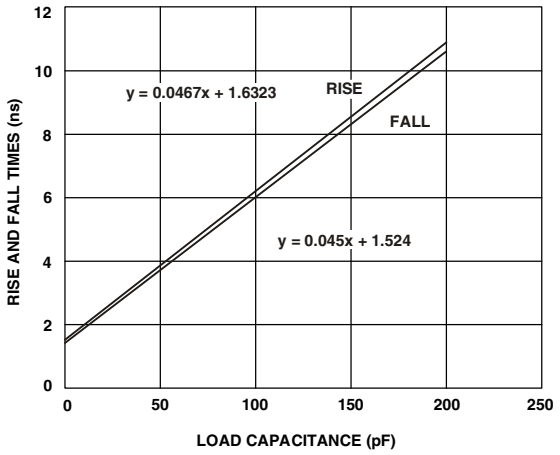

Figure 44. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

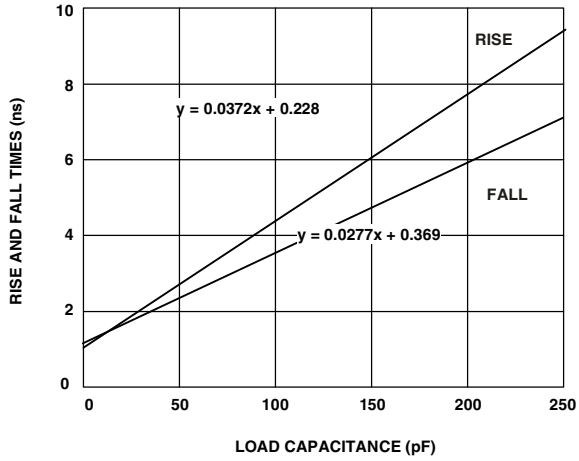

Figure 45. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

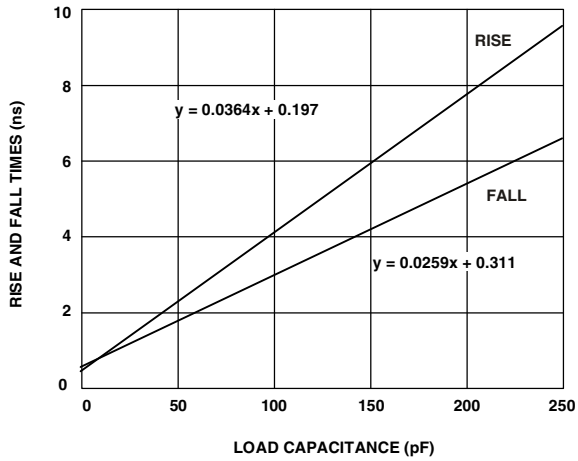

Figure 46. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N01	$\overline{RD}$	P01	SDA10	R01	$\overline{SDWE}$	T01	SDCKE
N02	SDCLK0	P02	$\overline{WR}$	R02	$\overline{SDRAS}$	T02	$\overline{SDCAS}$
N03	GND	P03	V_{DDINT}	R03	GND	T03	GND
N04	V_{DDEXT}	P04	V_{DDINT}	R04	GND	T04	V_{DDEXT}
N17	GND	P17	V_{DDINT}	R17	V_{DDEXT}	T17	GND
N18	GND	P18	V_{DDINT}	R18	GND	T18	GND
N19	DATA11	P19	DATA8	R19	DATA6	T19	DATA5
N20	DATA10	P20	DATA9	R20	DATA7	T20	DATA4
U01	$\overline{MS0}$	V01	ADDR22	W01	GND	Y01	GND
U02	$\overline{MS1}$	V02	ADDR23	W02	ADDR21	Y02	NC
U03	V_{DDINT}	V03	V_{DDINT}	W03	ADDR19	Y03	NC
U04	GND	V04	GND	W04	ADDR20	Y04	ADDR18
U05	V_{DDEXT}	V05	GND	W05	ADDR17	Y05	NC/$\overline{BR1}$[2]
U06	GND	V06	GND	W06	ADDR16	Y06	NC/$\overline{BR2}$[2]
U07	V_{DDEXT}	V07	GND	W07	ADDR15	Y07	XTAL
U08	V_{DDINT}	V08	V_{DDINT}	W08	ADDR14	Y08	CLKIN
U09	V_{DDEXT}	V09	GND	W09	A_{VDD}	Y09	NC
U10	GND	V10	GND	W10	A_{VSS}	Y10	NC
U11	V_{DDEXT}	V11	GND	W11	ADDR13	Y11	NC/$\overline{BR3}$[2]
U12	V_{DDINT}	V12	V_{DDINT}	W12	ADDR12	Y12	NC/$\overline{BR4}$[2]
U13	V_{DDEXT}	V13	V_{DDEXT}	W13	ADDR10	Y13	ADDR11
U14	V_{DDEXT}	V14	GND	W14	ADDR8	Y14	ADDR9
U15	V_{DDINT}	V15	V_{DDINT}	W15	ADDR5	Y15	ADDR7
U16	V_{DDEXT}	V16	GND	W16	ADDR4	Y16	ADDR6
U17	V_{DDINT}	V17	GND	W17	ADDR1	Y17	ADDR3
U18	V_{DDINT}	V18	GND	W18	ADDR2	Y18	GND
U19	DATA0	V19	DATA1	W19	ADDR0	Y19	GND
U20	DATA2	V20	DATA3	W20	NC	Y20	NC

[1] The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
[2] Applies to ADSP-21368 models only.

208-LEAD LQFP_EP PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDINT}	43	V_{DDINT}	85	V_{DDEXT}	127	V_{DDINT}	169	CLK_CFG0
2	DATA28	44	DATA4	86	GND	128	GND	170	BOOT_CFG0
3	DATA27	45	DATA5	87	V_{DDINT}	129	V_{DDEXT}	171	CLK_CFG1
4	GND	46	DATA2	88	ADDR14	130	DAI_P19 (SCLK5)	172	$\overline{EMU}$
5	V_{DDEXT}	47	DATA3	89	GND	131	DAI_P18 (SD5B)	173	BOOT_CFG1
6	DATA26	48	DATA0	90	V_{DDEXT}	132	DAI_P17 (SD5A)	174	TDO
7	DATA25	49	DATA1	91	ADDR15	133	DAI_P16 (SD4B)	175	DAI_P04 (SFS0)
8	DATA24	50	V_{DDEXT}	92	ADDR16	134	DAI_P15 (SD4A)	176	DAI_P02 (SD0B)
9	DATA23	51	GND	93	ADDR17	135	DAI_P14 (SFS3)	177	DAI_P03 (SCLK0)
10	GND	52	V_{DDINT}	94	ADDR18	136	DAI_P13 (SCLK3)	178	DAI_P01 (SD0A)
11	V_{DDINT}	53	V_{DDINT}	95	GND	137	DAI_P12 (SD3B)	179	V_{DDEXT}
12	DATA22	54	GND	96	V_{DDEXT}	138	V_{DDINT}	180	GND
13	DATA21	55	V_{DDEXT}	97	ADDR19	139	V_{DDEXT}	181	V_{DDINT}
14	DATA20	56	ADDR0	98	ADDR20	140	GND	182	GND
15	V_{DDEXT}	57	ADDR2	99	ADDR21	141	V_{DDINT}	183	DPI_P14 (TIMER1)
16	GND	58	ADDR1	100	ADDR23	142	GND	184	DPI_P13 (TIMER0)
17	DATA19	59	ADDR4	101	ADDR22	143	DAI_P11 (SD3A)	185	DPI_P12 (TWI_CLK)
18	DATA18	60	ADDR3	102	$\overline{MS1}$	144	DAI_P10 (SD2B)	186	DPI_P11 (TWI_DATA)
19	V_{DDINT}	61	ADDR5	103	$\overline{MS0}$	145	DAI_P08 (SFS1)	187	DPI_P10 (UART0RX)
20	GND	62	GND	104	V_{DDINT}	146	DAI_P09 (SD2A)	188	DPI_P09 (UART0TX)
21	DATA17	63	V_{DDINT}	105	V_{DDINT}	147	DAI_P06 (SD1B)	189	DPI_P08 (SPIFLG3)
22	V_{DDINT}	64	GND	106	GND	148	DAI_P07 (SCLK1)	190	DPI_P07 (SPIFLG2)
23	GND	65	V_{DDEXT}	107	V_{DDEXT}	149	DAI_P05 (SD1A)	191	V_{DDEXT}
24	V_{DDINT}	66	ADDR6	108	$\overline{SDCAS}$	150	V_{DDEXT}	192	GND
25	GND	67	ADDR7	109	$\overline{SDRAS}$	151	GND	193	V_{DDINT}
26	DATA16	68	ADDR8	110	SDCKE	152	V_{DDINT}	194	GND
27	DATA15	69	ADDR9	111	$\overline{SDWE}$	153	GND	195	DPI_P06 (SPIFLG1)
28	DATA14	70	ADDR10	112	$\overline{WR}$	154	V_{DDINT}	196	DPI_P05 (SPIFLG0)
29	DATA13	71	GND	113	SDA10	155	GND	197	DPI_P04 (SPIDS)
30	DATA12	72	V_{DDINT}	114	GND	156	V_{DDINT}	198	DPI_P03 (SPICLK)
31	V_{DDEXT}	73	GND	115	V_{DDEXT}	157	V_{DDINT}	199	DPI_P01 (SPIMOSI)
32	GND	74	V_{DDEXT}	116	SDCLK0	158	V_{DDINT}	200	DPI_P02 (SPIMISO)
33	V_{DDINT}	75	ADDR11	117	GND	159	GND	201	$\overline{RESETOUT}$
34	GND	76	ADDR12	118	V_{DDINT}	160	V_{DDINT}	202	$\overline{RESET}$
35	DATA11	77	ADDR13	119	$\overline{RD}$	161	V_{DDINT}	203	V_{DDEXT}
36	DATA10	78	GND	120	ACK	162	V_{DDINT}	204	GND
37	DATA9	79	V_{DDINT}	121	FLAG3	163	TDI	205	DATA30
38	DATA8	80	A_{VSS}	122	FLAG2	164	$\overline{TRST}$	206	DATA31
39	DATA7	81	A_{VDD}	123	FLAG1	165	TCK	207	DATA29

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number) (Continued)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
40	DATA6	82	GND	124	FLAG0	166	GND	208	V_{DDINT}
41	V_{DDEXT}	83	CLKIN	125	DAI_P20 (SFS5)	167	V_{DDINT}		
42	GND	84	XTAL	126	GND	168	TMS		