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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, DPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA Exposed Pad
Supplier Device Package	256-BGA-ED (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21368bbpz-2a

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10/13—Rev. E to Rev. F

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Added Related Signal Chains 12

Corrected $\overline{\text{EMU}}$ pin type from O/T(pu) to O(O/D, pu) in Pin Function Descriptions 13

Corrected Junction Temperature 256-Ball BGA Min Value at ambient temperature (–40°C to +85°C) from 0 to –40 in Operating Conditions 16

Added 400 MHz Min and Max values for Junction Temperature 208-Lead LQFP_EP at ambient temperature 0°C to +70°C in Operating Conditions 16

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processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

Table 3. Internal Memory Space [1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 BFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0009 7FFF	Block 0 ROM (Reserved) 0x0010 0000–0x0012 FFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 0 SRAM 0x0004 C000–0x0004 EFFF	Block 0 SRAM 0x0009 0000–0x0009 3FFF	Block 0 SRAM 0x0009 8000–0x0009 DFFF	Block 0 SRAM 0x0013 0000–0x0013 BFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 BFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000B 7FFF	Block 1 ROM (Reserved) 0x0014 0000–0x0016 FFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 1 SRAM 0x0005 C000–0x0005 EFFF	Block 1 SRAM 0x000B 0000–0x000B 3FFF	Block 1 SRAM 0x000B 8000–0x000B DFFF	Block 1 SRAM 0x0017 0000–0x0017 BFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000C 3FFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

[1] The ADSP-21368 and ADSP-21369 processors include a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

The SRAM can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 42k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2x64-bits, core CLK) and the IOD0/1 buses (2x32-bit, PCLK).

ROM-Based Security

The ADSP-21367/ADSP-21368/ADSP-21369 have a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Port

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports of the ADSP-21367/8/9 processors are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 14M words of external memory in bank 0 and 16M words of external memory in bank 1, bank 2, and bank 3.
- An SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3.
- Arbitration Logic to coordinate core and DMA transfers between internal and external memory over the external port.
- A Shared Memory Interface that allows the connection of up to four ADSP-21368 processors to create shared external bus systems (ADSP-21368 only).

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 4.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as either 32 bits wide for maximum performance and bandwidth or 16 bits wide for minimum device count and lower system cost.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF loads. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

External Memory

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus can be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 5.

Table 4. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000–0x00FF FFFF
Bank 1	16M	0x0400 0000–0x04FF FFFF
Bank 2	16M	0x0800 0000–0x08FF FFFF
Bank 3	16M	0x0C00 0000–0x0CFF FFFF

Shared External Memory

The ADSP-21368 processor supports connecting to common shared external memory with other ADSP-21368 processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to four processors.

Bus arbitration is accomplished through the $\overline{BR1–4}$ signals and the priority scheme for bus arbitration is determined by the setting of the RPBA pin. Table 8 on Page 13 provides descriptions of the pins used in multiprocessor systems.

External Port Throughput

The throughput for the external port, based on 166 MHz clock and 32-bit data bus, is 221M bytes/s for the AMI and 664M bytes/s for SDRAM.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21367/ADSP-21368/ADSP-21369 architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-21368 SHARC Processor Hardware Reference* and the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 8. Pin Descriptions (Continued)

Name	Type	State During/ After Reset (ID = 00x)	Description
$\overline{EMU}$	O (O/D, pu)		**Emulation Status.** Must be connected to the ADSP-21367/ADSP-21368/ ADSP-21369 Analog Devices DSP Tools product line of JTAG emulator target board connectors only.
CLK_CFG_{1-0}	I		**Core/CLKIN Ratio Control.** These pins set the start-up clock frequency. See the processor hardware reference for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
CLKIN	I		**Local Clock In.** Used with XTAL. CLKIN is the processor's clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use an external clock such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{RESET}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{RESET}$ input must be asserted (low) at power-up.
$\overline{RESETOUT}$	O	Driven low/ driven high	**Reset Out.** Drives out the core reset signal to an external device.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the processor hardware reference for a description of the boot modes.
$\overline{BR}_{4-1}$	I/O (pu)[1]	Pulled high/ pulled high	**External Bus Request.** Used by the ADSP-21368 processor to arbitrate for bus mastership. A processor only drives its own $\overline{BR}_x$ line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a system with less than four processors, the unused $\overline{BR}_x$ pins should be tied high; the processor's own $\overline{BR}_x$ line must not be tied high or low because it is an output.
ID_{2-0}	I (pd)		**Processor ID.** Determines which bus request ($\overline{BR}_{4-1}$) is used by the ADSP-21368 processor. ID = 001 corresponds to $\overline{BR}_1$, ID = 010 corresponds to $\overline{BR}_2$, and so on. Use ID = 000 or 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset. ID = 101,110, and 111 are reserved.
RPBA	I (pu)[1]		**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for the ADSP-21368 external bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every processor in the system.

[1] The pull-up is always enabled on the ADSP-21367 and ADSP-21369 processors. The pull-up on the ADSP-21368 processor is only enabled on the processor with ID_{2-0} = 00x
[2] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01–20).

Table 20. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, and PH = FSxPHASE. For more information, see the processor hardware reference, "Precision Clock Generators" chapter.

[1] In normal mode.

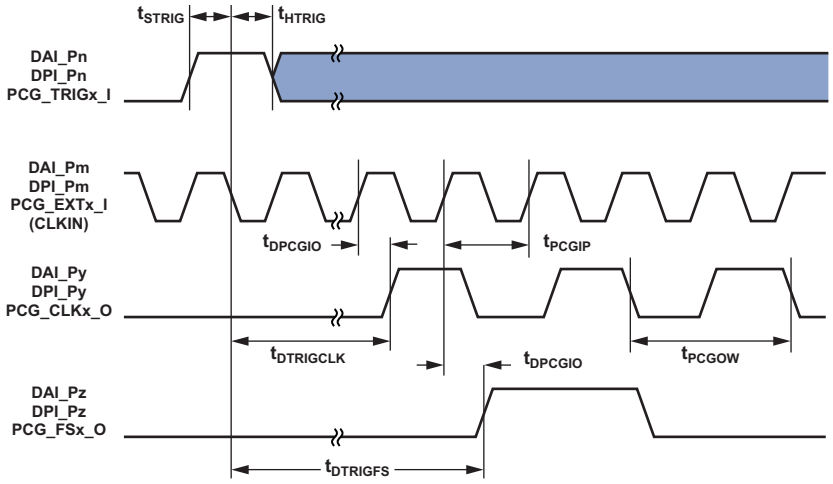


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the serial peripheral interface (SPI). See Table 8 on Page 13 for more information on flag use.

Table 21. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

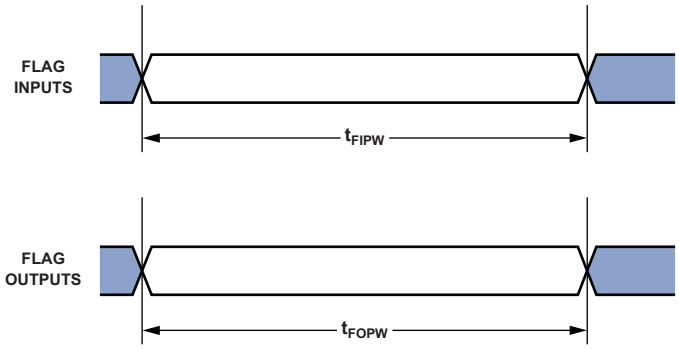


Figure 16. Flags

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

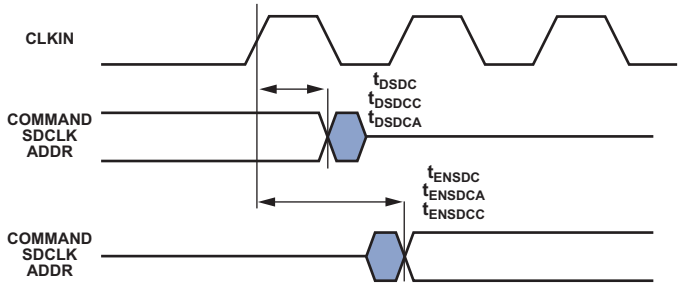


Figure 18. SDRAM Interface Enable/Disable Timing

Memory Write

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus masters, accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

Table 25. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 9.7 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 4.9	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 4.11		ns
t_{WDE}	Data Enabled to $\overline{WR}$ Low	t_{SDCLK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

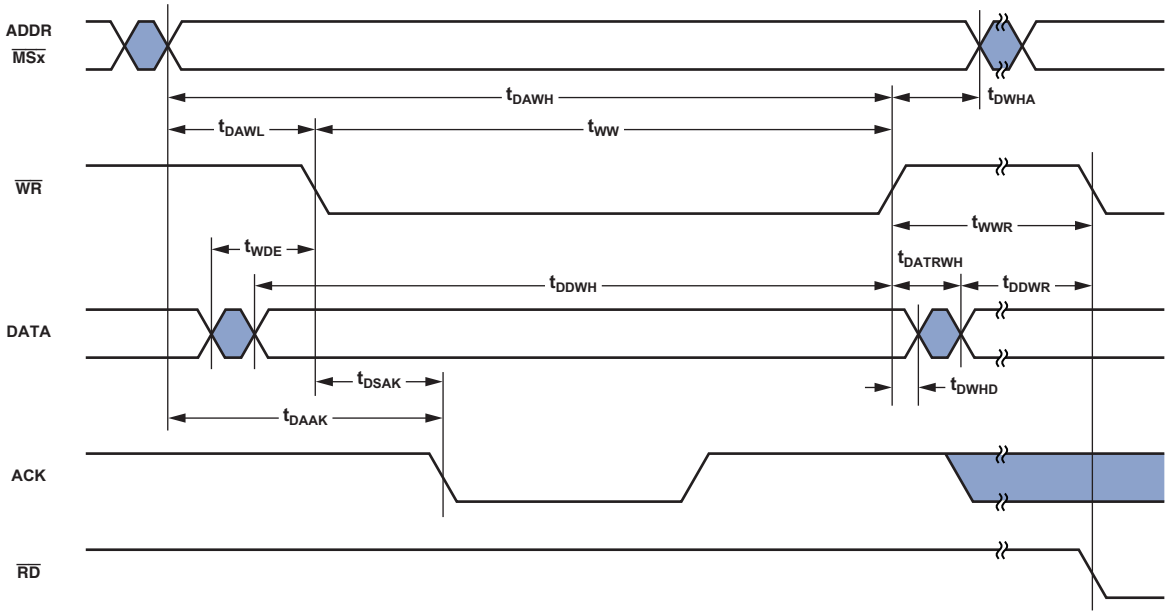


Figure 20. Memory Write

Asynchronous Memory Interface (AMI) Enable/Disable

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 26. AMI Enable/Disable

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{ENAMIAC}$	Address/Control Enable After Clock Rise	4		ns
t_{ENAMID}	Data Enable After Clock Rise	t_{SDCLK} + 4		ns
$t_{DISAMIAC}$	Address/Control Disable After Clock Rise		8.7	ns
$t_{DISAMID}$	Data Disable After Clock Rise		0	ns

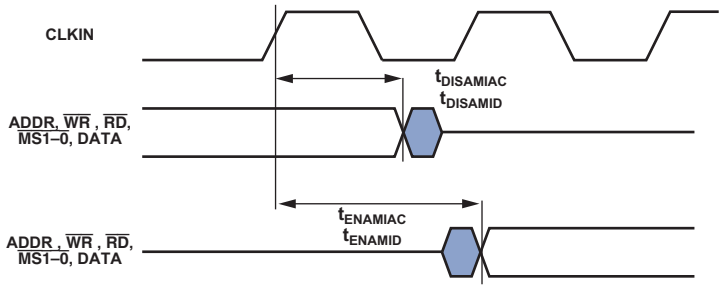


Figure 21. AMI Enable/Disable

Table 29. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		4	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCLKIW}[3]	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] Minimum SPORT divisor register value.

Table 30. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

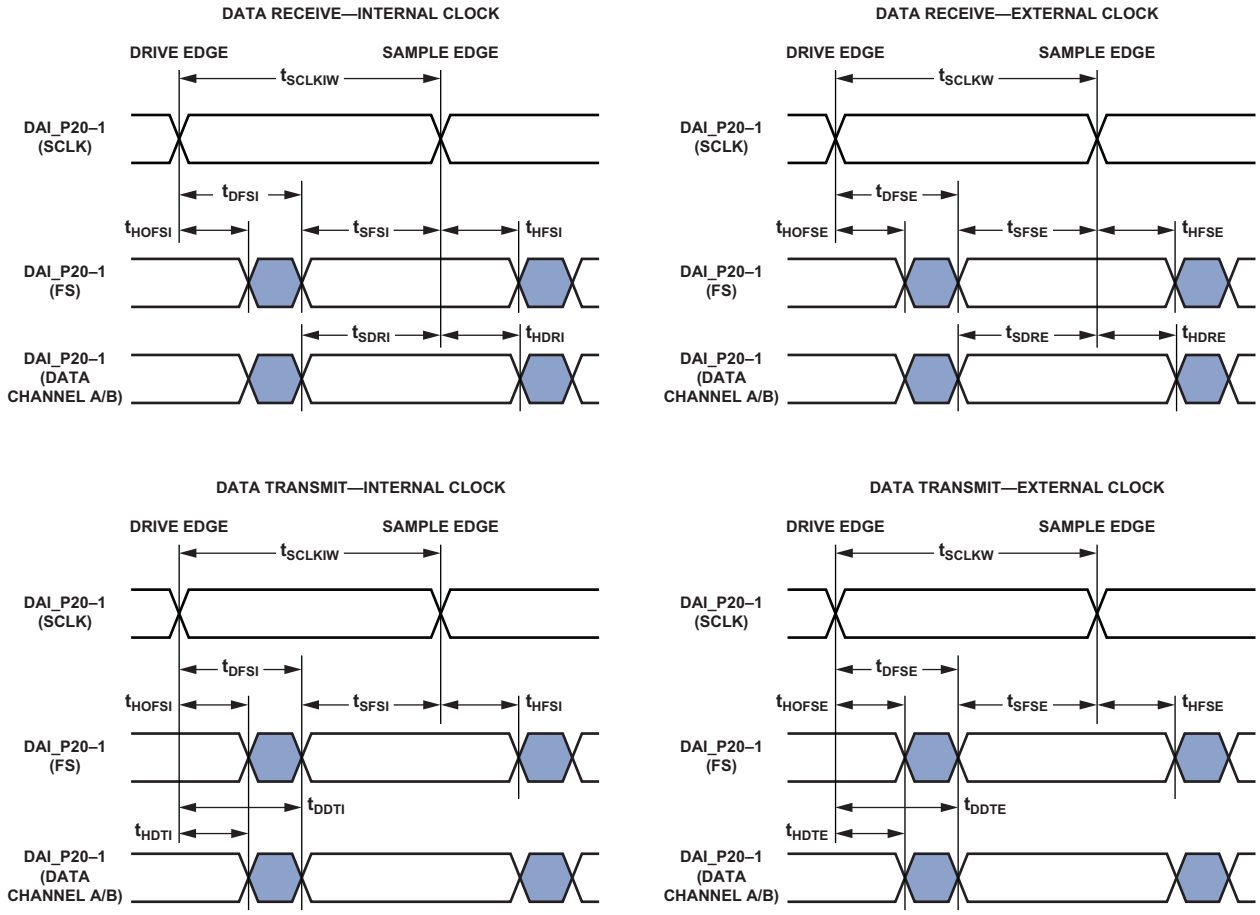


Figure 23. Serial Ports

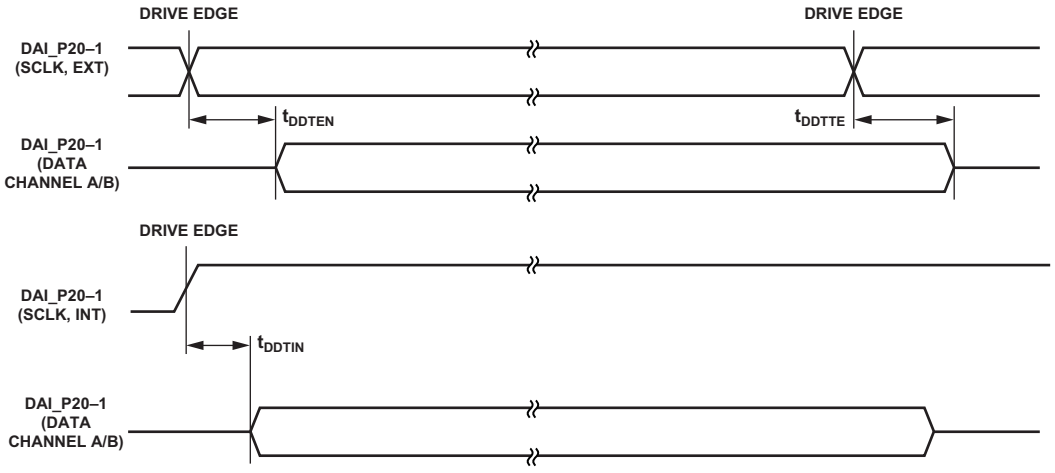


Figure 24. Enable and Three-State

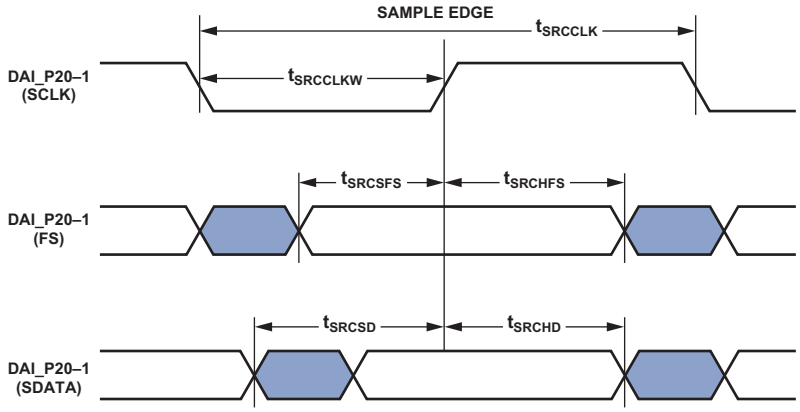


Figure 29. SRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

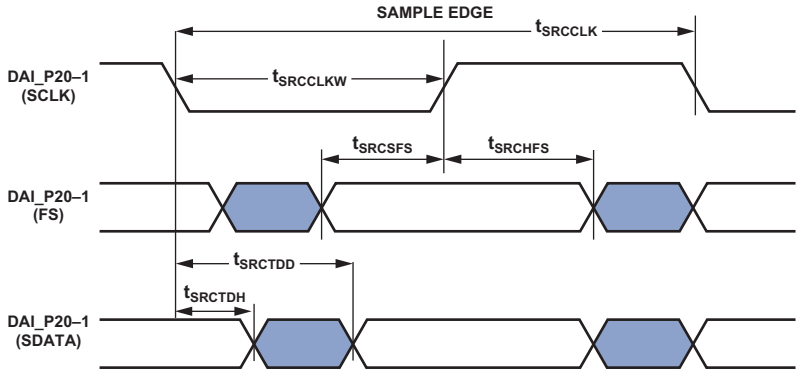


Figure 30. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

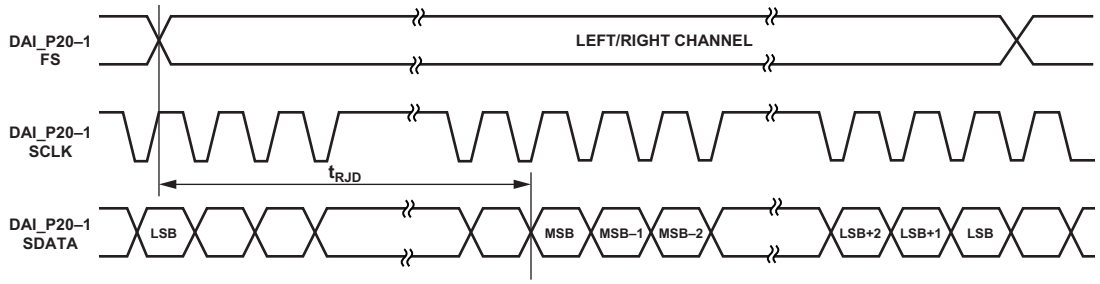


Figure 31. Right-Justified Mode

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

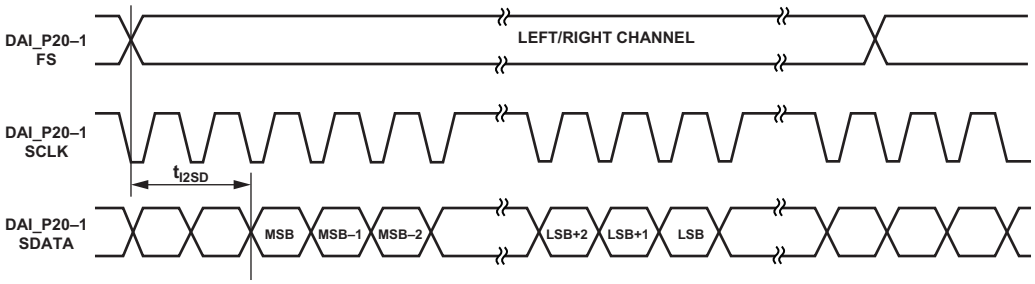


Figure 32. I²S-Justified Mode

JTAG Test Access Port and Emulation

Table 42. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$.

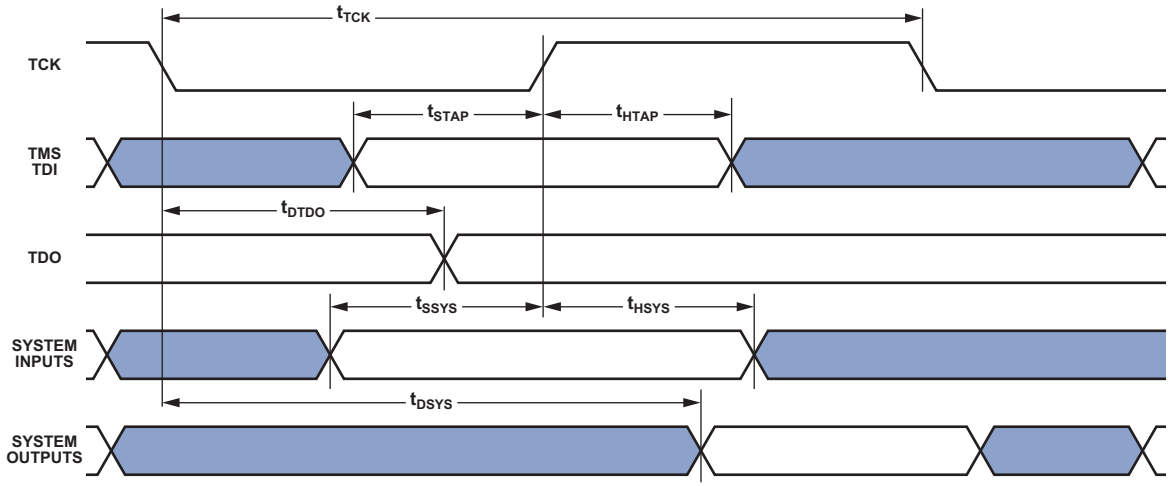


Figure 38. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 39 shows typical I-V characteristics for the output drivers and Figure 40 shows typical I-V characteristics for the SDCLK output drivers. The curves represent the current drive capability of the output drivers as a function of output voltage.

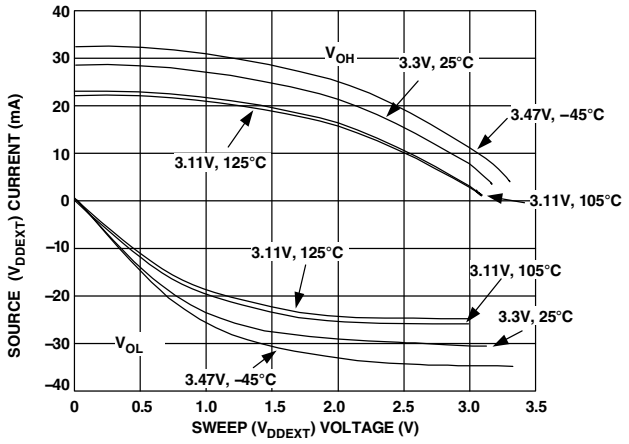


Figure 39. Typical Drive at Junction Temperature

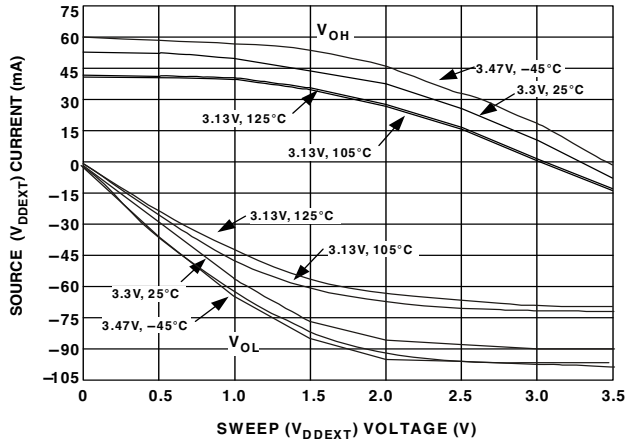


Figure 40. SDCLK1–0 Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 14 on Page 23 through Table 42 on Page 50. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 41.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 41. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

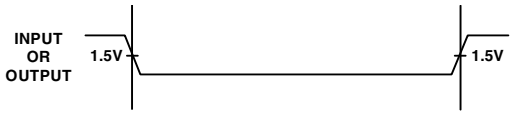
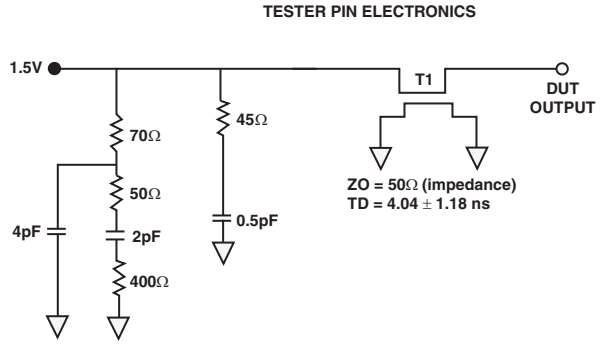


Figure 41. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 42). Figure 47 and Figure 48 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 43 through Figure 48 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

256-BALL BGA_ED PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number)

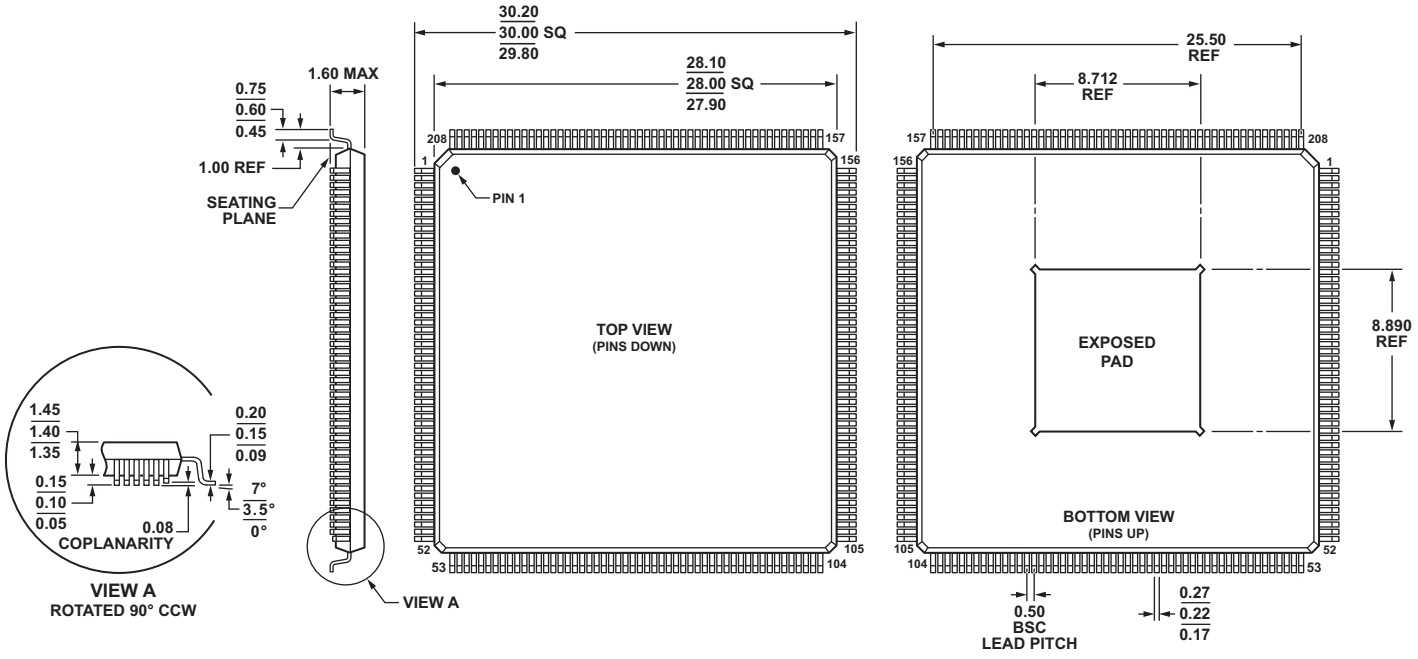
Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI_P05 (SD1A)	C01	DAI_P09 (SD2A)	D01	DAI_P10 (SD2B)
A02	TDI	B02	SDCLK1[1]	C02	DAI_P07 (SCLK1)	D02	DAI_P06 (SD1B)
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	V_{DDEXT}	D04	V_{DDEXT}
A05	CLK_CFG1	B05	BOOT_CFG0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOT_CFG1	C06	GND	D06	V_{DDEXT}
A07	DAI_P04 (SFS0)	B07	TDO	C07	V_{DDINT}	D07	V_{DDINT}
A08	DAI_P01 (SD0A)	B08	DAI_P03 (SCLK0)	C08	GND	D08	GND
A09	DPI_P14 (TIMER1)	B09	DAI_P02 (SD0B)	C09	GND	D09	V_{DDEXT}
A10	DPI_P12 (TWI_CLK)	B10	DPI_P13 (TIMER0)	C10	V_{DDINT}	D10	V_{DDINT}
A11	DPI_P10 (UART0RX)	B11	DPI_P11 (TWI_DATA)	C11	GND	D11	GND
A12	DPI_P09 (UART0TX)	B12	DPI_P08 (SPIFLG3)	C12	GND	D12	V_{DDEXT}
A13	DPI_P07 (SPIFLG2)	B13	DPI_P05 (SPIFLG0)	C13	V_{DDINT}	D13	V_{DDINT}
A14	DPI_P06 (SPIFLG1)	B14	DPI_P04 (SPIDS)	C14	GND	D14	GND
A15	DPI_P03 (SPICLK)	B15	DPI_P01 (SPIMOSI)	C15	GND	D15	V_{DDEXT}
A16	DPI_P02 (SPIMISO)	B16	$\overline{\text{RESET}}$	C16	V_{DDINT}	D16	GND
A17	$\overline{\text{RESETOUT}}$	B17	DATA30	C17	V_{DDINT}	D17	V_{DDEXT}
A18	DATA31	B18	DATA29	C18	V_{DDINT}	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC/RPBA[2]	D20	DATA24
E01	DAI_P11 (SD3A)	F01	DAI_P14 (SFS3)	G01	DAI_P15 (SD4A)	H01	DAI_P17 (SD5A)
E02	DAI_P08 (SFS1)	F02	DAI_P12 (SD3B)	G02	DAI_P13 (SCLK3)	H02	DAI_P16 (SD4B)
E03	V_{DDINT}	F03	GND	G03	GND	H03	V_{DDINT}
E04	V_{DDINT}	F04	GND	G04	V_{DDEXT}	H04	V_{DDINT}
E17	GND	F17	V_{DDEXT}	G17	V_{DDINT}	H17	V_{DDEXT}
E18	GND	F18	GND	G18	V_{DDINT}	H18	GND
E19	DATA25	F19	GND/ID2[2]	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI_P19 (SCLK5)	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI_P18 (SD5B)	K02	DAI_P20 (SFS5)	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	V_{DDINT}	M03	GND
J04	GND	K04	V_{DDEXT}	L04	V_{DDINT}	M04	GND
J17	GND	K17	V_{DDINT}	L17	V_{DDINT}	M17	V_{DDEXT}
J18	GND	K18	V_{DDINT}	L18	V_{DDINT}	M18	GND
J19	GND/ID1[2]	K19	GND/ID0[2]	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number) (Continued)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
40	DATA6	82	GND	124	FLAG0	166	GND	208	V_{DDINT}
41	V_{DDEXT}	83	CLKIN	125	DAI_P20 (SFS5)	167	V_{DDINT}		
42	GND	84	XTAL	126	GND	168	TMS		

PACKAGE DIMENSIONS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are available in 256-ball RoHS compliant and leaded BGA_ED, and 208-lead RoHS compliant LQFP_EP packages.



COMPLIANT TO JEDEC STANDARDS MS-026-BJB-HD

NOTE:
THE EXPOSED PAD IS REQUIRED TO BE ELECTRICALLY AND THERMALLY CONNECTED TO VSS. THIS SHOULD BE IMPLEMENTED BY SOLDERING THE EXPOSED PAD TO A VSS PCB LAND THAT IS THE SAME SIZE AS THE EXPOSED PAD. THE VSS PCB LAND SHOULD BE ROBUSTLY CONNECTED TO THE VSS PLANE IN THE PCB WITH AN ARRAY OF THERMAL VIAS FOR BEST PERFORMANCE.

Figure 51. 208-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-208-1)
Dimensions shown in millimeters