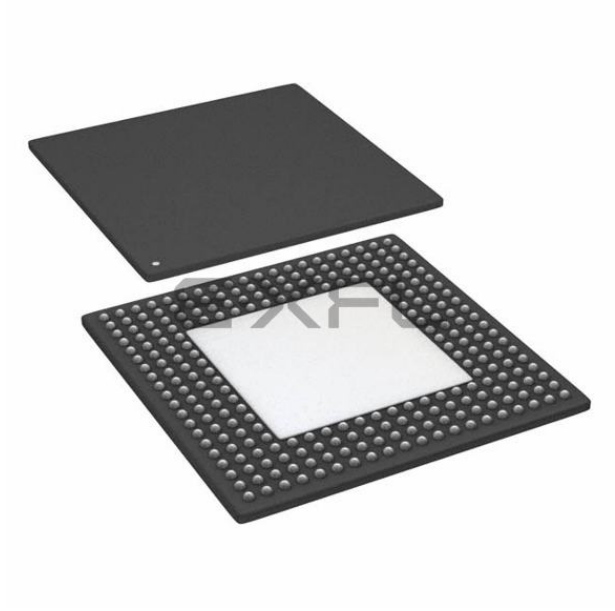

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, DPI
Clock Rate	400MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA Exposed Pad
Supplier Device Package	256-BGA-ED (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21368kbpz-3a

SIMD Computational Engine

The processors contain two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM data bus. These registers contain hardware to handle the data width difference.

Timer

A core timer that can generate periodic software Interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21367/ADSP-21368/ADSP-21369 feature an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2 on Page 4). With separate program and data memory buses and on-chip instruction cache, the processors can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processors include an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The ADSP-21367/ADSP-21368/ADSP-21369 have two data address generators (DAGs). The DAGs are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-21367/ADSP-21368/ADSP-21369 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

On-Chip Memory

The processors contain two megabits of internal RAM and six megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see Table 3 on Page 6). Each memory block supports single-cycle, independent accesses by the core processor and I/O

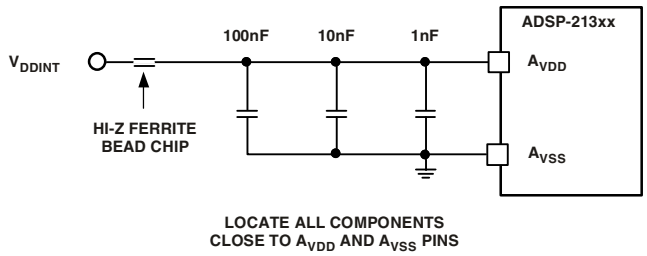


Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21367/ ADSP-21368/ADSP-21369 processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide."

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 13 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = Divider value 1, 2, 4, or 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 11. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. See the peripheral specific timing section for each peripheral's timing information.

Table 11. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the processor hardware reference.

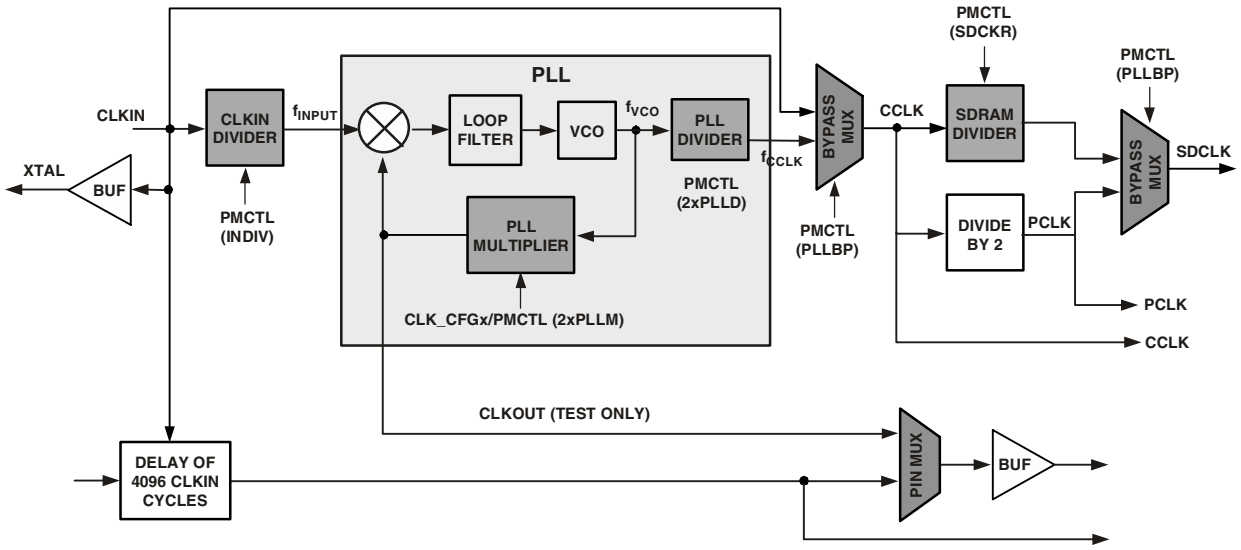


Figure 5. Core Clock and System Clock Relationship to CLKIN

Clock Input

Table 13. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	366 MHz[2] Min	366 MHz[2] Max	350 MHz[3] Min	350 MHz[3] Max	333 MHz[4] Min	333 MHz[4] Max	266 MHz[5] Min	266 MHz[5] Max	Unit
Timing Requirements												
t_{CK}	CLKIN Period	15[6]	100	16.39[6]	100	17.14[6]	100	18[6]	100	22.5[6]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3		3	ns
t_{CCLK}[7]	CCLK Period	2.5[6]	10	2.73[6]	10	2.85[6]	10	3.0[6]	10	3.75[6]	10	ns
f_{VCO}[8]	VCO Frequency	100	800	100	800	100	800	100	800	100	600	MHz
t_{CKJ}[9, 10]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 61.
[2] Applies to all 366 MHz models. See Ordering Guide on Page 61.
[3] Applies to all 350 MHz models. See Ordering Guide on Page 61.
[4] Applies to all 333 MHz models. See Ordering Guide on Page 61.
[5] Applies to all 266 MHz models. See Ordering Guide on Page 61.
[6] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[7] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[8] See Figure 5 on Page 19 for VCO diagram.
[9] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[10] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

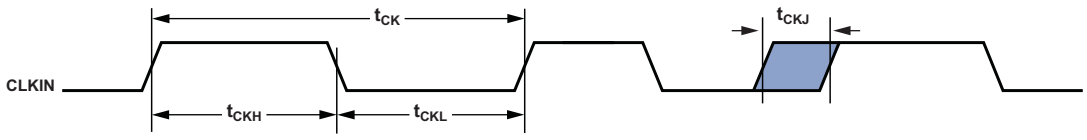


Figure 7. Clock Input

Timer WDTH_CAP Timing

The following specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specification provided in Table 18 is valid at the DPI_P14–1 pins.

Table 18. Timer Width Capture Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

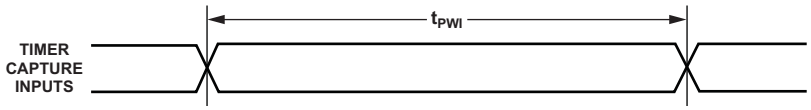


Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 19. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

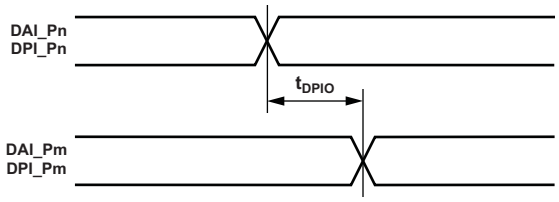


Figure 14. DAI/DPI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01–20).

Table 20. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, and PH = FSxPHASE. For more information, see the processor hardware reference, "Precision Clock Generators" chapter.

[1] In normal mode.

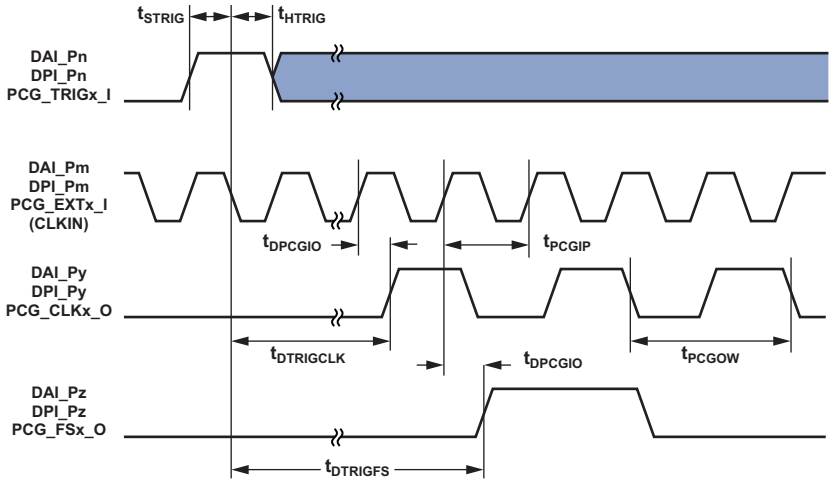


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the serial peripheral interface (SPI). See Table 8 on Page 13 for more information on flag use.

Table 21. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

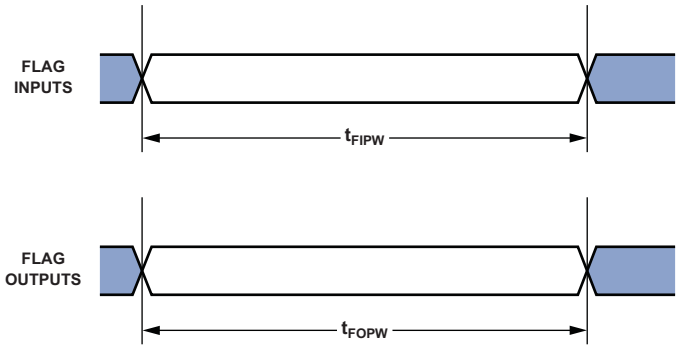


Figure 16. Flags

SDRAM Interface Timing (166 MHz SDCLK)

The 166 MHz access speed is for a single processor. When multiple ADSP-21368 processors are connected in a shared memory system, the access speed is 100 MHz.

Table 22. SDRAM Interface Timing[1]

Parameter		366 MHz Min	366 MHz Max	350 MHz Min	350 MHz Max	All Other Speed Grades Min	All Other Speed Grades Max	Unit
Timing Requirements								
t_{SSDAT}	DATA Setup Before SDCLK	500		500		500		ps
t_{HSDAT}	DATA Hold After SDCLK	1.23		1.23		1.23		ns
Switching Characteristics								
t_{SDCLK}	SDCLK Period	6.83		7.14		6.0		ns
t_{SDCLKH}	SDCLK Width High	3		3		2.6		ns
t_{SDCLKL}	SDCLK Width Low	3		3		2.6		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.8		4.8		4.8	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.2		1.2		1.2		ns
t_{DSDAT}	Data Disable After SDCLK		5.3		5.3		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.3		1.3		1.3		ns

[1] The processor needs to be programmed in $t_{SDCLK} = 2.5 \times t_{CCLK}$ mode when operated at 350 MHz, 366 MHz, and 400 MHz.
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE.

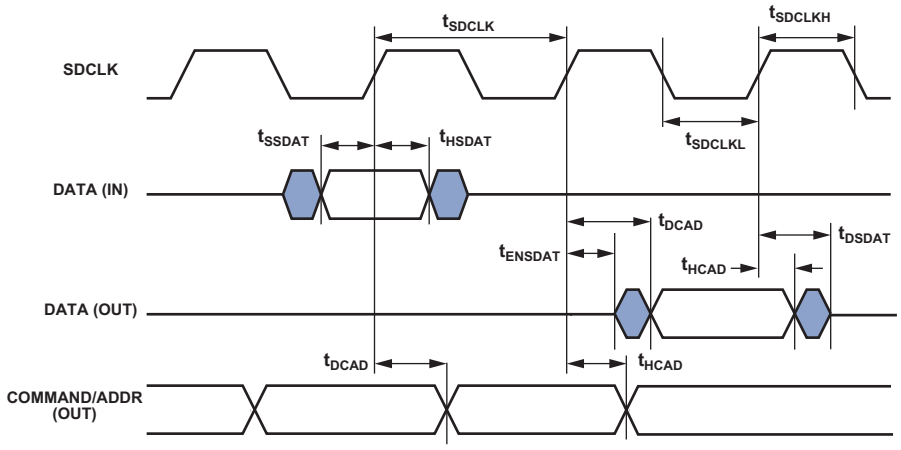


Figure 17. SDRAM Interface Timing

Memory Read

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 24. Memory Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W + t_{SDCLK} –5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[2]		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3, 4]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[1, 5]		t_{SDCLK} –9.5 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RH + 0.20		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[1]	t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI =RHC + IC (RHC = number of read hold cycles specified in AMICTLx register) × t_{SDCLK}.
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] The falling edge of $\overline{MS}$x is referenced.
[2] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Test Conditions on Page 51 for the calculation of hold times given capacitive and dc loads.
[5] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.

Memory Write

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus masters, accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

Table 25. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 9.7 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 4.9	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 4.11		ns
t_{WDE}	Data Enabled to $\overline{WR}$ Low	t_{SDCLK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

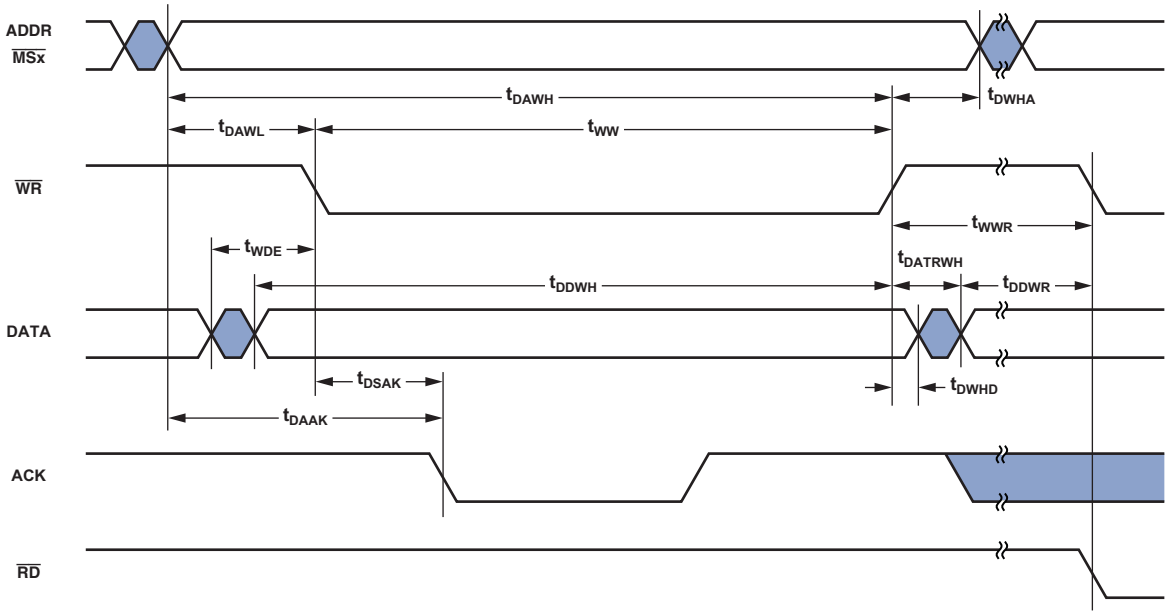


Figure 20. Memory Write

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals SCLK, frame sync (FS), data channel A, data channel B are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. Serial Ports—External Clock

Parameter		400 MHz 366 MHz 350 MHz Min	400 MHz 366 MHz 350 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements								
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		2.0		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics								
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)		10.25		10.25		10.25	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)	2		2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8		9.6		9.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Input Data Port

The timing requirements for the IDP are given in Table 32. IDP signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 32. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

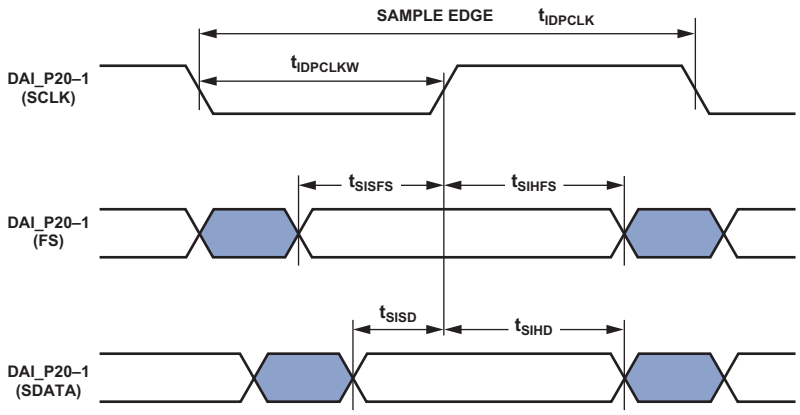


Figure 26. IDP Master Timing

Pulse-Width Modulation Generators

Table 34. PWM Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

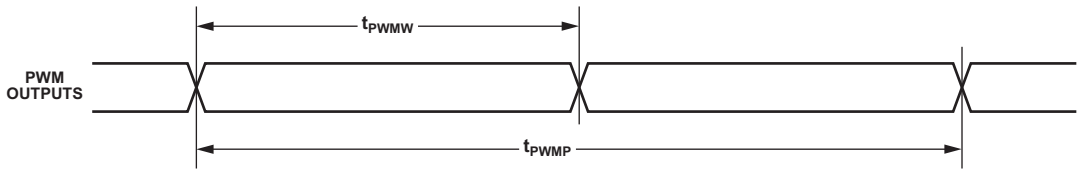


Figure 28. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals SCLK, frame sync (FS), and SDATA are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 35 are valid at the DAI_P20–1 pins.

Table 35. SRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
t_{SRCSD}[1]	SDATA Setup Before SCLK Rising Edge	4		ns
t_{SRCHD}[1]	SDATA Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

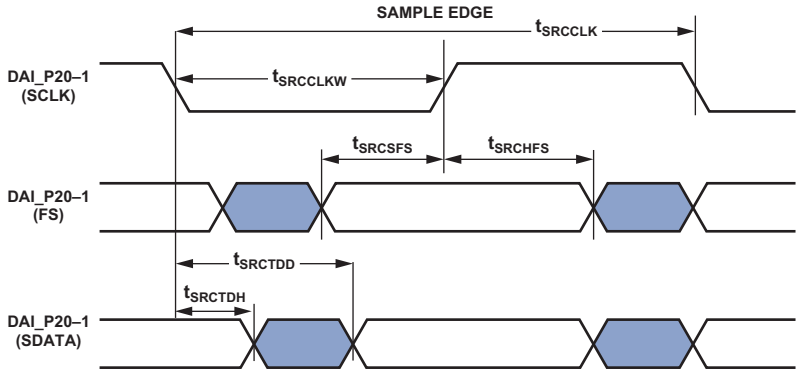


Figure 30. SRC Serial Output Port Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphase clock.

Table 38. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = 384 × FS		Oversampling Ratio × FS <= $1/t_{SITXCLK}$	MHz
TxCLK Frequency for TxCLK = 256 × FS		49.2	MHz
Frame Rate (FS)		192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 39. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK		5	ns
t_{HOFSI}	LRCLK Hold After SCLK	–2		ns
t_{DDTI}	Transmit Data Delay After SCLK		5	ns
t_{HDTI}	Transmit Data Hold After SCLK	–2		ns
t_{SCLKIW}[1]	Transmit SCLK Width	40		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of LRCLK.

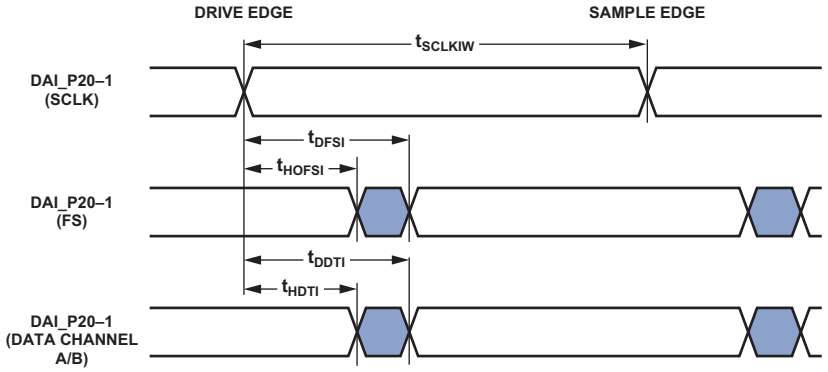


Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

JTAG Test Access Port and Emulation

Table 42. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$.

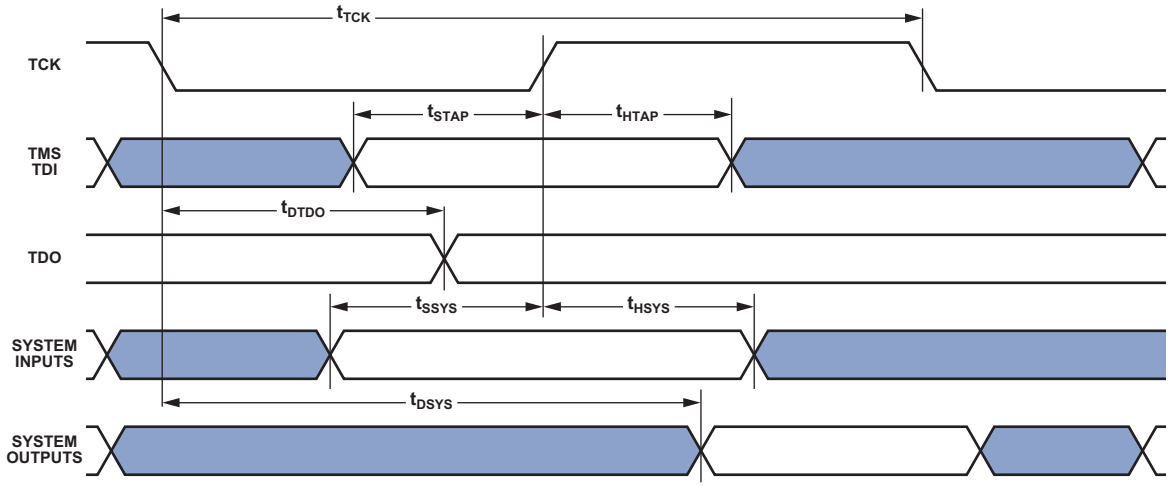


Figure 38. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 39 shows typical I-V characteristics for the output drivers and Figure 40 shows typical I-V characteristics for the SDCLK output drivers. The curves represent the current drive capability of the output drivers as a function of output voltage.

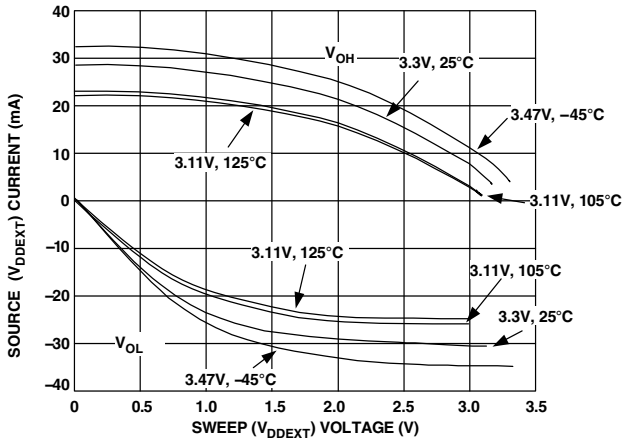


Figure 39. Typical Drive at Junction Temperature

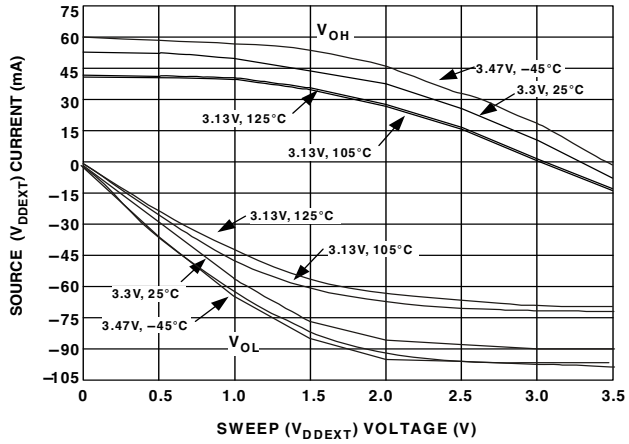


Figure 40. SDCLK1–0 Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 14 on Page 23 through Table 42 on Page 50. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 41.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 41. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

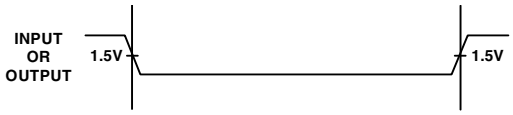
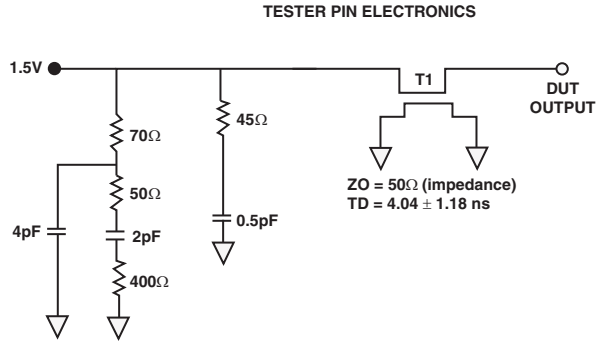


Figure 41. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 42). Figure 47 and Figure 48 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 43 through Figure 48 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

256-BALL BGA_ED PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI_P05 (SD1A)	C01	DAI_P09 (SD2A)	D01	DAI_P10 (SD2B)
A02	TDI	B02	SDCLK1[1]	C02	DAI_P07 (SCLK1)	D02	DAI_P06 (SD1B)
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	V_{DDEXT}	D04	V_{DDEXT}
A05	CLK_CFG1	B05	BOOT_CFG0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOT_CFG1	C06	GND	D06	V_{DDEXT}
A07	DAI_P04 (SFS0)	B07	TDO	C07	V_{DDINT}	D07	V_{DDINT}
A08	DAI_P01 (SD0A)	B08	DAI_P03 (SCLK0)	C08	GND	D08	GND
A09	DPI_P14 (TIMER1)	B09	DAI_P02 (SD0B)	C09	GND	D09	V_{DDEXT}
A10	DPI_P12 (TWI_CLK)	B10	DPI_P13 (TIMER0)	C10	V_{DDINT}	D10	V_{DDINT}
A11	DPI_P10 (UART0RX)	B11	DPI_P11 (TWI_DATA)	C11	GND	D11	GND
A12	DPI_P09 (UART0TX)	B12	DPI_P08 (SPIFLG3)	C12	GND	D12	V_{DDEXT}
A13	DPI_P07 (SPIFLG2)	B13	DPI_P05 (SPIFLG0)	C13	V_{DDINT}	D13	V_{DDINT}
A14	DPI_P06 (SPIFLG1)	B14	DPI_P04 (SPIDS)	C14	GND	D14	GND
A15	DPI_P03 (SPICLK)	B15	DPI_P01 (SPIMOSI)	C15	GND	D15	V_{DDEXT}
A16	DPI_P02 (SPIMISO)	B16	$\overline{\text{RESET}}$	C16	V_{DDINT}	D16	GND
A17	$\overline{\text{RESETOUT}}$	B17	DATA30	C17	V_{DDINT}	D17	V_{DDEXT}
A18	DATA31	B18	DATA29	C18	V_{DDINT}	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC/RPBA[2]	D20	DATA24
E01	DAI_P11 (SD3A)	F01	DAI_P14 (SFS3)	G01	DAI_P15 (SD4A)	H01	DAI_P17 (SD5A)
E02	DAI_P08 (SFS1)	F02	DAI_P12 (SD3B)	G02	DAI_P13 (SCLK3)	H02	DAI_P16 (SD4B)
E03	V_{DDINT}	F03	GND	G03	GND	H03	V_{DDINT}
E04	V_{DDINT}	F04	GND	G04	V_{DDEXT}	H04	V_{DDINT}
E17	GND	F17	V_{DDEXT}	G17	V_{DDINT}	H17	V_{DDEXT}
E18	GND	F18	GND	G18	V_{DDINT}	H18	GND
E19	DATA25	F19	GND/ID2[2]	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI_P19 (SCLK5)	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI_P18 (SD5B)	K02	DAI_P20 (SFS5)	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	V_{DDINT}	M03	GND
J04	GND	K04	V_{DDEXT}	L04	V_{DDINT}	M04	GND
J17	GND	K17	V_{DDINT}	L17	V_{DDINT}	M17	V_{DDEXT}
J18	GND	K18	V_{DDINT}	L18	V_{DDINT}	M18	GND
J19	GND/ID1[2]	K19	GND/ID0[2]	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N01	$\overline{RD}$	P01	SDA10	R01	$\overline{SDWE}$	T01	SDCKE
N02	SDCLK0	P02	$\overline{WR}$	R02	$\overline{SDRAS}$	T02	$\overline{SDCAS}$
N03	GND	P03	V_{DDINT}	R03	GND	T03	GND
N04	V_{DDEXT}	P04	V_{DDINT}	R04	GND	T04	V_{DDEXT}
N17	GND	P17	V_{DDINT}	R17	V_{DDEXT}	T17	GND
N18	GND	P18	V_{DDINT}	R18	GND	T18	GND
N19	DATA11	P19	DATA8	R19	DATA6	T19	DATA5
N20	DATA10	P20	DATA9	R20	DATA7	T20	DATA4
U01	$\overline{MS0}$	V01	ADDR22	W01	GND	Y01	GND
U02	$\overline{MS1}$	V02	ADDR23	W02	ADDR21	Y02	NC
U03	V_{DDINT}	V03	V_{DDINT}	W03	ADDR19	Y03	NC
U04	GND	V04	GND	W04	ADDR20	Y04	ADDR18
U05	V_{DDEXT}	V05	GND	W05	ADDR17	Y05	NC/$\overline{BR1}$[2]
U06	GND	V06	GND	W06	ADDR16	Y06	NC/$\overline{BR2}$[2]
U07	V_{DDEXT}	V07	GND	W07	ADDR15	Y07	XTAL
U08	V_{DDINT}	V08	V_{DDINT}	W08	ADDR14	Y08	CLKIN
U09	V_{DDEXT}	V09	GND	W09	A_{VDD}	Y09	NC
U10	GND	V10	GND	W10	A_{VSS}	Y10	NC
U11	V_{DDEXT}	V11	GND	W11	ADDR13	Y11	NC/$\overline{BR3}$[2]
U12	V_{DDINT}	V12	V_{DDINT}	W12	ADDR12	Y12	NC/$\overline{BR4}$[2]
U13	V_{DDEXT}	V13	V_{DDEXT}	W13	ADDR10	Y13	ADDR11
U14	V_{DDEXT}	V14	GND	W14	ADDR8	Y14	ADDR9
U15	V_{DDINT}	V15	V_{DDINT}	W15	ADDR5	Y15	ADDR7
U16	V_{DDEXT}	V16	GND	W16	ADDR4	Y16	ADDR6
U17	V_{DDINT}	V17	GND	W17	ADDR1	Y17	ADDR3
U18	V_{DDINT}	V18	GND	W18	ADDR2	Y18	GND
U19	DATA0	V19	DATA1	W19	ADDR0	Y19	GND
U20	DATA2	V20	DATA3	W20	NC	Y20	NC

[1] The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
[2] Applies to ADSP-21368 models only.

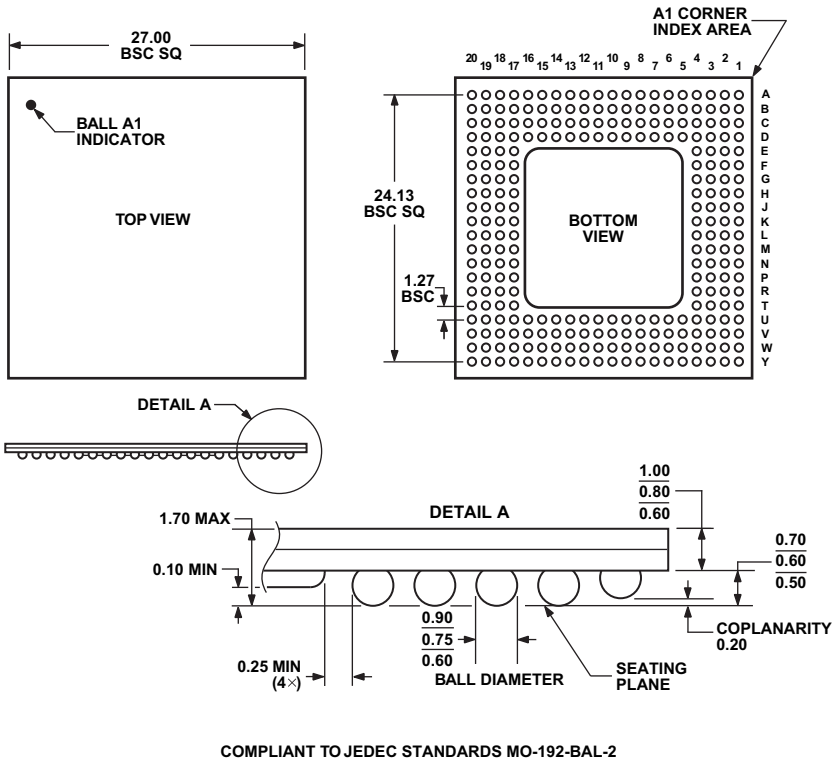


Figure 52. 256-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-256)
Dimension shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA_ED Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Lead Ball Grid Array BGA_ED (BP-256)	Solder Mask Defined (SMD)	0.63 mm	0.73 mm