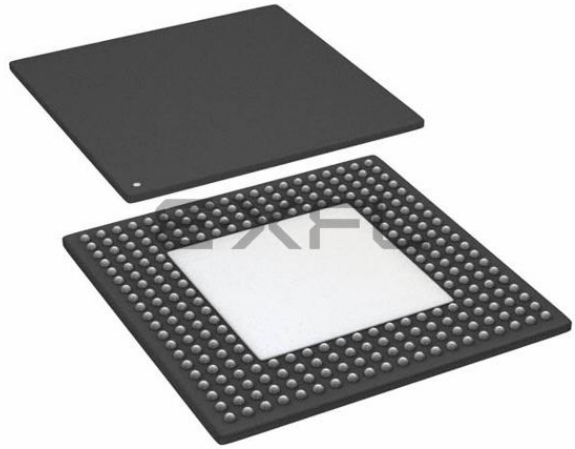

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA Exposed Pad
Supplier Device Package	256-BGA-ED (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21369bbpz-2a

GENERAL DESCRIPTION

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. These processors are source code-compatible with the ADSP-2126x and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with its large on-chip SRAM, mask programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features[1]

Feature	ADSP-21367	ADSP-21368	ADSP-21369/ ADSP-21369W
Frequency	400 MHz		
RAM	2M bits		
ROM[2]	6M bits		
Audio Decoders in ROM	Yes		
Pulse-Width Modulation	Yes		
S/PDIF	Yes		
SDRAM Memory Bus Width	32/16 bits		
Serial Ports	8		
IDP	Yes		
DAI	Yes		
UART	2		
DAI	Yes		
DPI	Yes		
S/PDIF Transceiver	1		
AMI Interface Bus Width	32/16/8 bits		
SPI	2		
TWI	Yes		
SRC Performance	128 dB		
Package	256 Ball-BGA, 208-Lead LQFP_EP	256 Ball-BGA	256 Ball-BGA, 208-Lead LQFP_EP

[1] W = Automotive grade product. See Automotive Products on Page 61 for more information.

[2] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-21367/ADSP-21368/ADSP-21369 processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (2M bit)
- On-chip mask-programmable ROM (6M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-21368 on Page 1 also shows the peripheral clock domain (also known as the I/O processor) and contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 MTM unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), a input data port (IDP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes three timers, a 2-wire interface, two UARTs, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG) and a flexible signal routing unit (DPI SRU).

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 are code compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21367/ADSP-21368/ADSP-21369 processors share architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

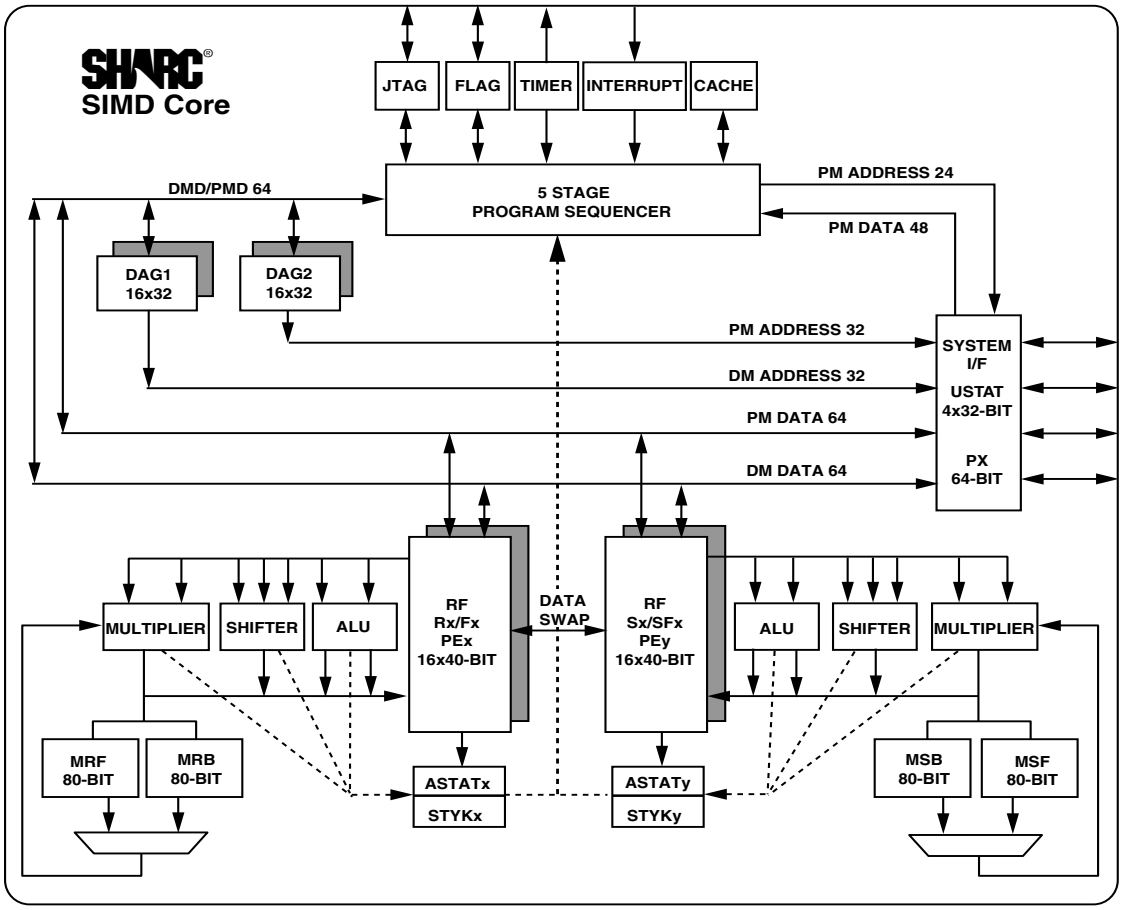

Figure 2. SHARC Core Block Diagram

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example, frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Synchronous/Asynchronous Sample Rate Converter

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), two universal asynchronous receiver-transmitters (UARTs), a 2-wire interface (TWI), 12 flags, and three general-purpose timers.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21367/ADSP-21368/ADSP-21369 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for five data bits to eight data bits, one stop bit or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Where the 16-bit UART_Divisor comes from the DLH register (most significant eight bits) and DLL register (least significant eight bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

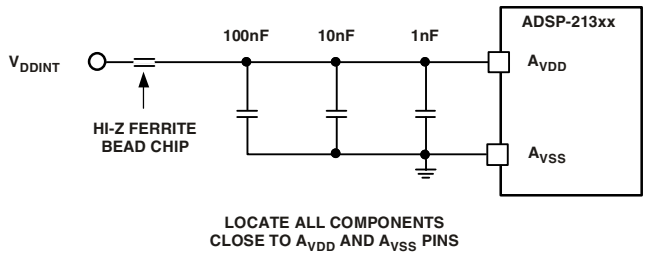

Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21367/ ADSP-21368/ADSP-21369 processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide."

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Table 8. Pin Descriptions (Continued)

Name	Type	State During/ After Reset (ID = 00x)	Description
$\overline{EMU}$	O (O/D, pu)		**Emulation Status.** Must be connected to the ADSP-21367/ADSP-21368/ ADSP-21369 Analog Devices DSP Tools product line of JTAG emulator target board connectors only.
CLK_CFG_{1-0}	I		**Core/CLKIN Ratio Control.** These pins set the start-up clock frequency. See the processor hardware reference for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
CLKIN	I		**Local Clock In.** Used with XTAL. CLKIN is the processor's clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use an external clock such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{RESET}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{RESET}$ input must be asserted (low) at power-up.
$\overline{RESETOUT}$	O	Driven low/ driven high	**Reset Out.** Drives out the core reset signal to an external device.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the processor hardware reference for a description of the boot modes.
$\overline{BR}_{4-1}$	I/O (pu)[1]	Pulled high/ pulled high	**External Bus Request.** Used by the ADSP-21368 processor to arbitrate for bus mastership. A processor only drives its own $\overline{BR}_x$ line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a system with less than four processors, the unused $\overline{BR}_x$ pins should be tied high; the processor's own $\overline{BR}_x$ line must not be tied high or low because it is an output.
ID_{2-0}	I (pd)		**Processor ID.** Determines which bus request ($\overline{BR}_{4-1}$) is used by the ADSP-21368 processor. ID = 001 corresponds to $\overline{BR}_1$, ID = 010 corresponds to $\overline{BR}_2$, and so on. Use ID = 000 or 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset. ID = 101,110, and 111 are reserved.
RPBA	I (pu)[1]		**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for the ADSP-21368 external bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every processor in the system.

[1] The pull-up is always enabled on the ADSP-21367 and ADSP-21369 processors. The pull-up on the ADSP-21368 processor is only enabled on the processor with ID_{2-0} = 00x
[2] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 13 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = Divider value 1, 2, 4, or 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 11. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. See the peripheral specific timing section for each peripheral's timing information.

Table 11. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the processor hardware reference.

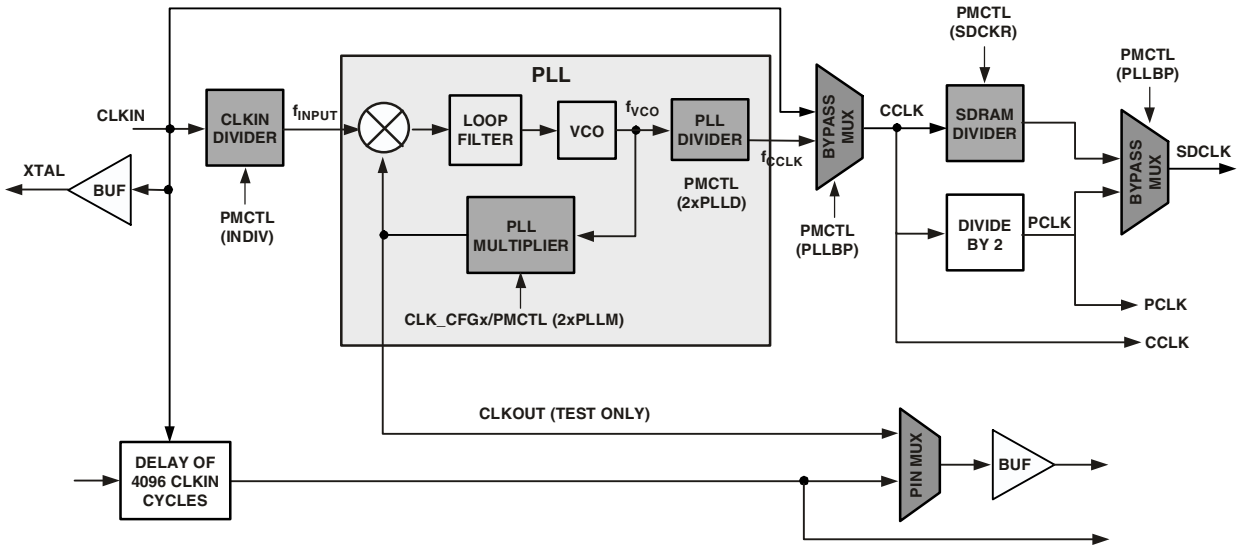

Figure 5. Core Clock and System Clock Relationship to CLKIN

Clock Input

Table 13. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	366 MHz[2] Min	366 MHz[2] Max	350 MHz[3] Min	350 MHz[3] Max	333 MHz[4] Min	333 MHz[4] Max	266 MHz[5] Min	266 MHz[5] Max	Unit
Timing Requirements												
t_{CK}	CLKIN Period	15[6]	100	16.39[6]	100	17.14[6]	100	18[6]	100	22.5[6]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3		3	ns
t_{CCLK}[7]	CCLK Period	2.5[6]	10	2.73[6]	10	2.85[6]	10	3.0[6]	10	3.75[6]	10	ns
f_{VCO}[8]	VCO Frequency	100	800	100	800	100	800	100	800	100	600	MHz
t_{CKJ}[9, 10]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 61.
[2] Applies to all 366 MHz models. See Ordering Guide on Page 61.
[3] Applies to all 350 MHz models. See Ordering Guide on Page 61.
[4] Applies to all 333 MHz models. See Ordering Guide on Page 61.
[5] Applies to all 266 MHz models. See Ordering Guide on Page 61.
[6] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[7] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[8] See Figure 5 on Page 19 for VCO diagram.
[9] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[10] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

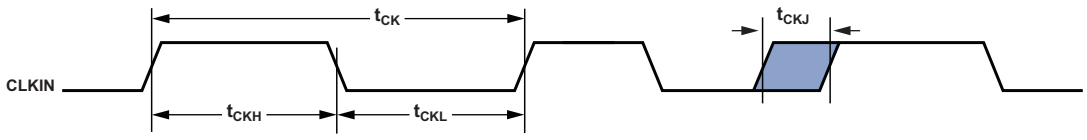

Figure 7. Clock Input

Clock Signals

The processors can use an external clock or a crystal. See the CLKIN pin description in Table 8 on Page 13. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode.

Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

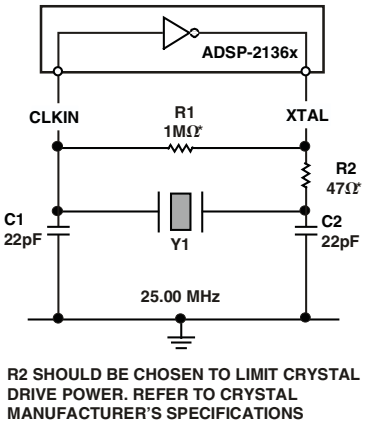

Figure 8. 400 MHz Operation (Fundamental Mode Crystal)

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01–20).

Table 20. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, and PH = FSxPHASE. For more information, see the processor hardware reference, "Precision Clock Generators" chapter.

[1] In normal mode.

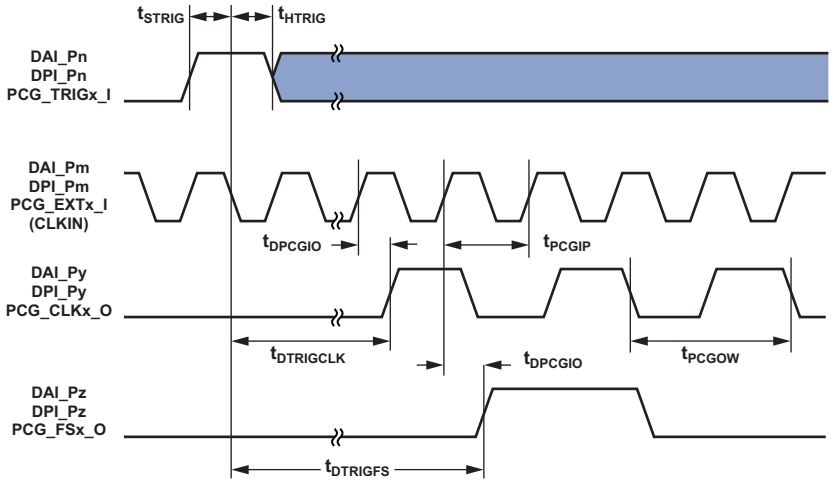

Figure 15. Precision Clock Generator (Direct Pin Routing)

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

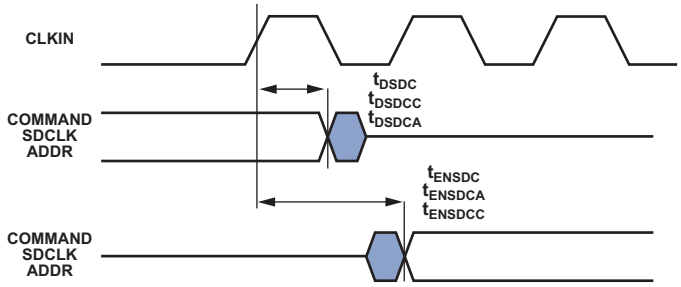

Figure 18. SDRAM Interface Enable/Disable Timing

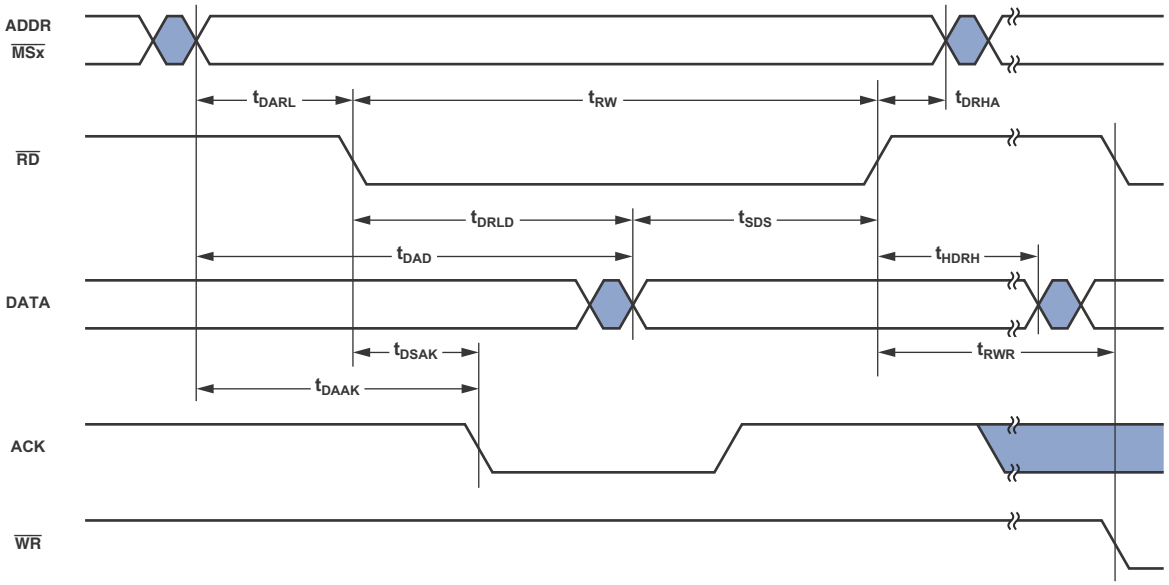

Figure 19. Memory Read

Shared Memory Bus Request

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 27. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$, Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$, Hold After CLKIN High	0.5		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		9	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns

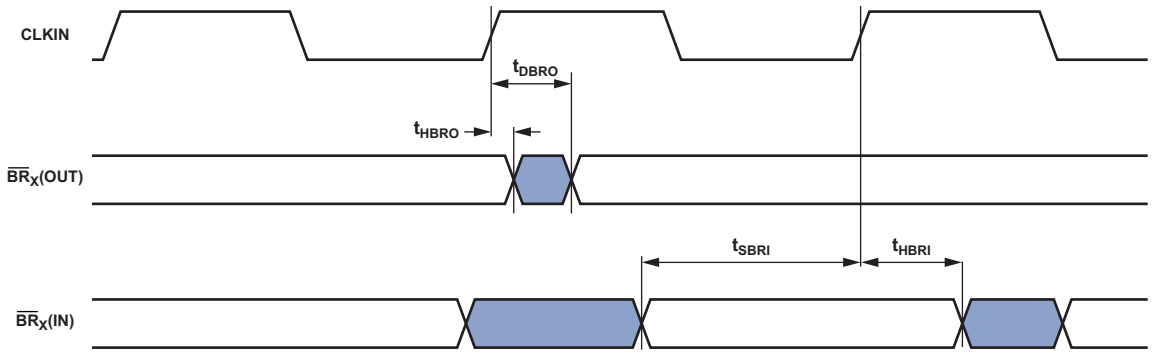

Figure 22. Shared Memory Bus Request

Table 29. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		4	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCLKIW}[3]	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] Minimum SPORT divisor register value.

Table 30. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

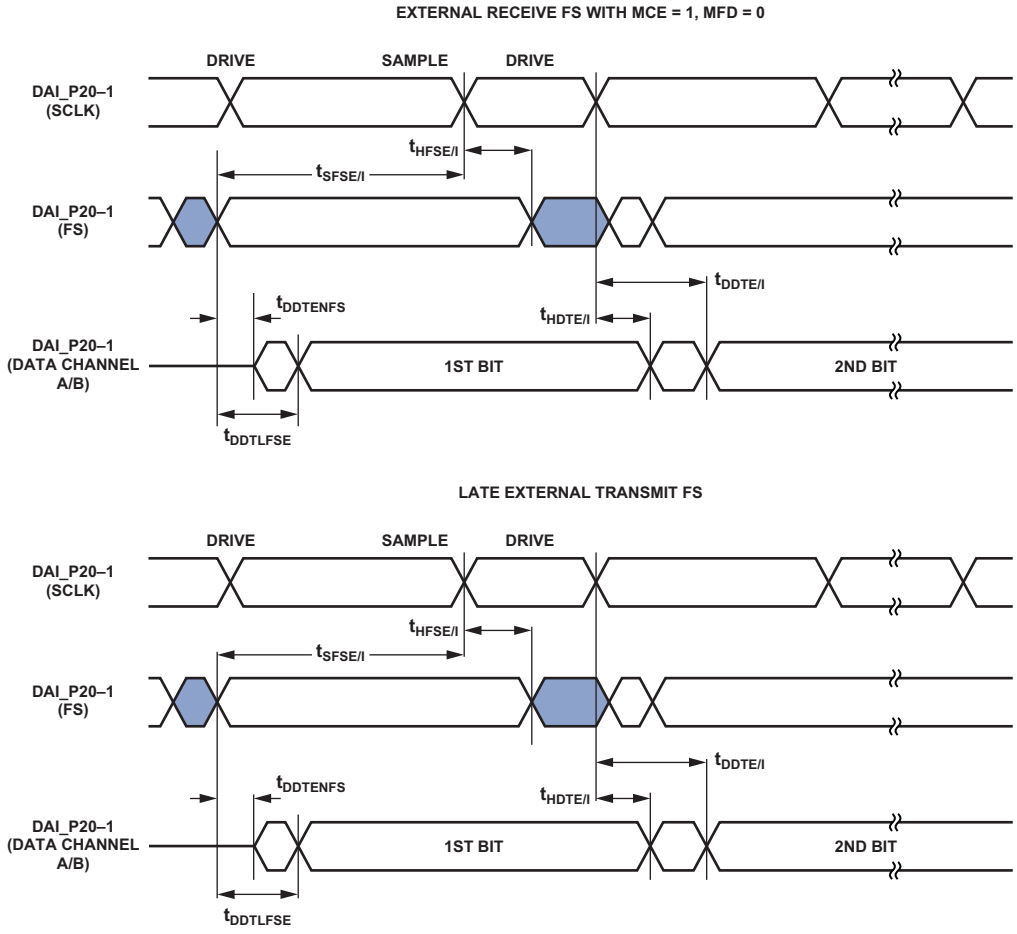

Figure 25. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

Input Data Port

The timing requirements for the IDP are given in Table 32. IDP signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 32. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

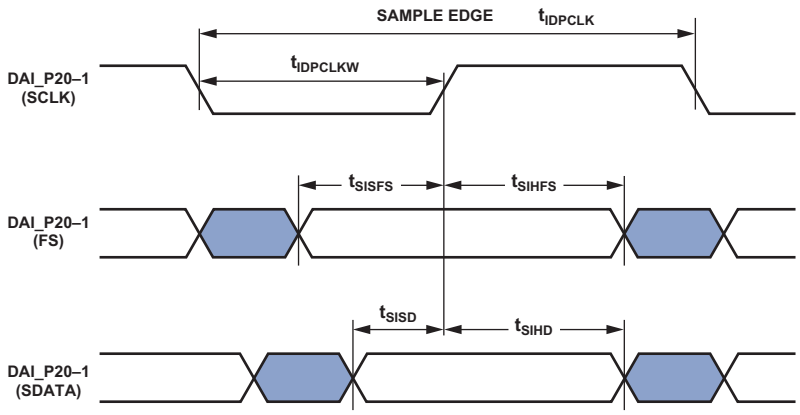

Figure 26. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 33. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, see the IDP chapter of the *ADSP-21368 SHARC Processor Hardware Reference*. Note that the 20 bits of external PDAP data can be provided through the external port DATA31–12 pins or the DAI pins.

Table 33. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Data Source pins are DATA31–12, or DAI pins. Source pins for SCLK and FS are: 1) DATA11–10 pins, 2) DAI pins.

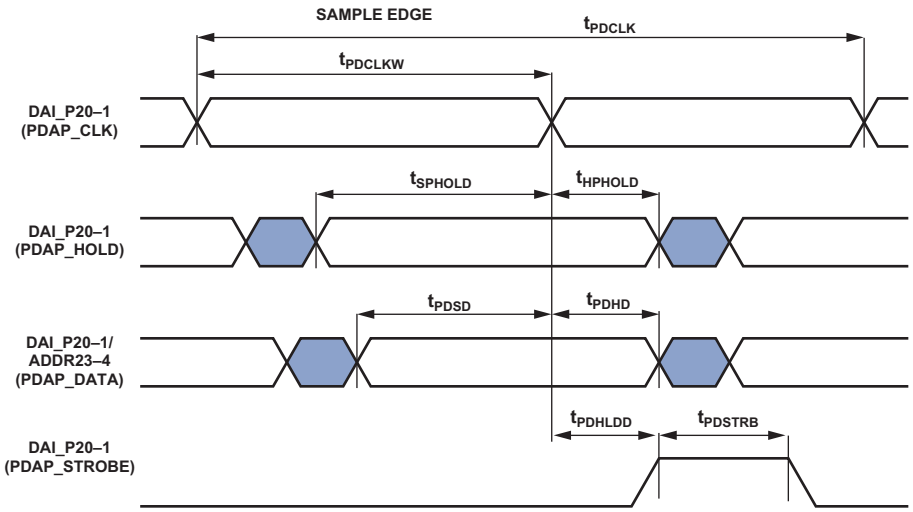

Figure 27. PDAP Timing

Pulse-Width Modulation Generators

Table 34. PWM Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

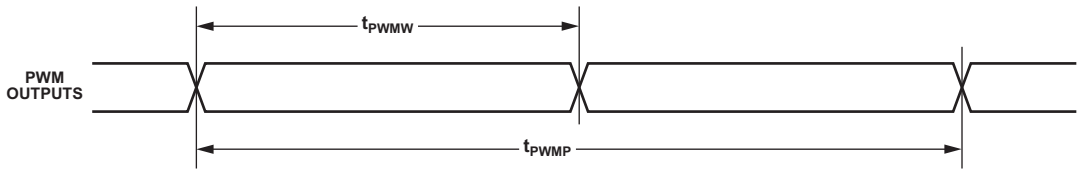

Figure 28. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals SCLK, frame sync (FS), and SDATA are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 35 are valid at the DAI_P20–1 pins.

Table 35. SRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
t_{SRCSD}[1]	SDATA Setup Before SCLK Rising Edge	4		ns
t_{SRCHD}[1]	SDATA Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

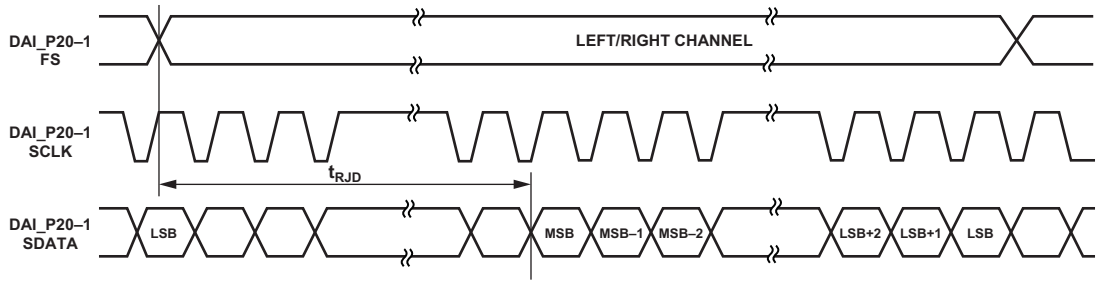

Figure 31. Right-Justified Mode

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

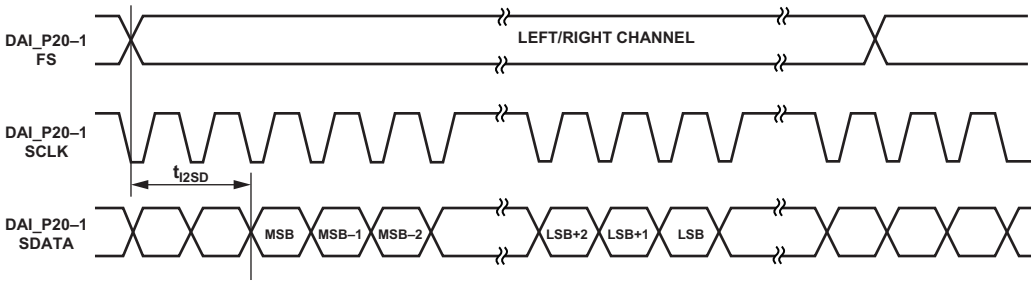

Figure 32. I²S-Justified Mode

SPI Interface—Master

The processors contain two SPI ports. The primary has dedicated pins and the secondary is available through the DPI. The timing provided in Table 40 and Table 41 on Page 49 applies to both.

Table 40. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

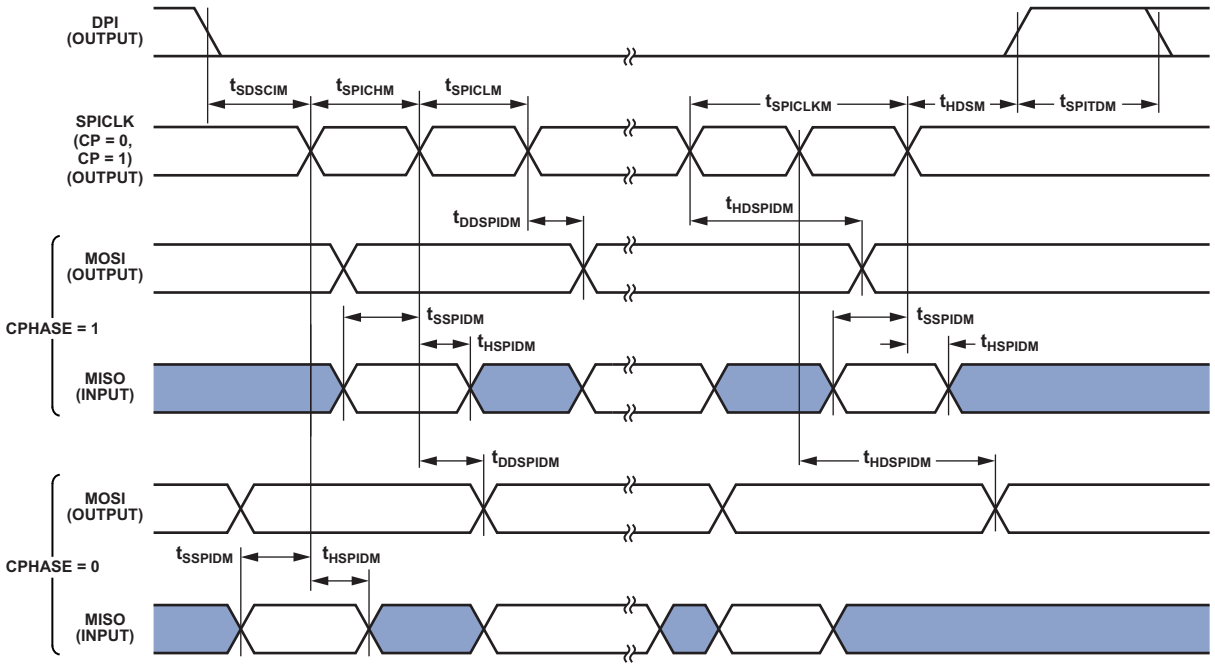

Figure 36. SPI Master Timing

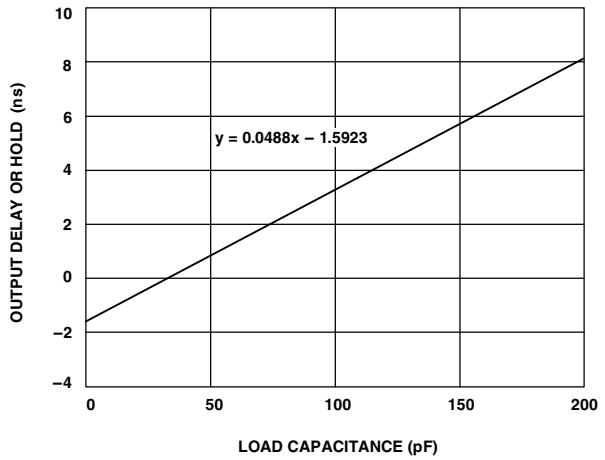

Figure 47. Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

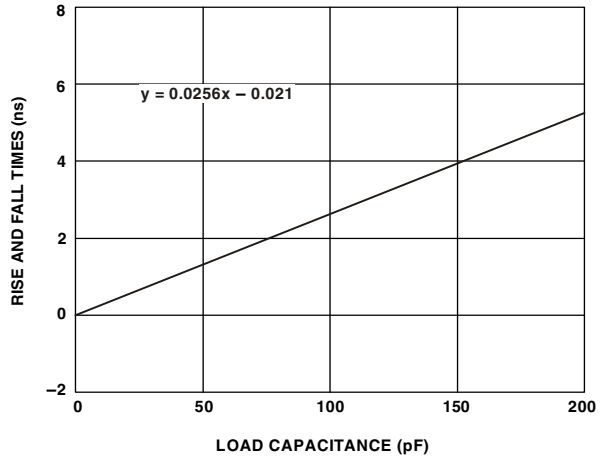

Figure 48. SDCLK Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

THERMAL CHARACTERISTICS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 43 and Table 44 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-9 (BGA_ED) and JESD51-8 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

The LQFP-EP package requires thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{TOP} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{TOP} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 43 and Table 44.

P_D = power dissipation (see Engineer-to-Engineer Note EE-299)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required. This is only applicable when a heat sink is used.

Values of θ_{JB} are provided for package comparison and PCB design considerations. The thermal characteristics values provided in Table 43 and Table 44 are modeled values @ 2 W.

Table 43. Thermal Characteristics for 256-Ball BGA_ED

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	12.5	°C/W
θ_{JMA}	Airflow = 1 m/s	10.6	°C/W
θ_{JMA}	Airflow = 2 m/s	9.9	°C/W
θ_{JC}		0.7	°C/W
θ_{JB}		5.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.3	°C/W

Table 44. Thermal Characteristics for 208-Lead LQFP EPAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W