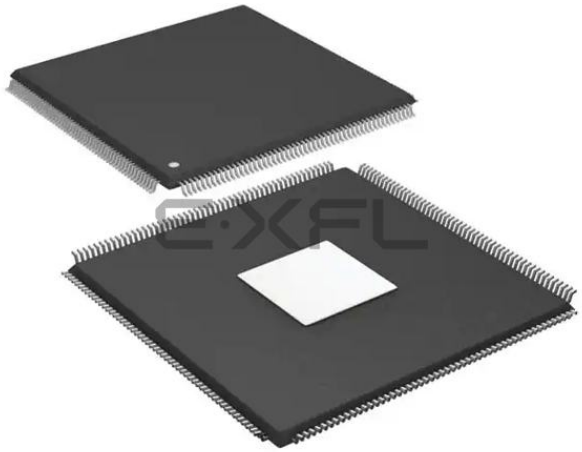

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	266MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21369bswz-1a

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10/13—Rev. E to Rev. F

Updated Development Tools 11

Added Related Signal Chains 12

Corrected $\overline{\text{EMU}}$ pin type from O/T(pu) to O(O/D, pu) in Pin Function Descriptions 13

Corrected Junction Temperature 256-Ball BGA Min Value at ambient temperature (–40°C to +85°C) from 0 to –40 in Operating Conditions 16

Added 400 MHz Min and Max values for Junction Temperature 208-Lead LQFP_EP at ambient temperature 0°C to +70°C in Operating Conditions 16

Added footnote 2 to Table 24 in Memory Read 30

Changed Max values in Table 34 in Pulse-Width Modulation Generators 41

Updated timing parameters in Table 40 and in Figure 36 in SPI Interface—Master 48

Updated Figure 37 in SPI Interface—Slave 49

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To view product/process change notifications (PCNs) related to this data sheet revision, please visit the processor's product page on the www.analog.com website and use the View PCN link.

GENERAL DESCRIPTION

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. These processors are source code-compatible with the ADSP-2126x and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with its large on-chip SRAM, mask programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features[1]

Feature	ADSP-21367	ADSP-21368	ADSP-21369/ ADSP-21369W
Frequency	400 MHz		
RAM	2M bits		
ROM[2]	6M bits		
Audio Decoders in ROM	Yes		
Pulse-Width Modulation	Yes		
S/PDIF	Yes		
SDRAM Memory Bus Width	32/16 bits		
Serial Ports	8		
IDP	Yes		
DAI	Yes		
UART	2		
DAI	Yes		
DPI	Yes		
S/PDIF Transceiver	1		
AMI Interface Bus Width	32/16/8 bits		
SPI	2		
TWI	Yes		
SRC Performance	128 dB		
Package	256 Ball-BGA, 208-Lead LQFP_EP	256 Ball-BGA	256 Ball-BGA, 208-Lead LQFP_EP

[1] W = Automotive grade product. See Automotive Products on Page 61 for more information.

[2] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-21367/ADSP-21368/ADSP-21369 processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (2M bit)
- On-chip mask-programmable ROM (6M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21367/ADSP-21368/ADSP-21369 architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-21368 SHARC Processor Hardware Reference* and the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 8: A = asynchronous, G = ground, I = input, O = output, O/T = output three-state, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, (pd) = pull-down resistor, (pu) = pull-up resistor.

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors use extensive pin multiplexing to achieve a lower pin count. For complete information on the multiplexing scheme, see the *ADSP-21368 SHARC Processor Hardware Reference*, "System Design" chapter.

Table 8. Pin Descriptions

Name	Type	State During/ After Reset (ID = 00x)	Description
$ADDR_{23-0}$	O/T (pu)[1]	Pulled high/ driven low	**External Address.** The processors output addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)[1]	Pulled high/ pulled high	**External Data.** Data pins can be multiplexed to support external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default). When configured using the IDP_PDAP_CTL register, IDP Channel 0 scans the external port data pins for parallel input data.
ACK	I (pu)[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (pu)[1]	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. See the processor hardware reference for more information.
$\overline{RD}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processors read a word from external memory.
$\overline{WR}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processors write a word to external memory.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request 0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request 1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS}_2$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/Memory Select 2.**
FLAG[3]/ TMREXP/$\overline{MS}_3$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select 3.**

Table 8. Pin Descriptions (Continued)

Name	Type	State During/ After Reset (ID = 00x)	Description
$\overline{\text{SDRAS}}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.
SDCKE	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (pu)[1]	Pulled high/ driven low	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK0	O/T	High-Z/driving	**SDRAM Clock Output 0.** Clock driver for this pin differs from all other clock drivers. See Figure 40 on Page 51.
SDCLK1	O/T		**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated. Clock driver for this pin differs from all other clock drivers. See Figure 40 on Page 51. The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
DAI _P_{20-1}	I/O with programmable pu[2]	Pulled high/ pulled high	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin, and to the pin's output enable. The configuration registers then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports (8), the SRC module, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins. Pull-ups can be disabled via the DAI_PIN_PULLUP register.
DPI _P_{14-1}	I/O with programmable pu[2]	Pulled high/ pulled high	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (3), SPIs (2), UARTs (2), flags (12) TWI (1), and general-purpose I/O (9) to the DPI_P14–1 pins. The TWI output is an open-drain output—so the pins used for I^2C data and clock should be connected to logic level 0. Pull-ups can be disabled via the DPI_PIN_PULLUP register.
TDI	I (pu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up, or held low for proper operation of the processor
$\overline{\text{TRST}}$	I (pu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.

Power-Up Sequencing

The timing requirements for processor start-up are given in Table 12. Note that during power-up, a leakage current of approximately 200µA may be observed on the $\overline{\text{RESET}}$ pin if it is driven low before power up is complete. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 12. Power-Up Sequencing Timing Requirements (Processor Start-up)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require $\overline{\text{RESET}}$ to be held low a minimum of four CLKIN cycles in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{srst} specification in Table 14. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

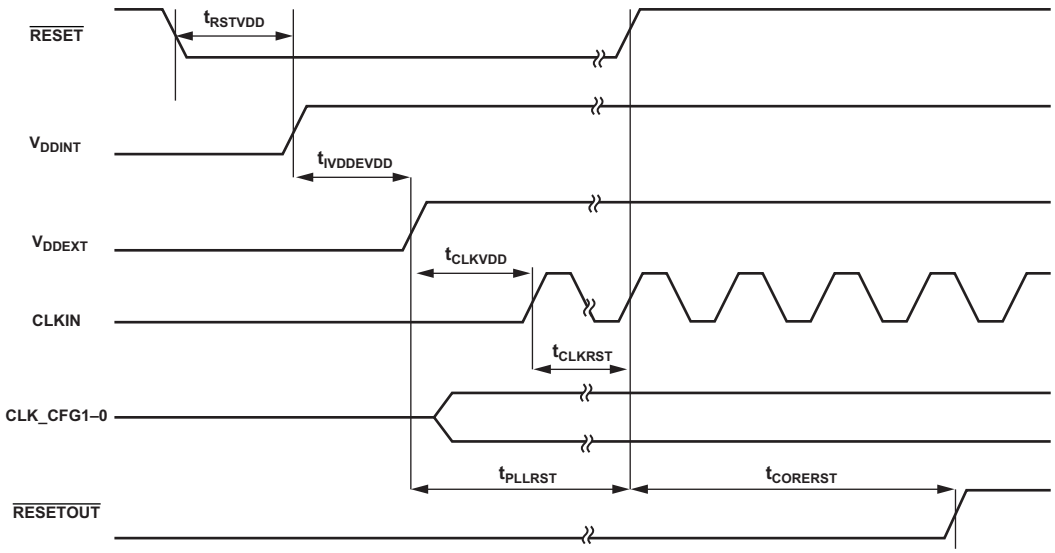


Figure 6. Power-Up Sequencing

Clock Input

Table 13. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	366 MHz[2] Min	366 MHz[2] Max	350 MHz[3] Min	350 MHz[3] Max	333 MHz[4] Min	333 MHz[4] Max	266 MHz[5] Min	266 MHz[5] Max	Unit
Timing Requirements												
t_{CK}	CLKIN Period	15[6]	100	16.39[6]	100	17.14[6]	100	18[6]	100	22.5[6]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	8.1[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3		3	ns
t_{CCLK}[7]	CCLK Period	2.5[6]	10	2.73[6]	10	2.85[6]	10	3.0[6]	10	3.75[6]	10	ns
f_{VCO}[8]	VCO Frequency	100	800	100	800	100	800	100	800	100	600	MHz
t_{CKJ}[9, 10]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 61.
[2] Applies to all 366 MHz models. See Ordering Guide on Page 61.
[3] Applies to all 350 MHz models. See Ordering Guide on Page 61.
[4] Applies to all 333 MHz models. See Ordering Guide on Page 61.
[5] Applies to all 266 MHz models. See Ordering Guide on Page 61.
[6] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[7] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[8] See Figure 5 on Page 19 for VCO diagram.
[9] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[10] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

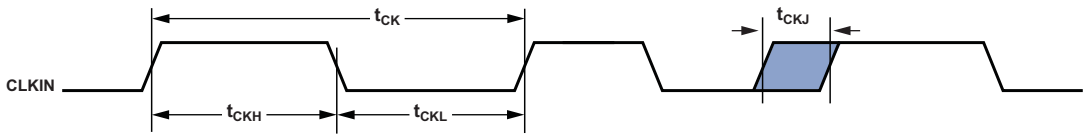


Figure 7. Clock Input

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 16. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 17. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

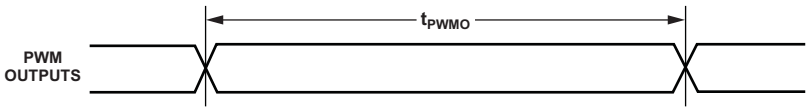


Figure 12. Timer PWM_OUT Timing

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

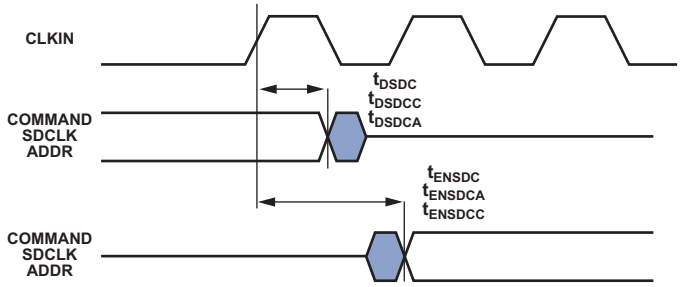


Figure 18. SDRAM Interface Enable/Disable Timing

Memory Read

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 24. Memory Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W + t_{SDCLK} –5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[2]		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3, 4]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[1, 5]		t_{SDCLK} –9.5 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RH + 0.20		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[1]	t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI =RHC + IC (RHC = number of read hold cycles specified in AMICTLx register) × t_{SDCLK}.
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] The falling edge of $\overline{MS}$x is referenced.
[2] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Test Conditions on Page 51 for the calculation of hold times given capacitive and dc loads.
[5] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.

Asynchronous Memory Interface (AMI) Enable/Disable

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 26. AMI Enable/Disable

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{ENAMIAC}$	Address/Control Enable After Clock Rise	4		ns
t_{ENAMID}	Data Enable After Clock Rise	t_{SDCLK} + 4		ns
$t_{DISAMIAC}$	Address/Control Disable After Clock Rise		8.7	ns
$t_{DISAMID}$	Data Disable After Clock Rise		0	ns

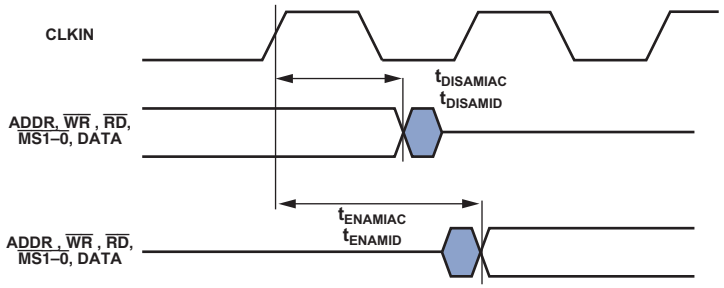


Figure 21. AMI Enable/Disable

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals SCLK, frame sync (FS), data channel A, data channel B are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. Serial Ports—External Clock

Parameter		400 MHz 366 MHz 350 MHz Min	400 MHz 366 MHz 350 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements								
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		2.0		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics								
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)		10.25		10.25		10.25	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)	2		2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8		9.6		9.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Input Data Port

The timing requirements for the IDP are given in Table 32. IDP signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 32. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

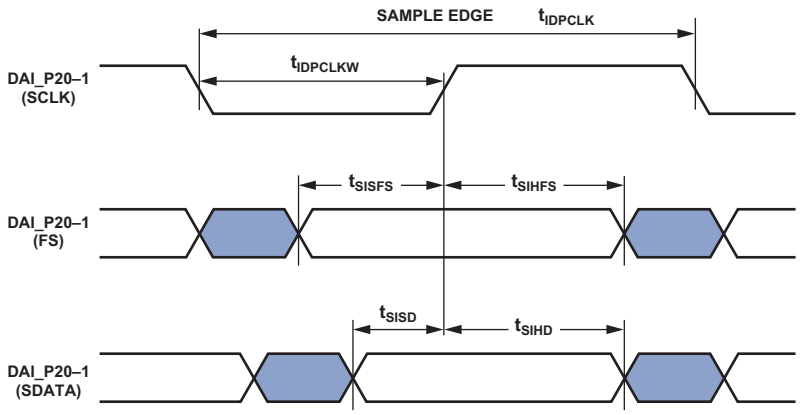


Figure 26. IDP Master Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

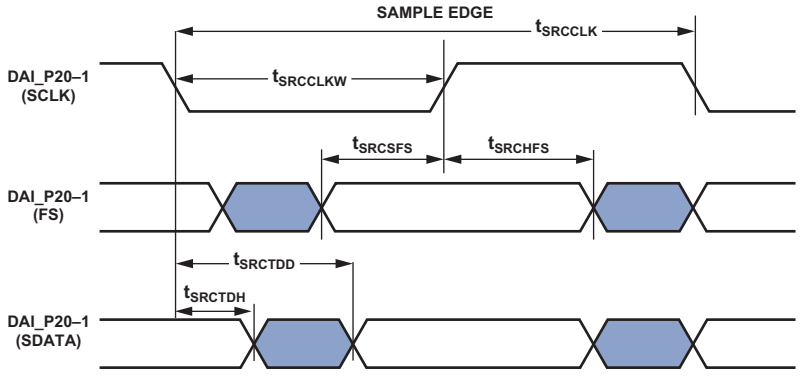


Figure 30. SRC Serial Output Port Timing

SPI Interface—Master

The processors contain two SPI ports. The primary has dedicated pins and the secondary is available through the DPI. The timing provided in Table 40 and Table 41 on Page 49 applies to both.

Table 40. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

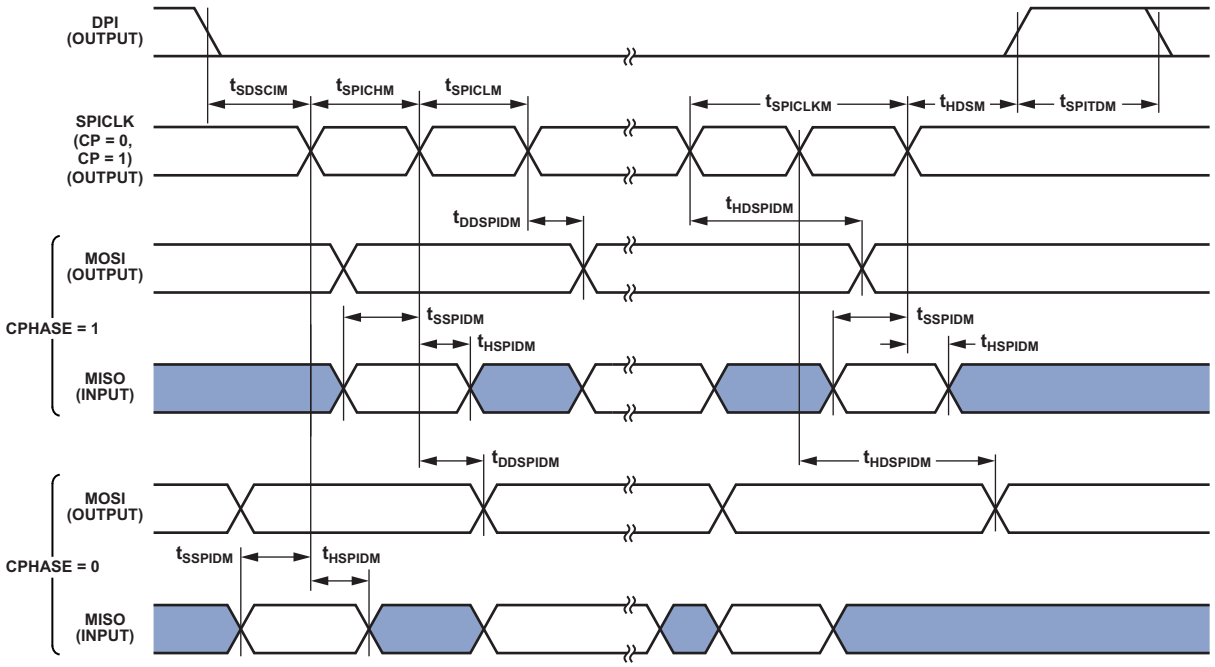


Figure 36. SPI Master Timing

OUTPUT DRIVE CURRENTS

Figure 39 shows typical I-V characteristics for the output drivers and Figure 40 shows typical I-V characteristics for the SDCLK output drivers. The curves represent the current drive capability of the output drivers as a function of output voltage.

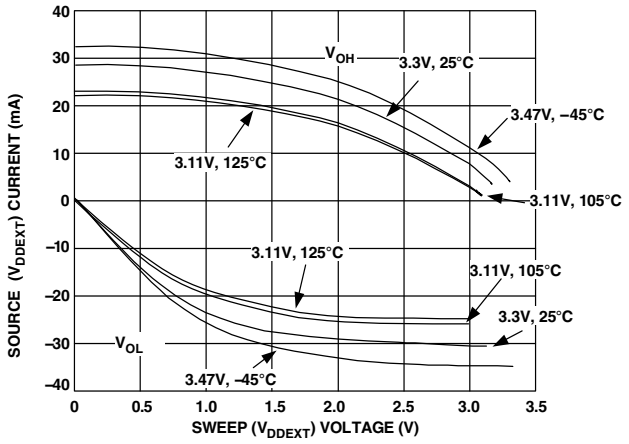


Figure 39. Typical Drive at Junction Temperature

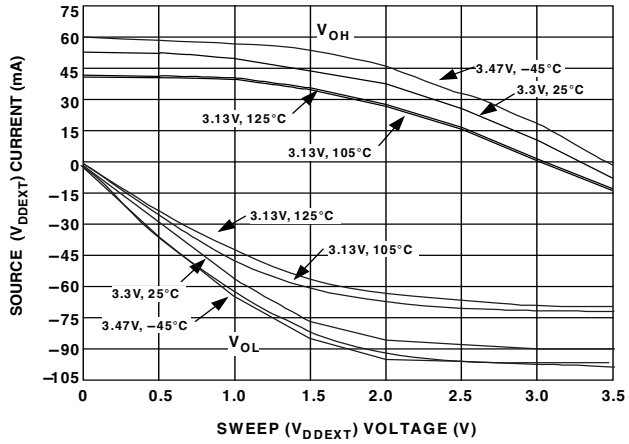


Figure 40. SDCLK1–0 Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 14 on Page 23 through Table 42 on Page 50. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 41.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 41. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

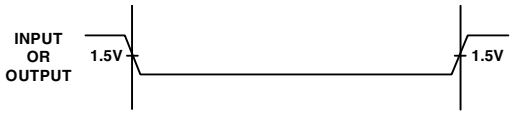
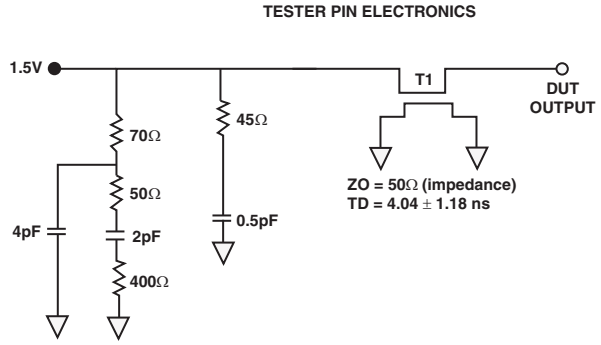


Figure 41. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 42). Figure 47 and Figure 48 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 43 through Figure 48 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

256-BALL BGA_ED PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI_P05 (SD1A)	C01	DAI_P09 (SD2A)	D01	DAI_P10 (SD2B)
A02	TDI	B02	SDCLK1[1]	C02	DAI_P07 (SCLK1)	D02	DAI_P06 (SD1B)
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	V_{DDEXT}	D04	V_{DDEXT}
A05	CLK_CFG1	B05	BOOT_CFG0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOT_CFG1	C06	GND	D06	V_{DDEXT}
A07	DAI_P04 (SFS0)	B07	TDO	C07	V_{DDINT}	D07	V_{DDINT}
A08	DAI_P01 (SD0A)	B08	DAI_P03 (SCLK0)	C08	GND	D08	GND
A09	DPI_P14 (TIMER1)	B09	DAI_P02 (SD0B)	C09	GND	D09	V_{DDEXT}
A10	DPI_P12 (TWI_CLK)	B10	DPI_P13 (TIMER0)	C10	V_{DDINT}	D10	V_{DDINT}
A11	DPI_P10 (UART0RX)	B11	DPI_P11 (TWI_DATA)	C11	GND	D11	GND
A12	DPI_P09 (UART0TX)	B12	DPI_P08 (SPIFLG3)	C12	GND	D12	V_{DDEXT}
A13	DPI_P07 (SPIFLG2)	B13	DPI_P05 (SPIFLG0)	C13	V_{DDINT}	D13	V_{DDINT}
A14	DPI_P06 (SPIFLG1)	B14	DPI_P04 (SPIDS)	C14	GND	D14	GND
A15	DPI_P03 (SPICLK)	B15	DPI_P01 (SPIMOSI)	C15	GND	D15	V_{DDEXT}
A16	DPI_P02 (SPIMISO)	B16	$\overline{\text{RESET}}$	C16	V_{DDINT}	D16	GND
A17	$\overline{\text{RESETOUT}}$	B17	DATA30	C17	V_{DDINT}	D17	V_{DDEXT}
A18	DATA31	B18	DATA29	C18	V_{DDINT}	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC/RPBA[2]	D20	DATA24
E01	DAI_P11 (SD3A)	F01	DAI_P14 (SFS3)	G01	DAI_P15 (SD4A)	H01	DAI_P17 (SD5A)
E02	DAI_P08 (SFS1)	F02	DAI_P12 (SD3B)	G02	DAI_P13 (SCLK3)	H02	DAI_P16 (SD4B)
E03	V_{DDINT}	F03	GND	G03	GND	H03	V_{DDINT}
E04	V_{DDINT}	F04	GND	G04	V_{DDEXT}	H04	V_{DDINT}
E17	GND	F17	V_{DDEXT}	G17	V_{DDINT}	H17	V_{DDEXT}
E18	GND	F18	GND	G18	V_{DDINT}	H18	GND
E19	DATA25	F19	GND/ID2[2]	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI_P19 (SCLK5)	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI_P18 (SD5B)	K02	DAI_P20 (SFS5)	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	V_{DDINT}	M03	GND
J04	GND	K04	V_{DDEXT}	L04	V_{DDINT}	M04	GND
J17	GND	K17	V_{DDINT}	L17	V_{DDINT}	M17	V_{DDEXT}
J18	GND	K18	V_{DDINT}	L18	V_{DDINT}	M18	GND
J19	GND/ID1[2]	K19	GND/ID0[2]	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13

208-LEAD LQFP_EP PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDINT}	43	V_{DDINT}	85	V_{DDEXT}	127	V_{DDINT}	169	CLK_CFG0
2	DATA28	44	DATA4	86	GND	128	GND	170	BOOT_CFG0
3	DATA27	45	DATA5	87	V_{DDINT}	129	V_{DDEXT}	171	CLK_CFG1
4	GND	46	DATA2	88	ADDR14	130	DAI_P19 (SCLK5)	172	$\overline{EMU}$
5	V_{DDEXT}	47	DATA3	89	GND	131	DAI_P18 (SD5B)	173	BOOT_CFG1
6	DATA26	48	DATA0	90	V_{DDEXT}	132	DAI_P17 (SD5A)	174	TDO
7	DATA25	49	DATA1	91	ADDR15	133	DAI_P16 (SD4B)	175	DAI_P04 (SFS0)
8	DATA24	50	V_{DDEXT}	92	ADDR16	134	DAI_P15 (SD4A)	176	DAI_P02 (SD0B)
9	DATA23	51	GND	93	ADDR17	135	DAI_P14 (SFS3)	177	DAI_P03 (SCLK0)
10	GND	52	V_{DDINT}	94	ADDR18	136	DAI_P13 (SCLK3)	178	DAI_P01 (SD0A)
11	V_{DDINT}	53	V_{DDINT}	95	GND	137	DAI_P12 (SD3B)	179	V_{DDEXT}
12	DATA22	54	GND	96	V_{DDEXT}	138	V_{DDINT}	180	GND
13	DATA21	55	V_{DDEXT}	97	ADDR19	139	V_{DDEXT}	181	V_{DDINT}
14	DATA20	56	ADDR0	98	ADDR20	140	GND	182	GND
15	V_{DDEXT}	57	ADDR2	99	ADDR21	141	V_{DDINT}	183	DPI_P14 (TIMER1)
16	GND	58	ADDR1	100	ADDR23	142	GND	184	DPI_P13 (TIMER0)
17	DATA19	59	ADDR4	101	ADDR22	143	DAI_P11 (SD3A)	185	DPI_P12 (TWI_CLK)
18	DATA18	60	ADDR3	102	$\overline{MS1}$	144	DAI_P10 (SD2B)	186	DPI_P11 (TWI_DATA)
19	V_{DDINT}	61	ADDR5	103	$\overline{MS0}$	145	DAI_P08 (SFS1)	187	DPI_P10 (UART0RX)
20	GND	62	GND	104	V_{DDINT}	146	DAI_P09 (SD2A)	188	DPI_P09 (UART0TX)
21	DATA17	63	V_{DDINT}	105	V_{DDINT}	147	DAI_P06 (SD1B)	189	DPI_P08 (SPIFLG3)
22	V_{DDINT}	64	GND	106	GND	148	DAI_P07 (SCLK1)	190	DPI_P07 (SPIFLG2)
23	GND	65	V_{DDEXT}	107	V_{DDEXT}	149	DAI_P05 (SD1A)	191	V_{DDEXT}
24	V_{DDINT}	66	ADDR6	108	$\overline{SDCAS}$	150	V_{DDEXT}	192	GND
25	GND	67	ADDR7	109	$\overline{SDRAS}$	151	GND	193	V_{DDINT}
26	DATA16	68	ADDR8	110	SDCKE	152	V_{DDINT}	194	GND
27	DATA15	69	ADDR9	111	$\overline{SDWE}$	153	GND	195	DPI_P06 (SPIFLG1)
28	DATA14	70	ADDR10	112	$\overline{WR}$	154	V_{DDINT}	196	DPI_P05 (SPIFLG0)
29	DATA13	71	GND	113	SDA10	155	GND	197	DPI_P04 (SPIDS)
30	DATA12	72	V_{DDINT}	114	GND	156	V_{DDINT}	198	DPI_P03 (SPICLK)
31	V_{DDEXT}	73	GND	115	V_{DDEXT}	157	V_{DDINT}	199	DPI_P01 (SPIMOSI)
32	GND	74	V_{DDEXT}	116	SDCLK0	158	V_{DDINT}	200	DPI_P02 (SPIMISO)
33	V_{DDINT}	75	ADDR11	117	GND	159	GND	201	$\overline{RESETOUT}$
34	GND	76	ADDR12	118	V_{DDINT}	160	V_{DDINT}	202	$\overline{RESET}$
35	DATA11	77	ADDR13	119	$\overline{RD}$	161	V_{DDINT}	203	V_{DDEXT}
36	DATA10	78	GND	120	ACK	162	V_{DDINT}	204	GND
37	DATA9	79	V_{DDINT}	121	FLAG3	163	TDI	205	DATA30
38	DATA8	80	A_{VSS}	122	FLAG2	164	$\overline{TRST}$	206	DATA31
39	DATA7	81	A_{VDD}	123	FLAG1	165	TCK	207	DATA29

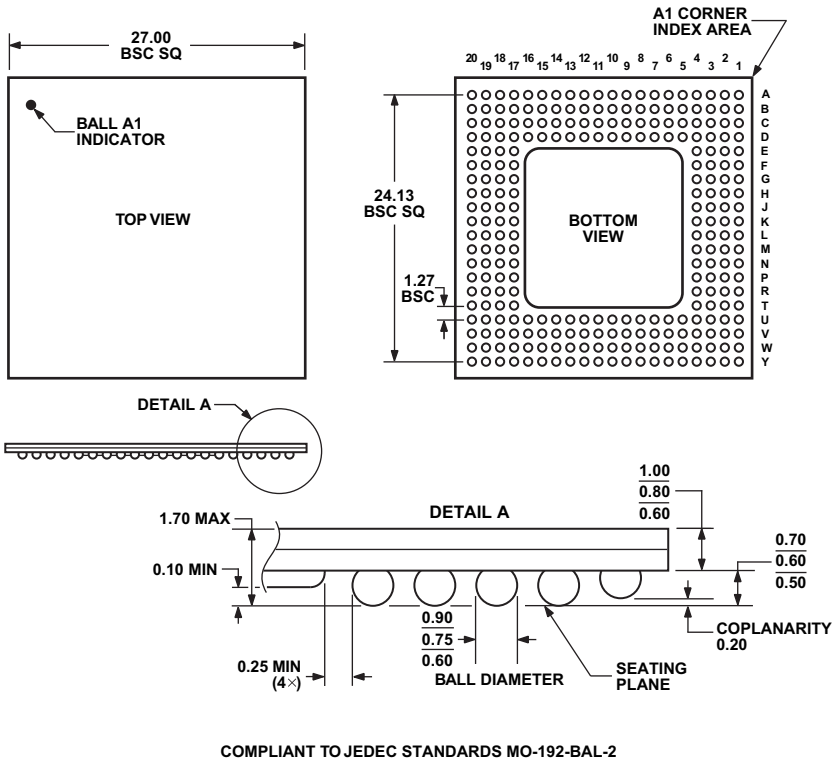


Figure 52. 256-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-256)
Dimension shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA_ED Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Lead Ball Grid Array BGA_ED (BP-256)	Solder Mask Defined (SMD)	0.63 mm	0.73 mm

D05267-0-10/13(F)