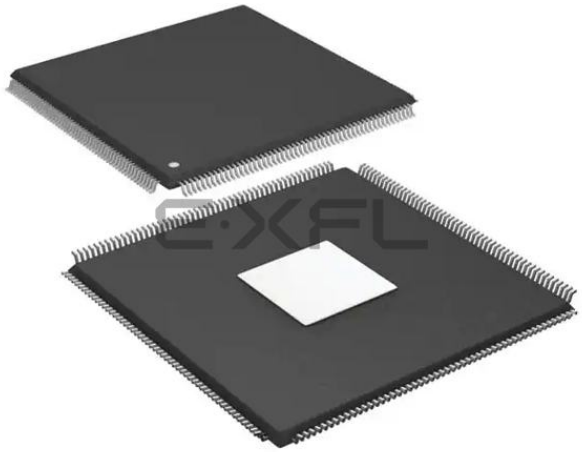

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21369bswz-2a

The block diagram of the ADSP-21368 on Page 1 also shows the peripheral clock domain (also known as the I/O processor) and contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 MTM unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), a input data port (IDP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes three timers, a 2-wire interface, two UARTs, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG) and a flexible signal routing unit (DPI SRU).

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 are code compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21367/ADSP-21368/ADSP-21369 processors share architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

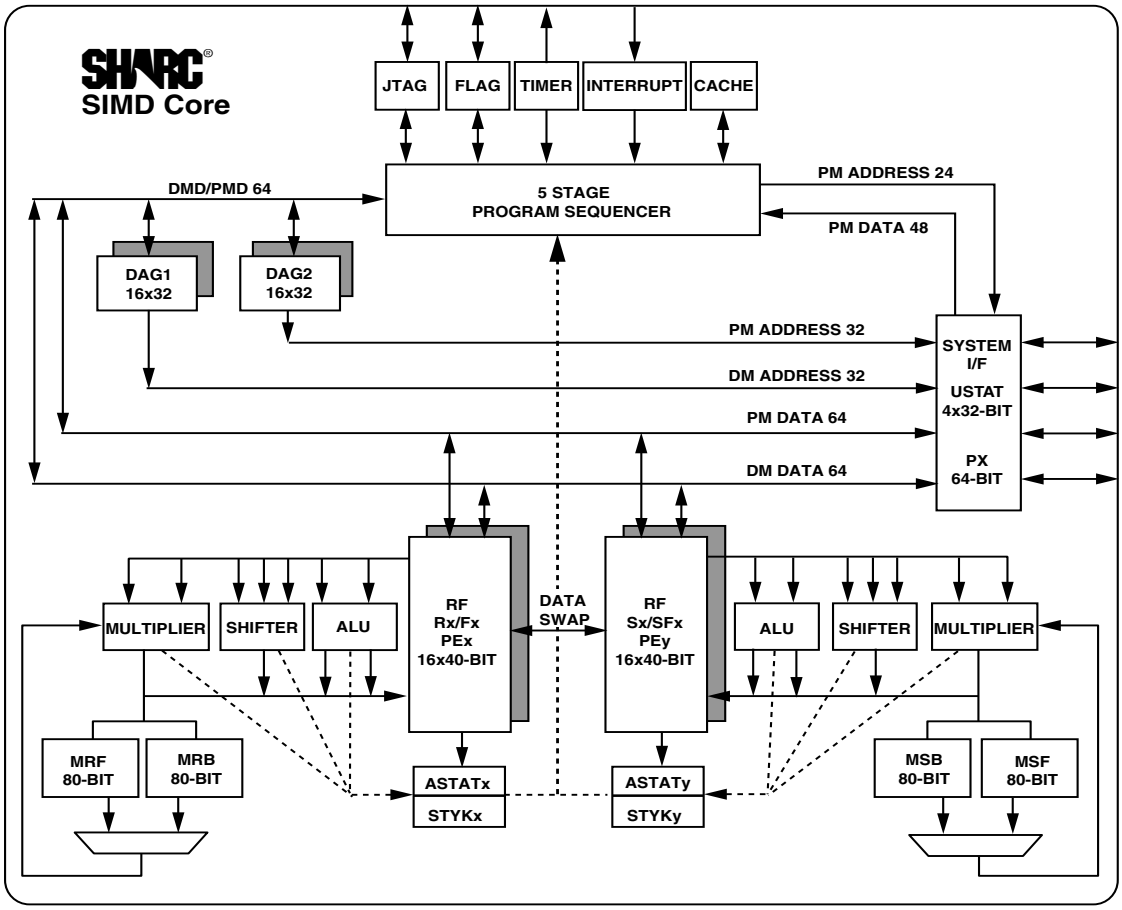

Figure 2. SHARC Core Block Diagram

processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

Table 3. Internal Memory Space [1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 BFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0009 7FFF	Block 0 ROM (Reserved) 0x0010 0000–0x0012 FFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 0 SRAM 0x0004 C000–0x0004 EFFF	Block 0 SRAM 0x0009 0000–0x0009 3FFF	Block 0 SRAM 0x0009 8000–0x0009 DFFF	Block 0 SRAM 0x0013 0000–0x0013 BFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 BFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000B 7FFF	Block 1 ROM (Reserved) 0x0014 0000–0x0016 FFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 1 SRAM 0x0005 C000–0x0005 EFFF	Block 1 SRAM 0x000B 0000–0x000B 3FFF	Block 1 SRAM 0x000B 8000–0x000B DFFF	Block 1 SRAM 0x0017 0000–0x0017 BFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000C 3FFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

[1] The ADSP-21368 and ADSP-21369 processors include a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

The SRAM can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 42k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2x64-bits, core CLK) and the IOD0/1 buses (2x32-bit, PCLK).

ROM-Based Security

The ADSP-21367/ADSP-21368/ADSP-21369 have a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

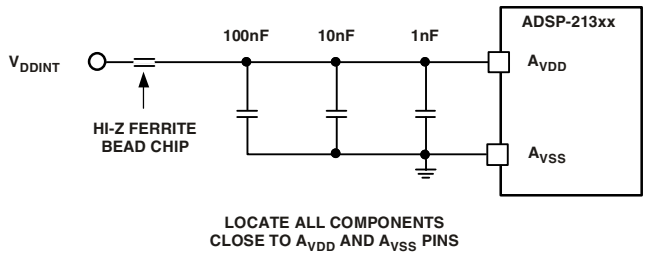

Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21367/ ADSP-21368/ADSP-21369 processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide."

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	400 MHz		366 MHz 350 MHz		333 MHz 266 MHz		Unit
		Min	Max	Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.1	–0.5	+1.1	–0.5	+1.1	V
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to 70°C	0	95	0	110	0	110	°C
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+120	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ 0°C to 70°C	0	95	N/A	N/A	0	105	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+105	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: DATAx, ACK, RPBA, $\overline{BRx}$, IDx, FLAGx, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]			0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{IL}[3, 5, 6]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{IHPD}[5]	High Level Input Current Pull-Down	@ V_{DDEXT} = Max, V_{IN} = 0 V			250	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
$I_{DD-INTYP}$[10]	Supply Current (Internal)	t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25°C		700		mA
		t_{CCLK} = 3.00 ns, V_{DDINT} = 1.2 V, 25°C		900		mA
		t_{CCLK} = 2.85 ns, V_{DDINT} = 1.3 V, 25°C		1050		mA
		t_{CCLK} = 2.73 ns, V_{DDINT} = 1.3 V, 25°C		1080		mA
		t_{CCLK} = 2.50 ns, V_{DDINT} = 1.3 V, 25°C		1100		mA
AI_{DD}[11]	Supply Current (Analog)	A_{VDD} = Max			11	mA
C_{IN}[12, 13]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.3 V			4.7	pF

[1] Applies to output and bidirectional pins: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, FLAGx, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDCLKx, $\overline{EMU}$, TDO.
[2] See Output Drive Currents on Page 51 for typical drive current capabilities.
[3] Applies to input pins without internal pull-ups: BOOT_CFGx, CLK_CFGx, CLKIN, $\overline{RESET}$, TCK.
[4] Applies to input pins with internal pull-ups: ACK, RPBA, TMS, TDI, $\overline{TRST}$.
[5] Applies to input pins with internal pull-downs: IDx.
[6] Applies to input pins with internal pull-ups disabled: ACK, RPBA.
[7] Applies to three-statable pins without internal pull-ups: FLAGx, SDCLKx, TDO.
[8] Applies to three-statable pins with internal pull-ups: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, $\overline{EMU}$.
[9] Applies to three-statable pins with internal pull-ups disabled: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10
[10] See the Engineer-to-Engineer Note "*Estimating Power Dissipation for ADSP-21368 SHARC Processors*" (EE-299) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 13 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = Divider value 1, 2, 4, or 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 11. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. See the peripheral specific timing section for each peripheral's timing information.

Table 11. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the processor hardware reference.

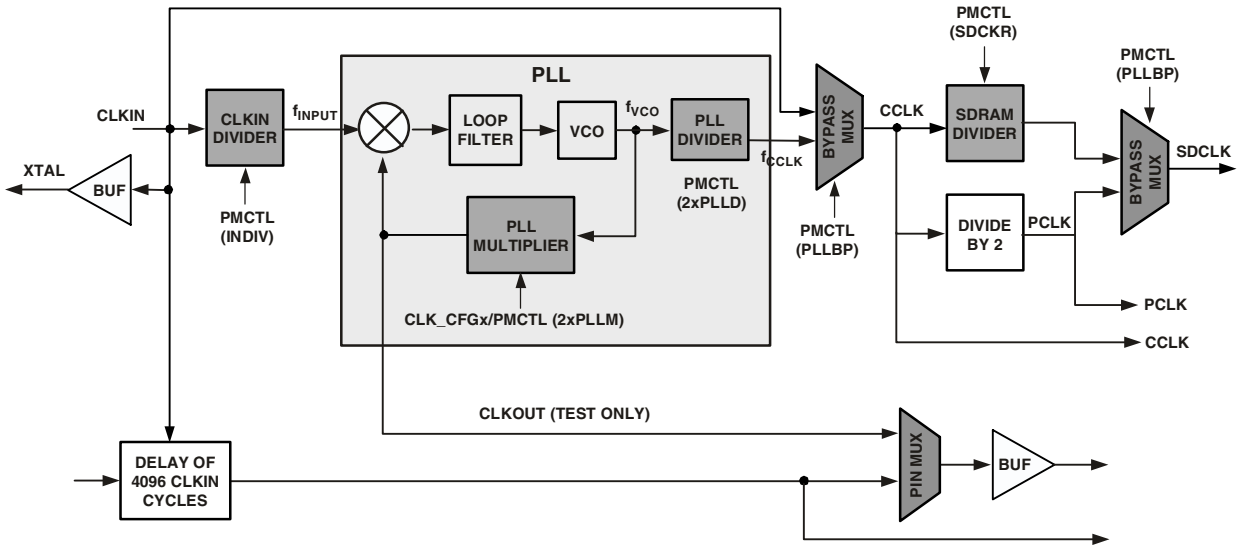

Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor start-up are given in Table 12. Note that during power-up, a leakage current of approximately 200µA may be observed on the $\overline{\text{RESET}}$ pin if it is driven low before power up is complete. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 12. Power-Up Sequencing Timing Requirements (Processor Start-up)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require $\overline{\text{RESET}}$ to be held low a minimum of four CLKIN cycles in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{srst} specification in Table 14. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

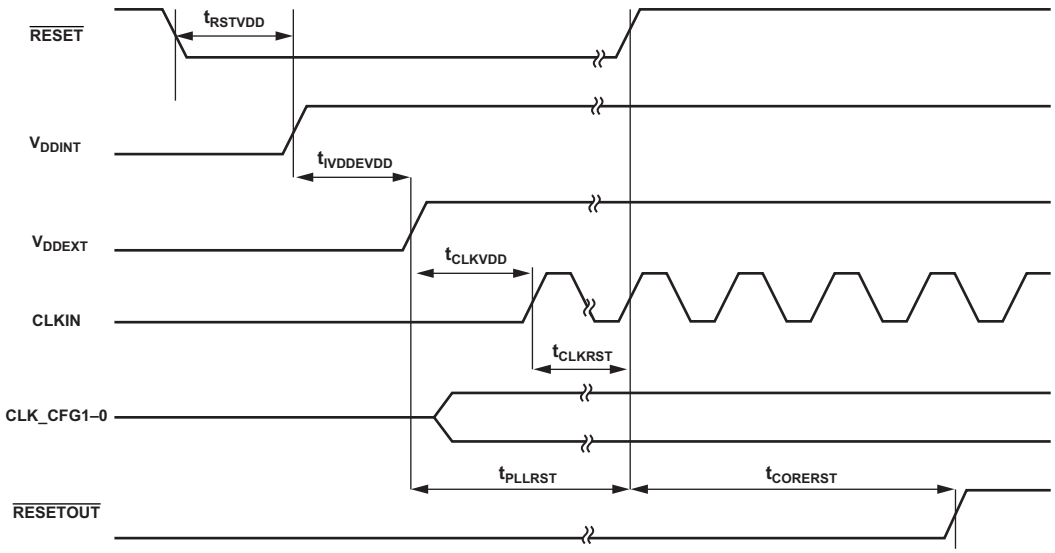

Figure 6. Power-Up Sequencing

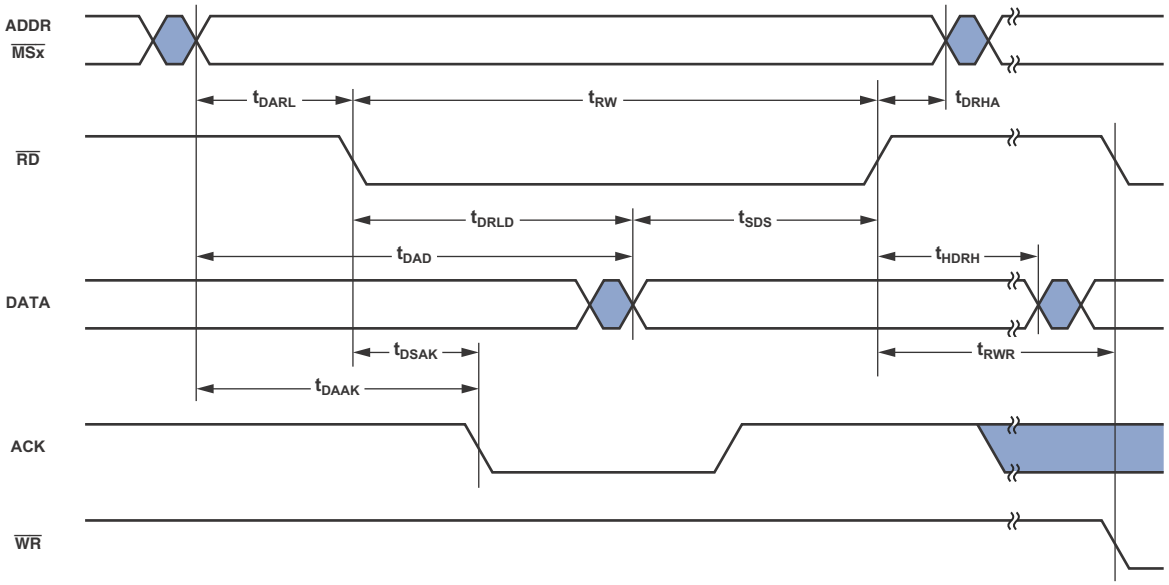

Figure 19. Memory Read

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals SCLK, frame sync (FS), data channel A, data channel B are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. Serial Ports—External Clock

Parameter		400 MHz 366 MHz 350 MHz Min	400 MHz 366 MHz 350 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements								
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		2.0		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics								
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)		10.25		10.25		10.25	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)	2		2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8		9.6		9.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 29. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		4	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCLKIW}[3]	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] Minimum SPORT divisor register value.

Table 30. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

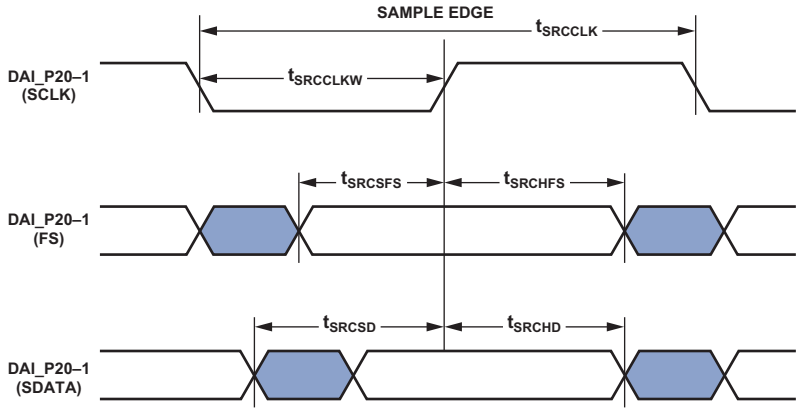

Figure 29. SRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

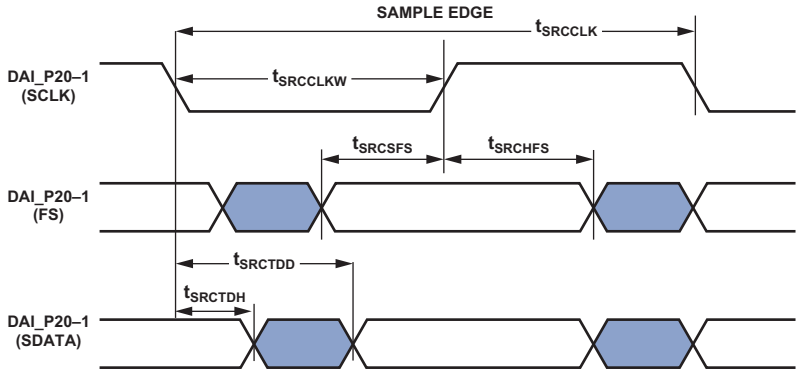

Figure 30. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

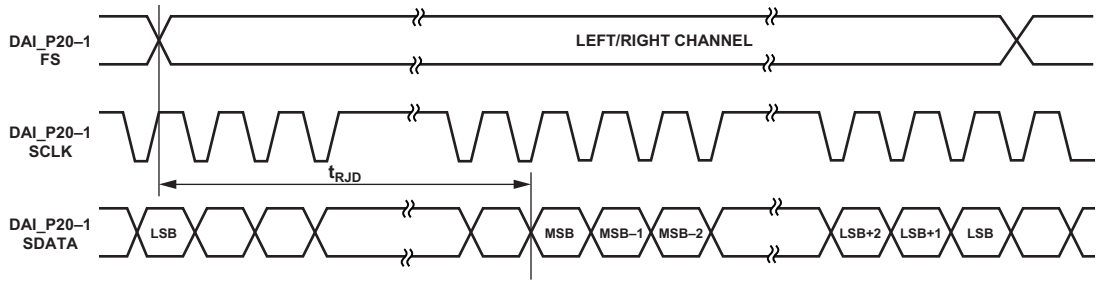

Figure 31. Right-Justified Mode

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

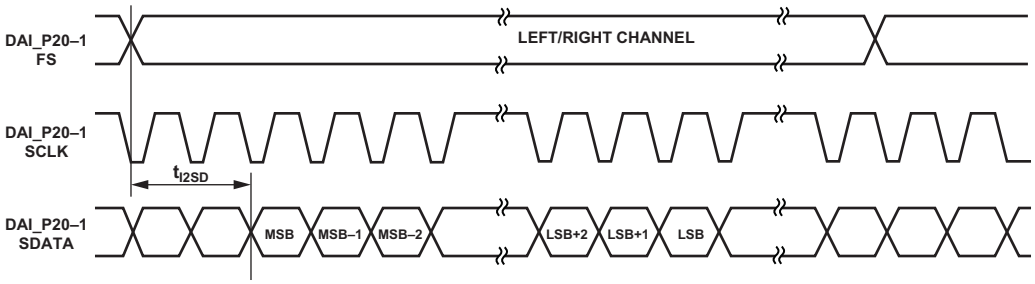

Figure 32. I²S-Justified Mode

SPI Interface—Master

The processors contain two SPI ports. The primary has dedicated pins and the secondary is available through the DPI. The timing provided in Table 40 and Table 41 on Page 49 applies to both.

Table 40. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

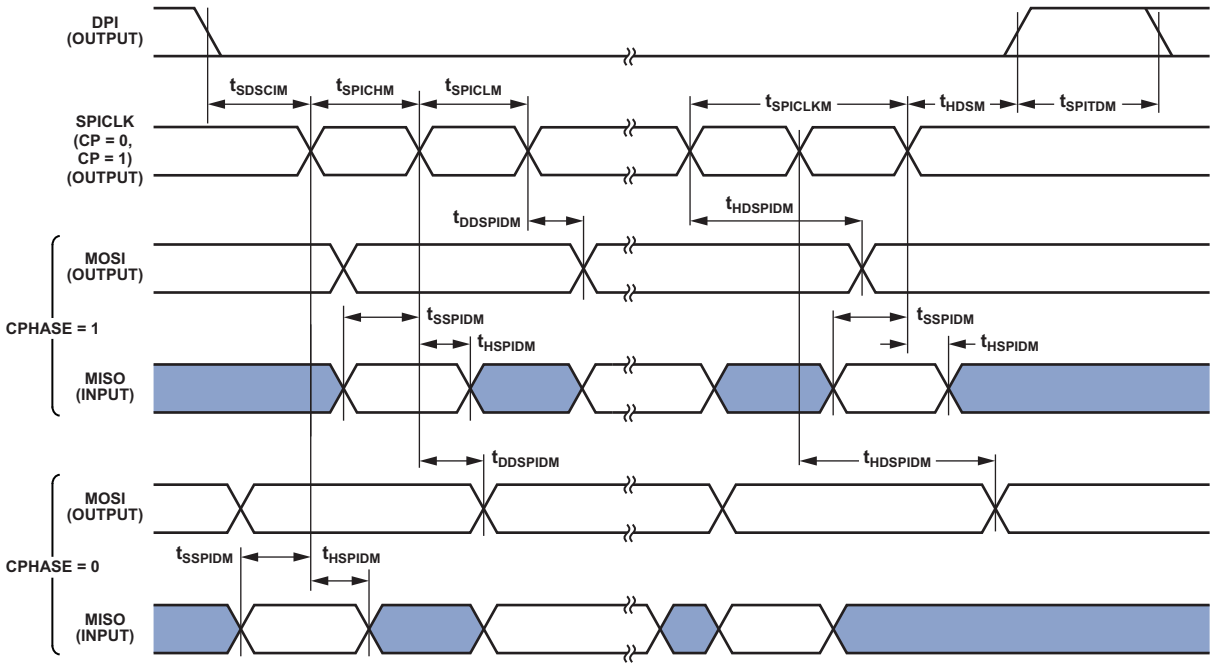

Figure 36. SPI Master Timing

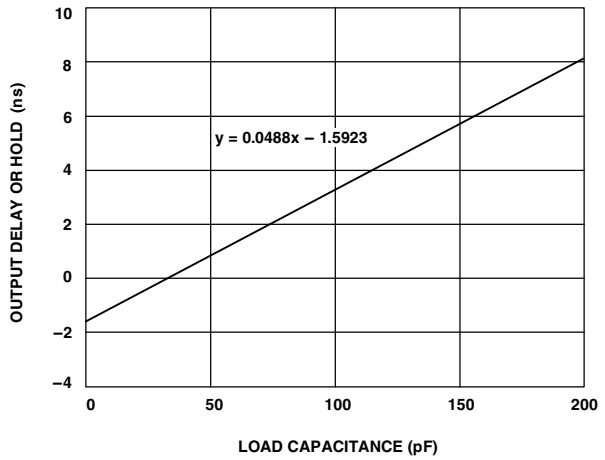

Figure 47. Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

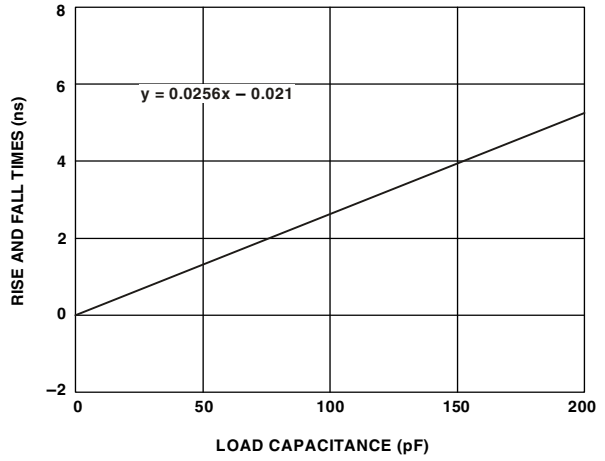

Figure 48. SDCLK Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

THERMAL CHARACTERISTICS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 43 and Table 44 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-9 (BGA_ED) and JESD51-8 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

The LQFP-EP package requires thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{TOP} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{TOP} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 43 and Table 44.

P_D = power dissipation (see Engineer-to-Engineer Note EE-299)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required. This is only applicable when a heat sink is used.

Values of θ_{JB} are provided for package comparison and PCB design considerations. The thermal characteristics values provided in Table 43 and Table 44 are modeled values @ 2 W.

Table 43. Thermal Characteristics for 256-Ball BGA_ED

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	12.5	°C/W
θ_{JMA}	Airflow = 1 m/s	10.6	°C/W
θ_{JMA}	Airflow = 2 m/s	9.9	°C/W
θ_{JC}		0.7	°C/W
θ_{JB}		5.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.3	°C/W

Table 44. Thermal Characteristics for 208-Lead LQFP EPAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N01	$\overline{RD}$	P01	SDA10	R01	$\overline{SDWE}$	T01	SDCKE
N02	SDCLK0	P02	$\overline{WR}$	R02	$\overline{SDRAS}$	T02	$\overline{SDCAS}$
N03	GND	P03	V_{DDINT}	R03	GND	T03	GND
N04	V_{DDEXT}	P04	V_{DDINT}	R04	GND	T04	V_{DDEXT}
N17	GND	P17	V_{DDINT}	R17	V_{DDEXT}	T17	GND
N18	GND	P18	V_{DDINT}	R18	GND	T18	GND
N19	DATA11	P19	DATA8	R19	DATA6	T19	DATA5
N20	DATA10	P20	DATA9	R20	DATA7	T20	DATA4
U01	$\overline{MS0}$	V01	ADDR22	W01	GND	Y01	GND
U02	$\overline{MS1}$	V02	ADDR23	W02	ADDR21	Y02	NC
U03	V_{DDINT}	V03	V_{DDINT}	W03	ADDR19	Y03	NC
U04	GND	V04	GND	W04	ADDR20	Y04	ADDR18
U05	V_{DDEXT}	V05	GND	W05	ADDR17	Y05	NC/$\overline{BR1}$[2]
U06	GND	V06	GND	W06	ADDR16	Y06	NC/$\overline{BR2}$[2]
U07	V_{DDEXT}	V07	GND	W07	ADDR15	Y07	XTAL
U08	V_{DDINT}	V08	V_{DDINT}	W08	ADDR14	Y08	CLKIN
U09	V_{DDEXT}	V09	GND	W09	A_{VDD}	Y09	NC
U10	GND	V10	GND	W10	A_{VSS}	Y10	NC
U11	V_{DDEXT}	V11	GND	W11	ADDR13	Y11	NC/$\overline{BR3}$[2]
U12	V_{DDINT}	V12	V_{DDINT}	W12	ADDR12	Y12	NC/$\overline{BR4}$[2]
U13	V_{DDEXT}	V13	V_{DDEXT}	W13	ADDR10	Y13	ADDR11
U14	V_{DDEXT}	V14	GND	W14	ADDR8	Y14	ADDR9
U15	V_{DDINT}	V15	V_{DDINT}	W15	ADDR5	Y15	ADDR7
U16	V_{DDEXT}	V16	GND	W16	ADDR4	Y16	ADDR6
U17	V_{DDINT}	V17	GND	W17	ADDR1	Y17	ADDR3
U18	V_{DDINT}	V18	GND	W18	ADDR2	Y18	GND
U19	DATA0	V19	DATA1	W19	ADDR0	Y19	GND
U20	DATA2	V20	DATA3	W20	NC	Y20	NC

[1] The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
[2] Applies to ADSP-21368 models only.

208-LEAD LQFP_EP PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDINT}	43	V_{DDINT}	85	V_{DDEXT}	127	V_{DDINT}	169	CLK_CFG0
2	DATA28	44	DATA4	86	GND	128	GND	170	BOOT_CFG0
3	DATA27	45	DATA5	87	V_{DDINT}	129	V_{DDEXT}	171	CLK_CFG1
4	GND	46	DATA2	88	ADDR14	130	DAI_P19 (SCLK5)	172	$\overline{EMU}$
5	V_{DDEXT}	47	DATA3	89	GND	131	DAI_P18 (SD5B)	173	BOOT_CFG1
6	DATA26	48	DATA0	90	V_{DDEXT}	132	DAI_P17 (SD5A)	174	TDO
7	DATA25	49	DATA1	91	ADDR15	133	DAI_P16 (SD4B)	175	DAI_P04 (SFS0)
8	DATA24	50	V_{DDEXT}	92	ADDR16	134	DAI_P15 (SD4A)	176	DAI_P02 (SD0B)
9	DATA23	51	GND	93	ADDR17	135	DAI_P14 (SFS3)	177	DAI_P03 (SCLK0)
10	GND	52	V_{DDINT}	94	ADDR18	136	DAI_P13 (SCLK3)	178	DAI_P01 (SD0A)
11	V_{DDINT}	53	V_{DDINT}	95	GND	137	DAI_P12 (SD3B)	179	V_{DDEXT}
12	DATA22	54	GND	96	V_{DDEXT}	138	V_{DDINT}	180	GND
13	DATA21	55	V_{DDEXT}	97	ADDR19	139	V_{DDEXT}	181	V_{DDINT}
14	DATA20	56	ADDR0	98	ADDR20	140	GND	182	GND
15	V_{DDEXT}	57	ADDR2	99	ADDR21	141	V_{DDINT}	183	DPI_P14 (TIMER1)
16	GND	58	ADDR1	100	ADDR23	142	GND	184	DPI_P13 (TIMER0)
17	DATA19	59	ADDR4	101	ADDR22	143	DAI_P11 (SD3A)	185	DPI_P12 (TWI_CLK)
18	DATA18	60	ADDR3	102	$\overline{MS1}$	144	DAI_P10 (SD2B)	186	DPI_P11 (TWI_DATA)
19	V_{DDINT}	61	ADDR5	103	$\overline{MS0}$	145	DAI_P08 (SFS1)	187	DPI_P10 (UART0RX)
20	GND	62	GND	104	V_{DDINT}	146	DAI_P09 (SD2A)	188	DPI_P09 (UART0TX)
21	DATA17	63	V_{DDINT}	105	V_{DDINT}	147	DAI_P06 (SD1B)	189	DPI_P08 (SPIFLG3)
22	V_{DDINT}	64	GND	106	GND	148	DAI_P07 (SCLK1)	190	DPI_P07 (SPIFLG2)
23	GND	65	V_{DDEXT}	107	V_{DDEXT}	149	DAI_P05 (SD1A)	191	V_{DDEXT}
24	V_{DDINT}	66	ADDR6	108	$\overline{SDCAS}$	150	V_{DDEXT}	192	GND
25	GND	67	ADDR7	109	$\overline{SDRAS}$	151	GND	193	V_{DDINT}
26	DATA16	68	ADDR8	110	SDCKE	152	V_{DDINT}	194	GND
27	DATA15	69	ADDR9	111	$\overline{SDWE}$	153	GND	195	DPI_P06 (SPIFLG1)
28	DATA14	70	ADDR10	112	$\overline{WR}$	154	V_{DDINT}	196	DPI_P05 (SPIFLG0)
29	DATA13	71	GND	113	SDA10	155	GND	197	DPI_P04 (SPIDS)
30	DATA12	72	V_{DDINT}	114	GND	156	V_{DDINT}	198	DPI_P03 (SPICLK)
31	V_{DDEXT}	73	GND	115	V_{DDEXT}	157	V_{DDINT}	199	DPI_P01 (SPIMOSI)
32	GND	74	V_{DDEXT}	116	SDCLK0	158	V_{DDINT}	200	DPI_P02 (SPIMISO)
33	V_{DDINT}	75	ADDR11	117	GND	159	GND	201	$\overline{RESETOUT}$
34	GND	76	ADDR12	118	V_{DDINT}	160	V_{DDINT}	202	$\overline{RESET}$
35	DATA11	77	ADDR13	119	$\overline{RD}$	161	V_{DDINT}	203	V_{DDEXT}
36	DATA10	78	GND	120	ACK	162	V_{DDINT}	204	GND
37	DATA9	79	V_{DDINT}	121	FLAG3	163	TDI	205	DATA30
38	DATA8	80	A_{VSS}	122	FLAG2	164	$\overline{TRST}$	206	DATA31
39	DATA7	81	A_{VDD}	123	FLAG1	165	TCK	207	DATA29

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number) (Continued)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
40	DATA6	82	GND	124	FLAG0	166	GND	208	V_{DDINT}
41	V_{DDEXT}	83	CLKIN	125	DAI_P20 (SFS5)	167	V_{DDINT}		
42	GND	84	XTAL	126	GND	168	TMS		

AUTOMOTIVE PRODUCTS

An ADSP-21369 model is available for automotive applications with controlled manufacturing. Note that this special model may have specifications that differ from the general release models.

The automotive grade product shown in Table 48 is available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 48. Automotive Products

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21369WBSWZ1xx	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1

[1] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21367KBP-2A	[2]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KBPZ-2A	[2, 3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367BBP-2A	[2]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367BBPZ-2A	[2, 3]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KBPZ-3A	[2, 3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KSWZ-1A	[2, 3]	0°C to +70°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367KSWZ-2A	[2, 3]	0°C to +70°C	333 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367KSWZ-4A	[2, 3]	0°C to +70°C	350 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367KSWZ-5A	[2, 3]	0°C to +70°C	366 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367BSWZ-1A	[2, 3]	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21368KBPZ-2A	[3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368BBPZ-2A	[3]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368KBPZ-3A	[3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KBPZ-2A	[3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369BBP-2A		–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369BBPZ-2A	[2]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KBPZ-3A	[3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KSWZ-1A	[3]	0°C to +70°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-2A	[3]	0°C to +70°C	333 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-4A	[3]	0°C to +70°C	350 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-5A	[3]	0°C to +70°C	366 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-6A	[3]	0°C to +70°C	400 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369BSWZ-1A	[3]	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369BSWZ-2A	[3]	–40°C to +85°C	333 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1

[1] Referenced temperature is ambient temperature.
[2] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.
[3] Z = RoHS Compliant Part.