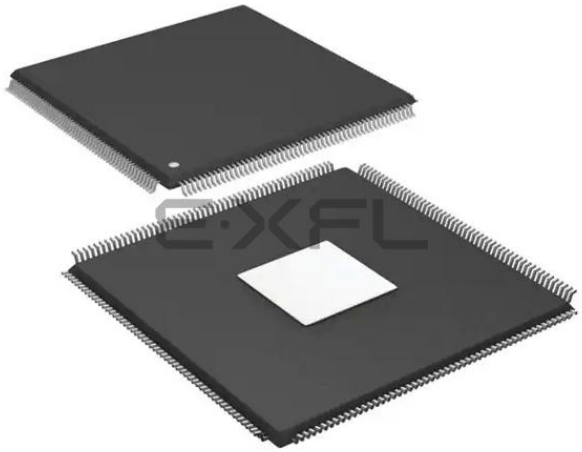

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	266MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21369kswz-1a

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10/13—Rev. E to Rev. F

Updated Development Tools 11

Added Related Signal Chains 12

Corrected $\overline{\text{EMU}}$ pin type from O/T(pu) to O(O/D, pu) in Pin Function Descriptions 13

Corrected Junction Temperature 256-Ball BGA Min Value at ambient temperature (–40°C to +85°C) from 0 to –40 in Operating Conditions 16

Added 400 MHz Min and Max values for Junction Temperature 208-Lead LQFP_EP at ambient temperature 0°C to +70°C in Operating Conditions 16

Added footnote 2 to Table 24 in Memory Read 30

Changed Max values in Table 34 in Pulse-Width Modulation Generators 41

Updated timing parameters in Table 40 and in Figure 36 in SPI Interface—Master 48

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To view product/process change notifications (PCNs) related to this data sheet revision, please visit the processor's product page on the www.analog.com website and use the View PCN link.

GENERAL DESCRIPTION

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. These processors are source code-compatible with the ADSP-2126x and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with its large on-chip SRAM, mask programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features[1]

Feature	ADSP-21367	ADSP-21368	ADSP-21369/ ADSP-21369W
Frequency	400 MHz		
RAM	2M bits		
ROM[2]	6M bits		
Audio Decoders in ROM	Yes		
Pulse-Width Modulation	Yes		
S/PDIF	Yes		
SDRAM Memory Bus Width	32/16 bits		
Serial Ports	8		
IDP	Yes		
DAI	Yes		
UART	2		
DAI	Yes		
DPI	Yes		
S/PDIF Transceiver	1		
AMI Interface Bus Width	32/16/8 bits		
SPI	2		
TWI	Yes		
SRC Performance	128 dB		
Package	256 Ball-BGA, 208-Lead LQFP_EP	256 Ball-BGA	256 Ball-BGA, 208-Lead LQFP_EP

[1] W = Automotive grade product. See Automotive Products on Page 61 for more information.

[2] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-21367/ADSP-21368/ADSP-21369 processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (2M bit)
- On-chip mask-programmable ROM (6M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

Table 3. Internal Memory Space [1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 BFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0009 7FFF	Block 0 ROM (Reserved) 0x0010 0000–0x0012 FFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 0 SRAM 0x0004 C000–0x0004 EFFF	Block 0 SRAM 0x0009 0000–0x0009 3FFF	Block 0 SRAM 0x0009 8000–0x0009 DFFF	Block 0 SRAM 0x0013 0000–0x0013 BFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 BFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000B 7FFF	Block 1 ROM (Reserved) 0x0014 0000–0x0016 FFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 1 SRAM 0x0005 C000–0x0005 EFFF	Block 1 SRAM 0x000B 0000–0x000B 3FFF	Block 1 SRAM 0x000B 8000–0x000B DFFF	Block 1 SRAM 0x0017 0000–0x0017 BFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000C 3FFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

[1] The ADSP-21368 and ADSP-21369 processors include a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

The SRAM can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 42k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2x64-bits, core CLK) and the IOD0/1 buses (2x32-bit, PCLK).

ROM-Based Security

The ADSP-21367/ADSP-21368/ADSP-21369 have a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example, frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Synchronous/Asynchronous Sample Rate Converter

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), two universal asynchronous receiver-transmitters (UARTs), a 2-wire interface (TWI), 12 flags, and three general-purpose timers.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21367/ADSP-21368/ADSP-21369 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for five data bits to eight data bits, one stop bit or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Where the 16-bit UART_Divisor comes from the DLH register (most significant eight bits) and DLL register (least significant eight bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21367/ADSP-21368/ADSP-21369 architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-21368 SHARC Processor Hardware Reference* and the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 8: A = asynchronous, G = ground, I = input, O = output, O/T = output three-state, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, (pd) = pull-down resistor, (pu) = pull-up resistor.

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors use extensive pin multiplexing to achieve a lower pin count. For complete information on the multiplexing scheme, see the *ADSP-21368 SHARC Processor Hardware Reference*, "System Design" chapter.

Table 8. Pin Descriptions

Name	Type	State During/ After Reset (ID = 00x)	Description
$ADDR_{23-0}$	O/T (pu)[1]	Pulled high/ driven low	**External Address.** The processors output addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)[1]	Pulled high/ pulled high	**External Data.** Data pins can be multiplexed to support external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default). When configured using the IDP_PDAP_CTL register, IDP Channel 0 scans the external port data pins for parallel input data.
ACK	I (pu)[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (pu)[1]	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. See the processor hardware reference for more information.
$\overline{RD}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processors read a word from external memory.
$\overline{WR}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processors write a word to external memory.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request 0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request 1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS}_2$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/Memory Select 2.**
FLAG[3]/ TMREXP/$\overline{MS}_3$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select 3.**

Power-Up Sequencing

The timing requirements for processor start-up are given in Table 12. Note that during power-up, a leakage current of approximately 200µA may be observed on the $\overline{\text{RESET}}$ pin if it is driven low before power up is complete. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 12. Power-Up Sequencing Timing Requirements (Processor Start-up)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require $\overline{\text{RESET}}$ to be held low a minimum of four CLKIN cycles in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{srst} specification in Table 14. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

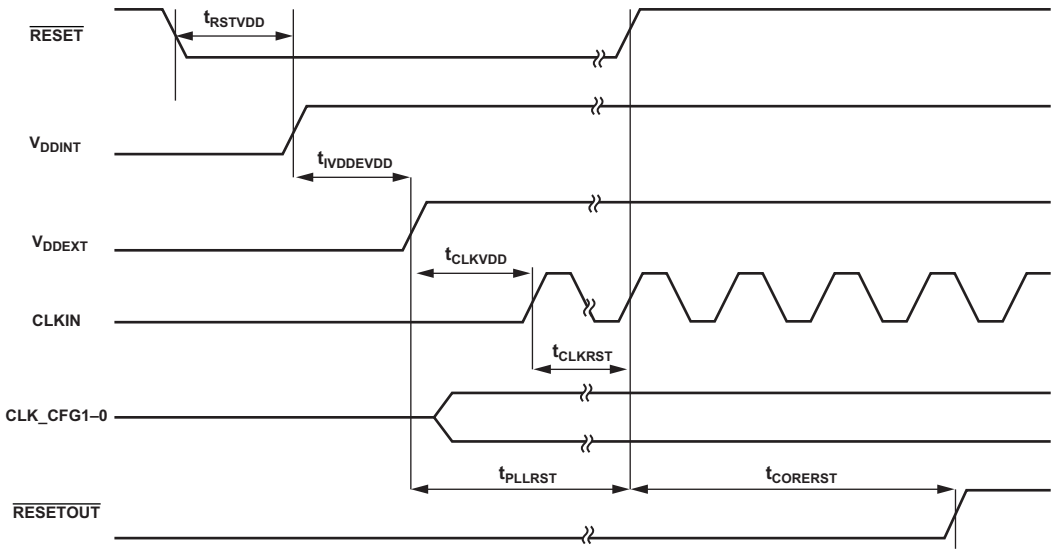


Figure 6. Power-Up Sequencing

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 16. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 17. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

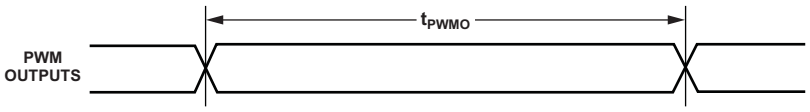


Figure 12. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specification provided in Table 18 is valid at the DPI_P14–1 pins.

Table 18. Timer Width Capture Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

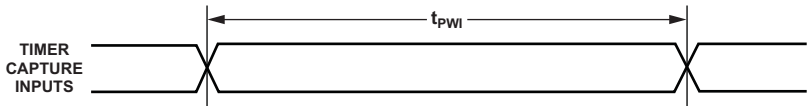


Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 19. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

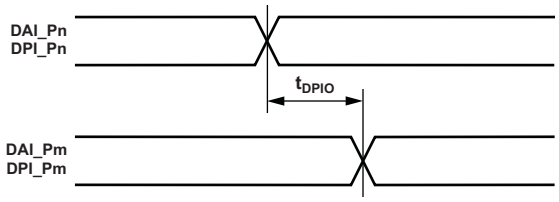


Figure 14. DAI/DPI Pin to Pin Direct Routing

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

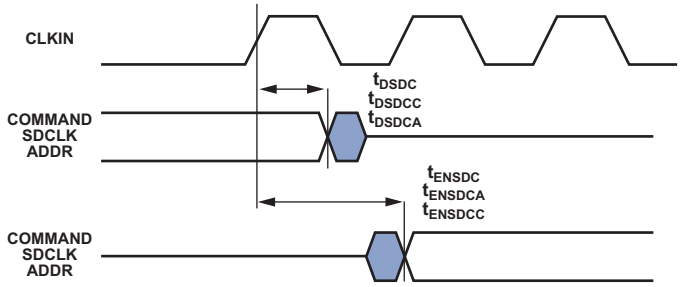


Figure 18. SDRAM Interface Enable/Disable Timing

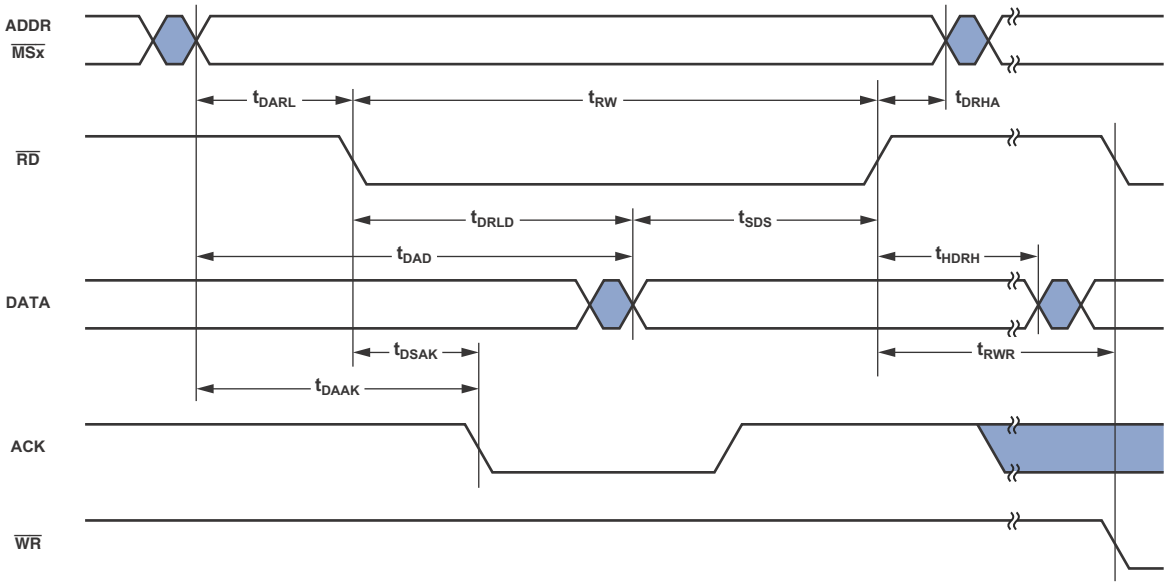


Figure 19. Memory Read

Asynchronous Memory Interface (AMI) Enable/Disable

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 26. AMI Enable/Disable

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{ENAMIAC}$	Address/Control Enable After Clock Rise	4		ns
t_{ENAMID}	Data Enable After Clock Rise	t_{SDCLK} + 4		ns
$t_{DISAMIAC}$	Address/Control Disable After Clock Rise		8.7	ns
$t_{DISAMID}$	Data Disable After Clock Rise		0	ns

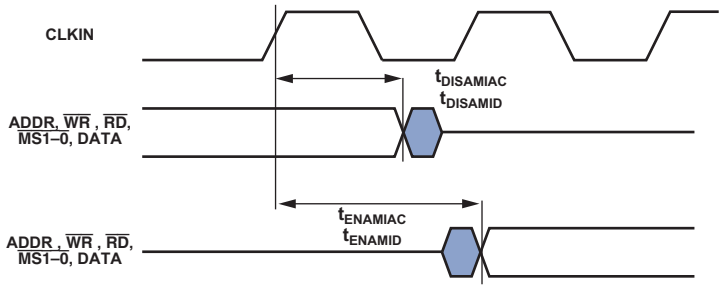


Figure 21. AMI Enable/Disable

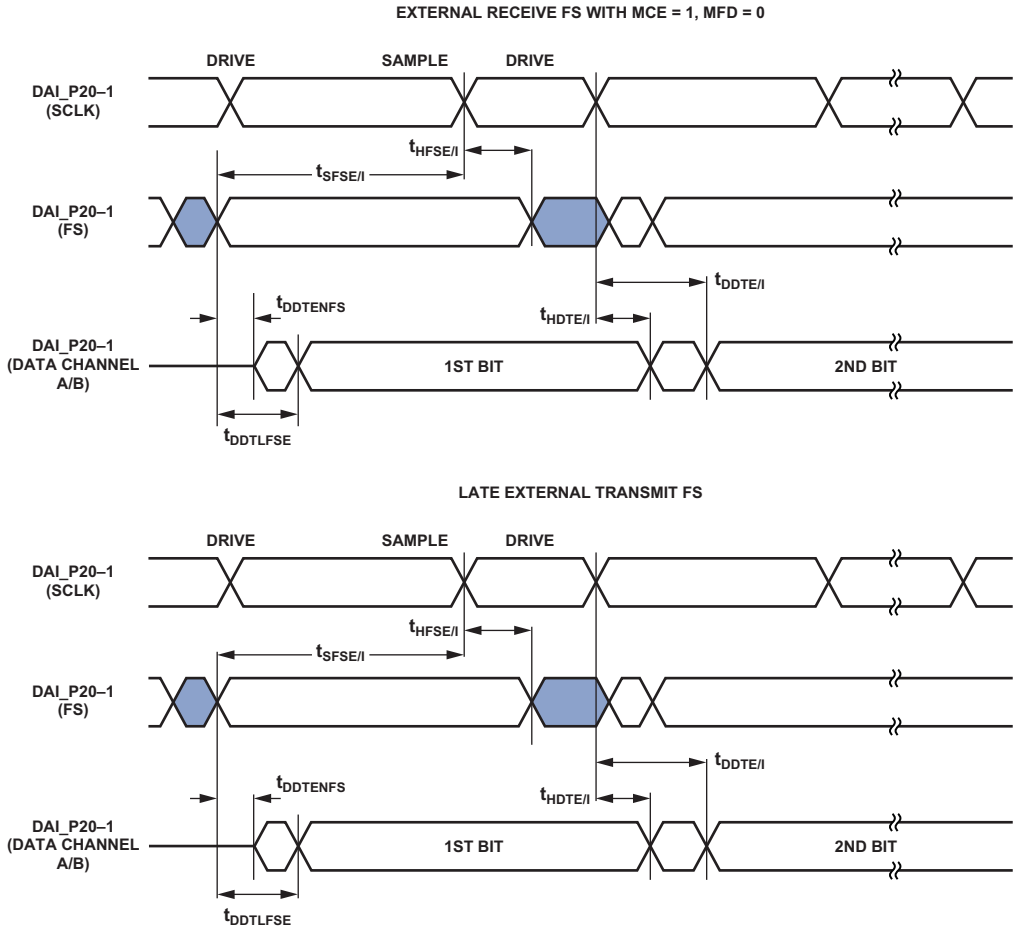


Figure 25. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

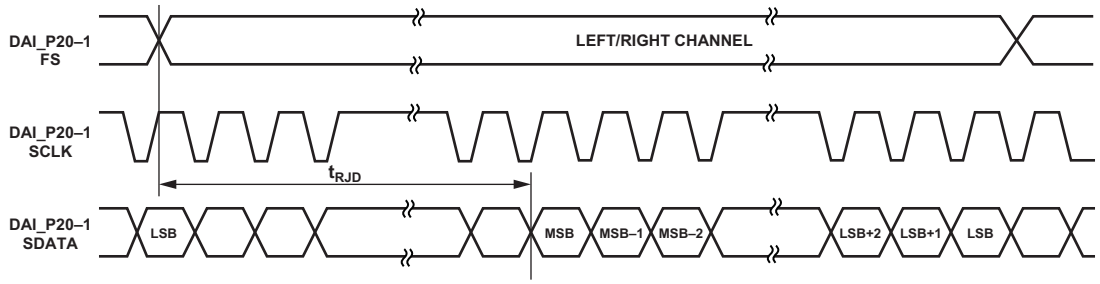


Figure 31. Right-Justified Mode

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

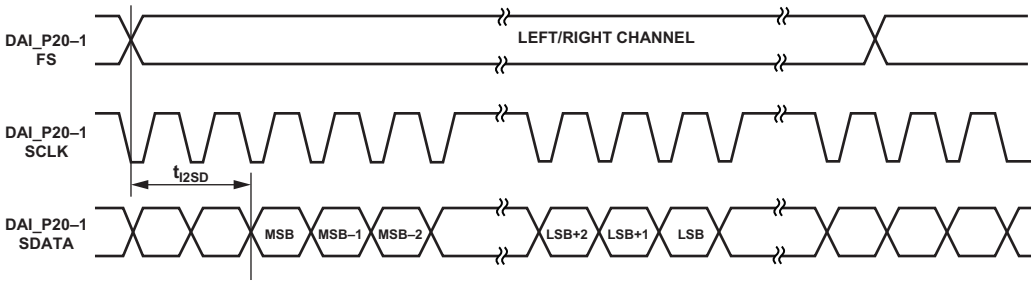


Figure 32. I²S-Justified Mode

Figure 33 shows the left-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

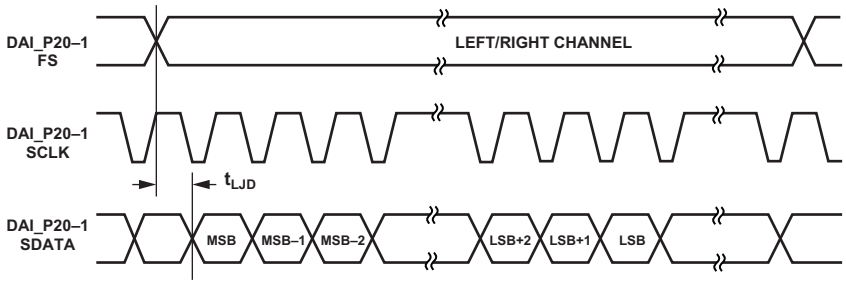


Figure 33. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the input port are given in Table 37. Input signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 37. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	3		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	3		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	3		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	3		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

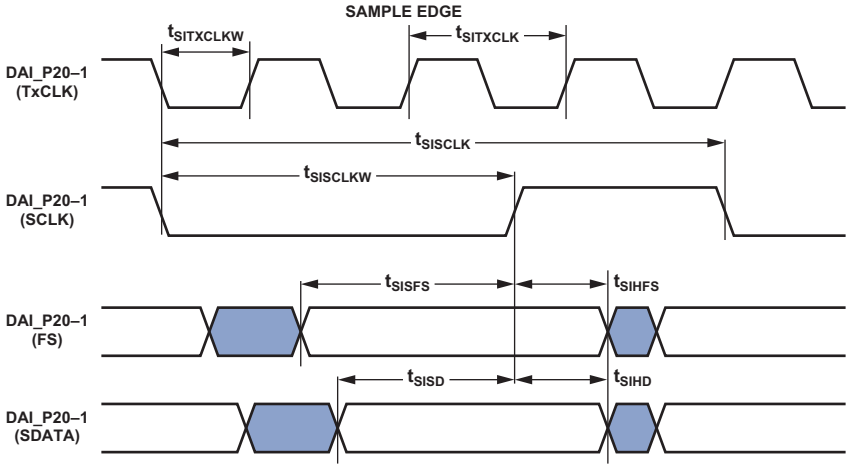


Figure 34. S/PDIF Transmitter Input Timing

JTAG Test Access Port and Emulation

Table 42. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$.

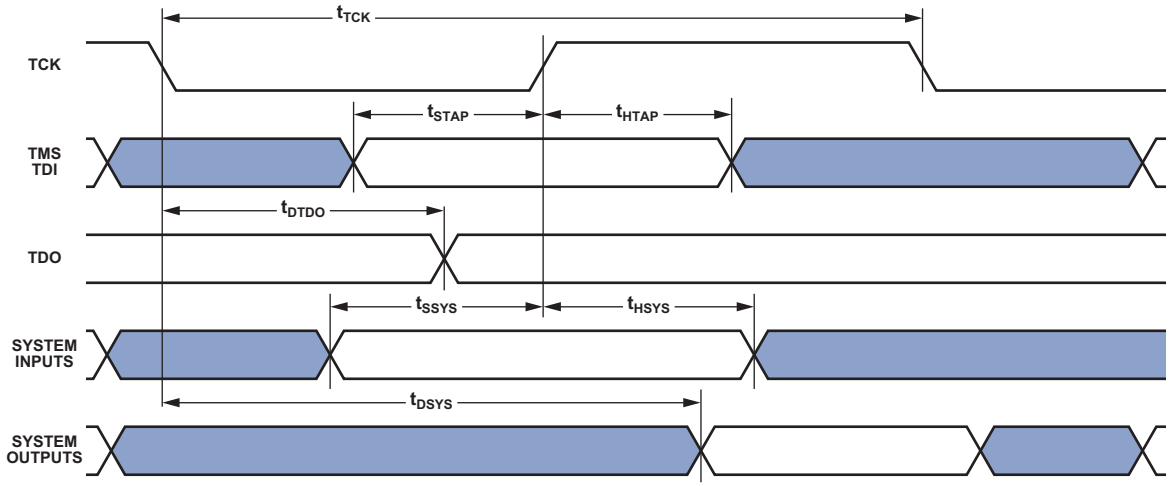


Figure 38. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 39 shows typical I-V characteristics for the output drivers and Figure 40 shows typical I-V characteristics for the SDCLK output drivers. The curves represent the current drive capability of the output drivers as a function of output voltage.

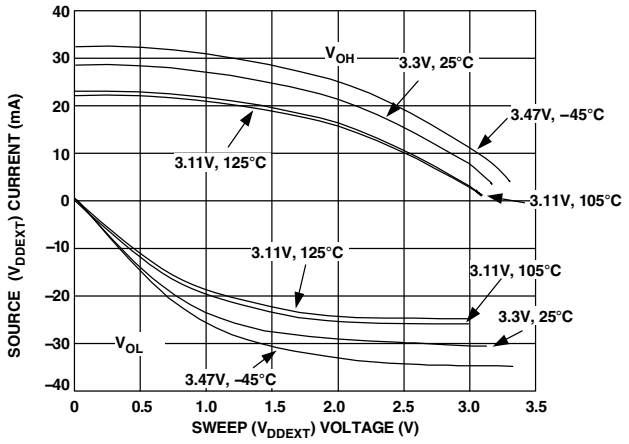


Figure 39. Typical Drive at Junction Temperature

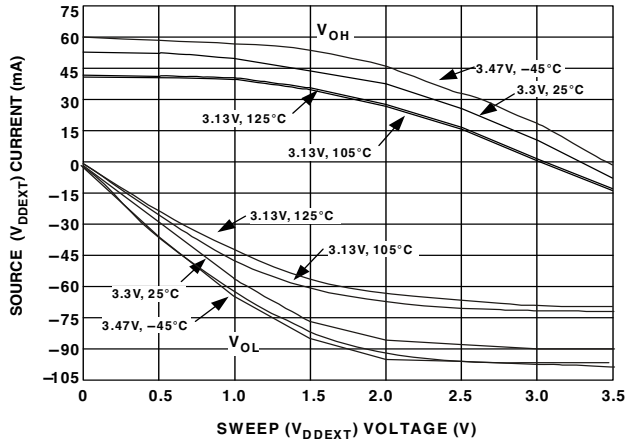


Figure 40. SDCLK1–0 Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 14 on Page 23 through Table 42 on Page 50. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 41.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 41. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

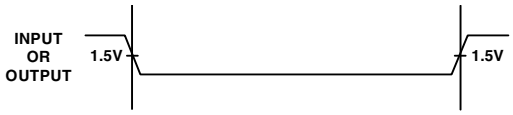
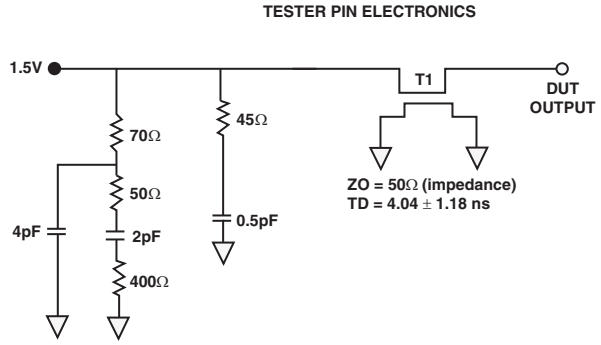


Figure 41. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 42). Figure 47 and Figure 48 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 43 through Figure 48 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 49 shows the bottom view of the BGA_ED ball configuration. Figure 50 shows the top view of the BGA_ED ball configuration.

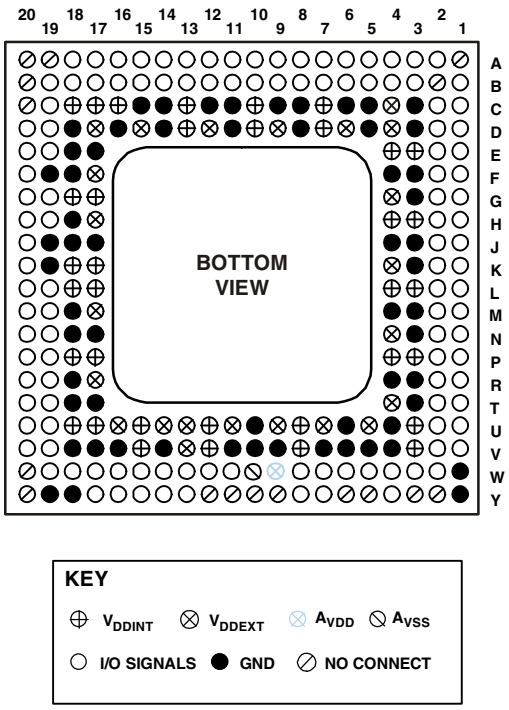


Figure 49. 256-Ball BGA_ED Ball Configuration (Bottom View)

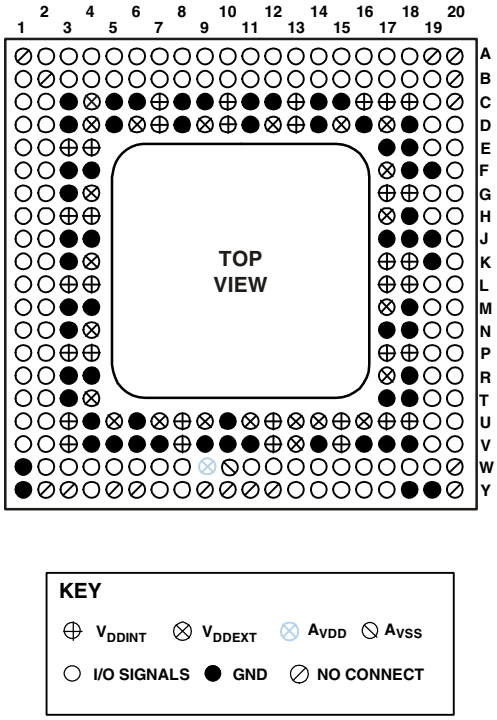


Figure 50. 256-Ball BGA_ED Ball Configuration (Top View)

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number) (Continued)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
40	DATA6	82	GND	124	FLAG0	166	GND	208	V_{DDINT}
41	V_{DDEXT}	83	CLKIN	125	DAI_P20 (SFS5)	167	V_{DDINT}		
42	GND	84	XTAL	126	GND	168	TMS		