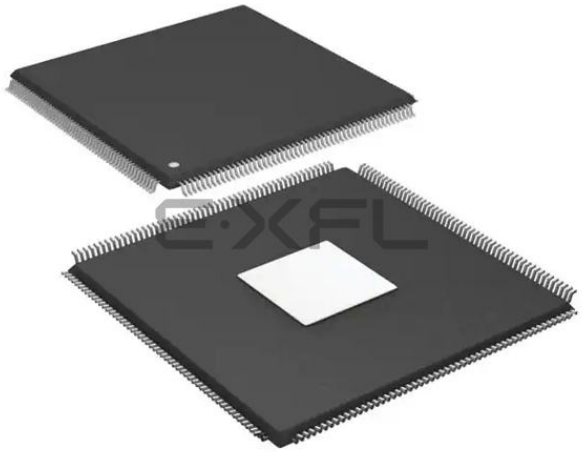

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	400MHz
Non-Volatile Memory	ROM (768kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21369kswz-6a

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and Banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit, 16-bit, or 32-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 2-phase PWM inverters.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provide the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU1), shown in Figure 1.

The SRU is amatrix routing unit (or group of multiplexers) that enable the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI include eight serial ports, an S/PDIF receiver/transmitter, four precision clock generators (PCG), eight channels of synchronous sample rate converters, and an input data port (IDP). The IDP provides an additional input path to the processor core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

For complete information on using the DAI, see the *ADSP-21368 SHARC Processor Hardware Reference*.

Serial Ports

The processors feature eight synchronous serial ports (SPORTs) that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 16 programmable and simultaneous receive or transmit pins that support up to 32 transmit or 32 receive channels of audio data when all eight SPORTs are enabled, or eight full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50 Mbps. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I^2S mode
- I^2S mode
- Packed I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example, frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Synchronous/Asynchronous Sample Rate Converter

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), two universal asynchronous receiver-transmitters (UARTs), a 2-wire interface (TWI), 12 flags, and three general-purpose timers.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21367/ADSP-21368/ADSP-21369 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for five data bits to eight data bits, one stop bit or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Where the 16-bit UART_Divisor comes from the DLH register (most significant eight bits) and DLL register (least significant eight bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

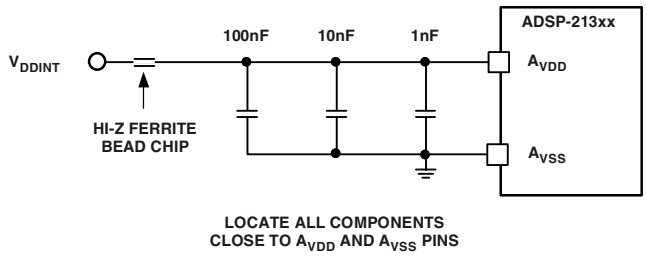


Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21367/ ADSP-21368/ADSP-21369 processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide."

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 8: A = asynchronous, G = ground, I = input, O = output, O/T = output three-state, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, (pd) = pull-down resistor, (pu) = pull-up resistor.

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors use extensive pin multiplexing to achieve a lower pin count. For complete information on the multiplexing scheme, see the *ADSP-21368 SHARC Processor Hardware Reference*, "System Design" chapter.

Table 8. Pin Descriptions

Name	Type	State During/ After Reset (ID = 00x)	Description
$ADDR_{23-0}$	O/T (pu)[1]	Pulled high/ driven low	**External Address.** The processors output addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)[1]	Pulled high/ pulled high	**External Data.** Data pins can be multiplexed to support external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default). When configured using the IDP_PDAP_CTL register, IDP Channel 0 scans the external port data pins for parallel input data.
ACK	I (pu)[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (pu)[1]	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. See the processor hardware reference for more information.
$\overline{RD}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processors read a word from external memory.
$\overline{WR}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processors write a word to external memory.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request 0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request 1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS}_2$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/Memory Select 2.**
FLAG[3]/ TMREXP/$\overline{MS}_3$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select 3.**

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	400 MHz		366 MHz 350 MHz		333 MHz 266 MHz		Unit
		Min	Max	Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.1	–0.5	+1.1	–0.5	+1.1	V
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to 70°C	0	95	0	110	0	110	°C
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+120	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ 0°C to 70°C	0	95	N/A	N/A	0	105	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+105	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: DATAx, ACK, RPBA, $\overline{BRx}$, IDx, FLAGx, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]			0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{IL}[3, 5, 6]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{IHPD}[5]	High Level Input Current Pull-Down	@ V_{DDEXT} = Max, V_{IN} = 0 V			250	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	µA
$I_{DD-INTYP}$[10]	Supply Current (Internal)	t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25°C		700		mA
		t_{CCLK} = 3.00 ns, V_{DDINT} = 1.2 V, 25°C		900		mA
		t_{CCLK} = 2.85 ns, V_{DDINT} = 1.3 V, 25°C		1050		mA
		t_{CCLK} = 2.73 ns, V_{DDINT} = 1.3 V, 25°C		1080		mA
		t_{CCLK} = 2.50 ns, V_{DDINT} = 1.3 V, 25°C		1100		mA
AI_{DD}[11]	Supply Current (Analog)	A_{VDD} = Max			11	mA
C_{IN}[12, 13]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.3 V			4.7	pF

[1] Applies to output and bidirectional pins: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, FLAGx, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDCLKx, $\overline{EMU}$, TDO.
[2] See Output Drive Currents on Page 51 for typical drive current capabilities.
[3] Applies to input pins without internal pull-ups: BOOT_CFGx, CLK_CFGx, CLKIN, $\overline{RESET}$, TCK.
[4] Applies to input pins with internal pull-ups: ACK, RPBA, TMS, TDI, $\overline{TRST}$.
[5] Applies to input pins with internal pull-downs: IDx.
[6] Applies to input pins with internal pull-ups disabled: ACK, RPBA.
[7] Applies to three-statable pins without internal pull-ups: FLAGx, SDCLKx, TDO.
[8] Applies to three-statable pins with internal pull-ups: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, $\overline{EMU}$.
[9] Applies to three-statable pins with internal pull-ups disabled: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10
[10] See the Engineer-to-Engineer Note "*Estimating Power Dissipation for ADSP-21368 SHARC Processors*" (EE-299) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Clock Signals

The processors can use an external clock or a crystal. See the CLKIN pin description in Table 8 on Page 13. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode.

Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

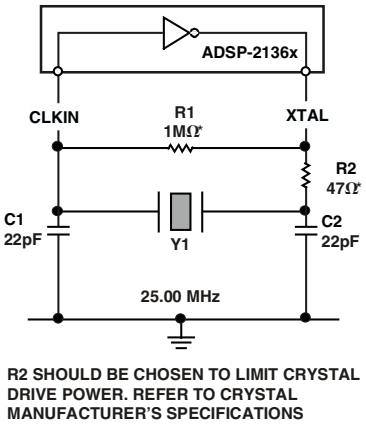


Figure 8. 400 MHz Operation (Fundamental Mode Crystal)

Reset

Table 14. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

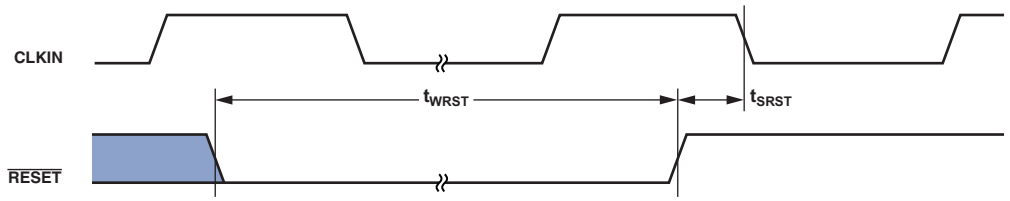


Figure 9. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

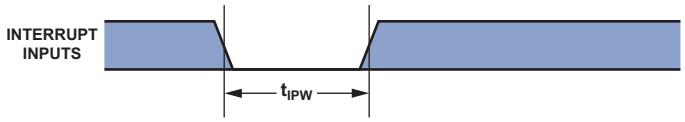


Figure 10. Interrupts

Timer WDTH_CAP Timing

The following specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specification provided in Table 18 is valid at the DPI_P14–1 pins.

Table 18. Timer Width Capture Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

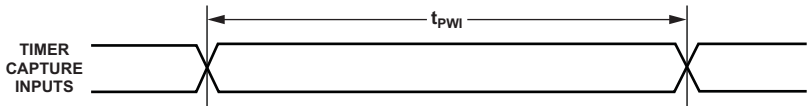


Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 19. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

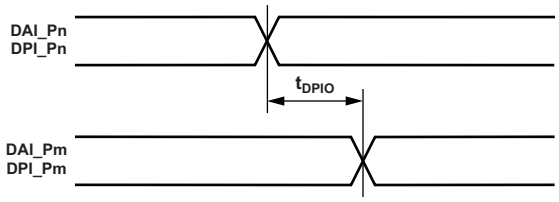


Figure 14. DAI/DPI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01–20).

Table 20. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, and PH = FSxPHASE. For more information, see the processor hardware reference, "Precision Clock Generators" chapter.

[1] In normal mode.

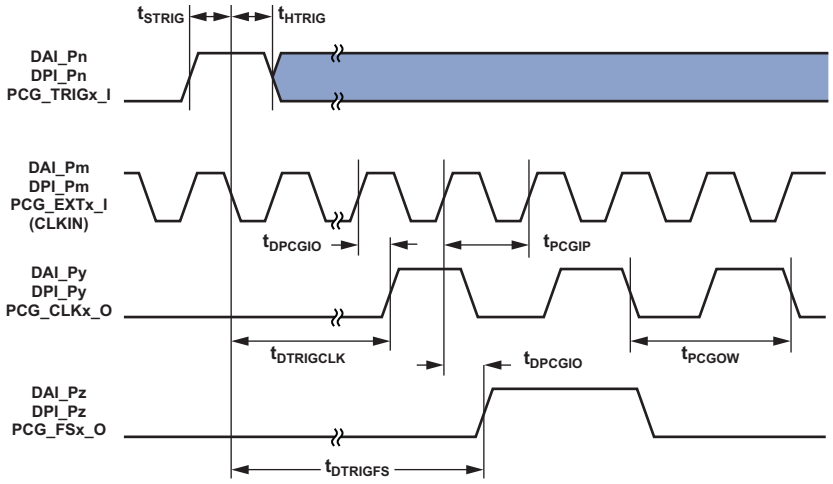


Figure 15. Precision Clock Generator (Direct Pin Routing)

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 23. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

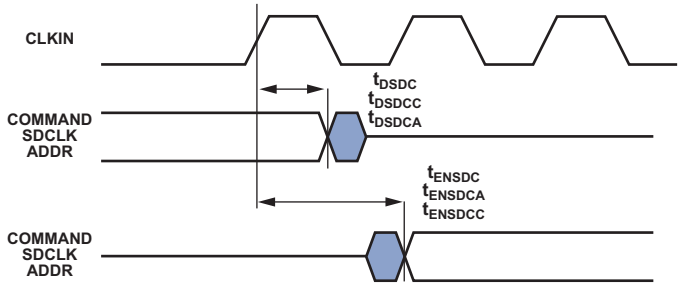


Figure 18. SDRAM Interface Enable/Disable Timing

Memory Write

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus masters, accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

Table 25. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 9.7 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 4.9	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 4.11		ns
t_{WDE}	Data Enabled to $\overline{WR}$ Low	t_{SDCLK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

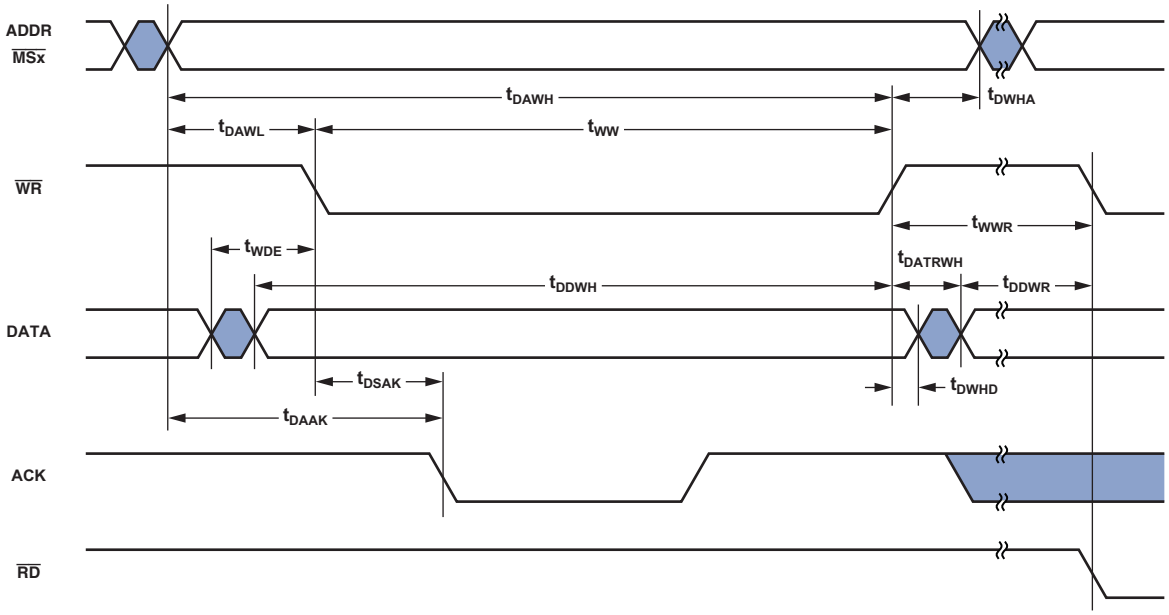


Figure 20. Memory Write

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals SCLK, frame sync (FS), data channel A, data channel B are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. Serial Ports—External Clock

Parameter		400 MHz 366 MHz 350 MHz Min	400 MHz 366 MHz 350 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements								
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		2.0		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics								
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)		10.25		10.25		10.25	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)	2		2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8		9.6		9.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Input Data Port

The timing requirements for the IDP are given in Table 32. IDP signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 32. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

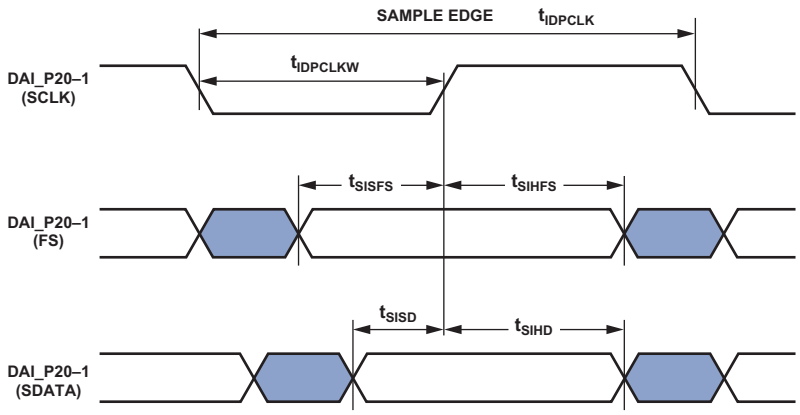


Figure 26. IDP Master Timing

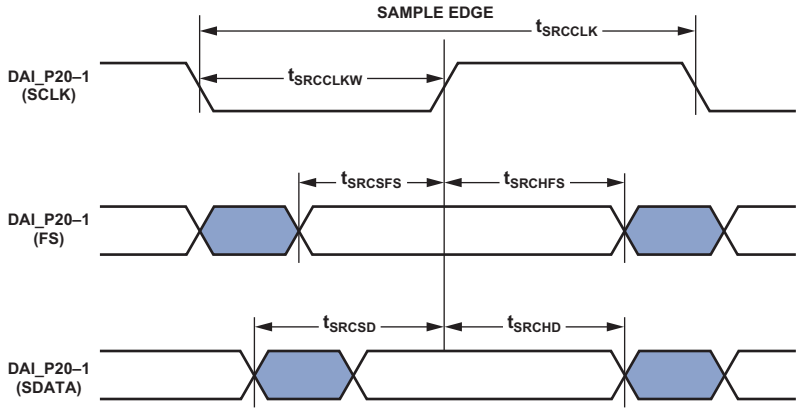


Figure 29. SRC Serial Input Port Timing

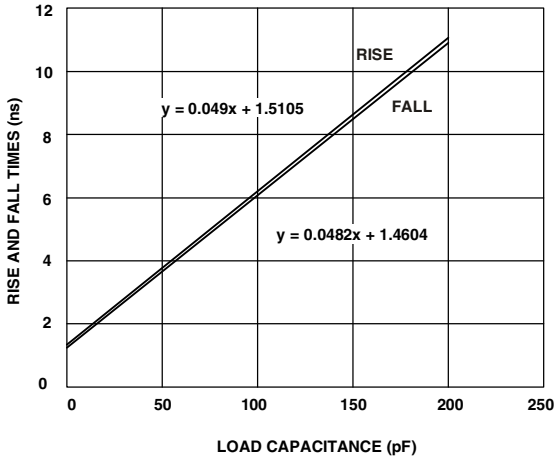


Figure 43. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

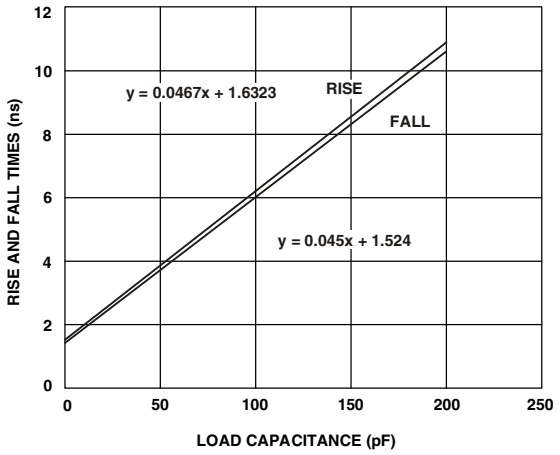


Figure 44. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

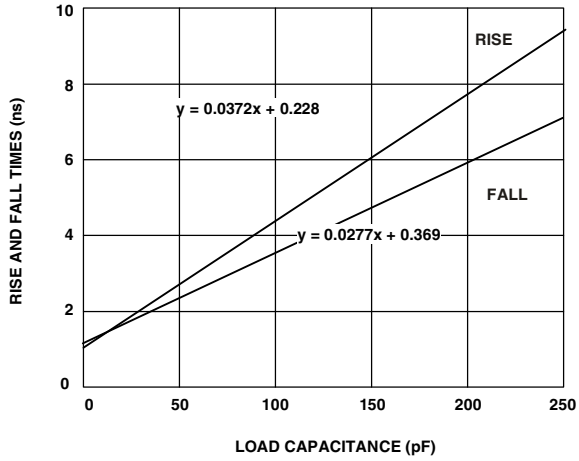


Figure 45. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

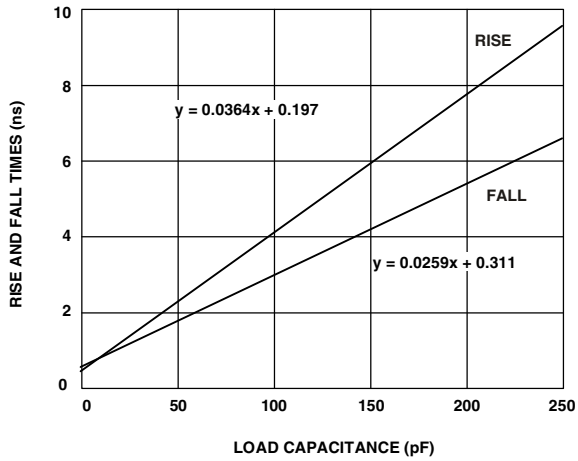


Figure 46. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

256-BALL BGA_ED PINOUT

The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 45. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI_P05 (SD1A)	C01	DAI_P09 (SD2A)	D01	DAI_P10 (SD2B)
A02	TDI	B02	SDCLK1[1]	C02	DAI_P07 (SCLK1)	D02	DAI_P06 (SD1B)
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	V_{DDEXT}	D04	V_{DDEXT}
A05	CLK_CFG1	B05	BOOT_CFG0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOT_CFG1	C06	GND	D06	V_{DDEXT}
A07	DAI_P04 (SFS0)	B07	TDO	C07	V_{DDINT}	D07	V_{DDINT}
A08	DAI_P01 (SD0A)	B08	DAI_P03 (SCLK0)	C08	GND	D08	GND
A09	DPI_P14 (TIMER1)	B09	DAI_P02 (SD0B)	C09	GND	D09	V_{DDEXT}
A10	DPI_P12 (TWI_CLK)	B10	DPI_P13 (TIMER0)	C10	V_{DDINT}	D10	V_{DDINT}
A11	DPI_P10 (UART0RX)	B11	DPI_P11 (TWI_DATA)	C11	GND	D11	GND
A12	DPI_P09 (UART0TX)	B12	DPI_P08 (SPIFLG3)	C12	GND	D12	V_{DDEXT}
A13	DPI_P07 (SPIFLG2)	B13	DPI_P05 (SPIFLG0)	C13	V_{DDINT}	D13	V_{DDINT}
A14	DPI_P06 (SPIFLG1)	B14	DPI_P04 (SPIDS)	C14	GND	D14	GND
A15	DPI_P03 (SPICLK)	B15	DPI_P01 (SPIMOSI)	C15	GND	D15	V_{DDEXT}
A16	DPI_P02 (SPIMISO)	B16	$\overline{\text{RESET}}$	C16	V_{DDINT}	D16	GND
A17	$\overline{\text{RESETOUT}}$	B17	DATA30	C17	V_{DDINT}	D17	V_{DDEXT}
A18	DATA31	B18	DATA29	C18	V_{DDINT}	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC/RPBA[2]	D20	DATA24
E01	DAI_P11 (SD3A)	F01	DAI_P14 (SFS3)	G01	DAI_P15 (SD4A)	H01	DAI_P17 (SD5A)
E02	DAI_P08 (SFS1)	F02	DAI_P12 (SD3B)	G02	DAI_P13 (SCLK3)	H02	DAI_P16 (SD4B)
E03	V_{DDINT}	F03	GND	G03	GND	H03	V_{DDINT}
E04	V_{DDINT}	F04	GND	G04	V_{DDEXT}	H04	V_{DDINT}
E17	GND	F17	V_{DDEXT}	G17	V_{DDINT}	H17	V_{DDEXT}
E18	GND	F18	GND	G18	V_{DDINT}	H18	GND
E19	DATA25	F19	GND/ID2[2]	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI_P19 (SCLK5)	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI_P18 (SD5B)	K02	DAI_P20 (SFS5)	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	V_{DDINT}	M03	GND
J04	GND	K04	V_{DDEXT}	L04	V_{DDINT}	M04	GND
J17	GND	K17	V_{DDINT}	L17	V_{DDINT}	M17	V_{DDEXT}
J18	GND	K18	V_{DDINT}	L18	V_{DDINT}	M18	GND
J19	GND/ID1[2]	K19	GND/ID0[2]	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13

208-LEAD LQFP_EP PINOUT

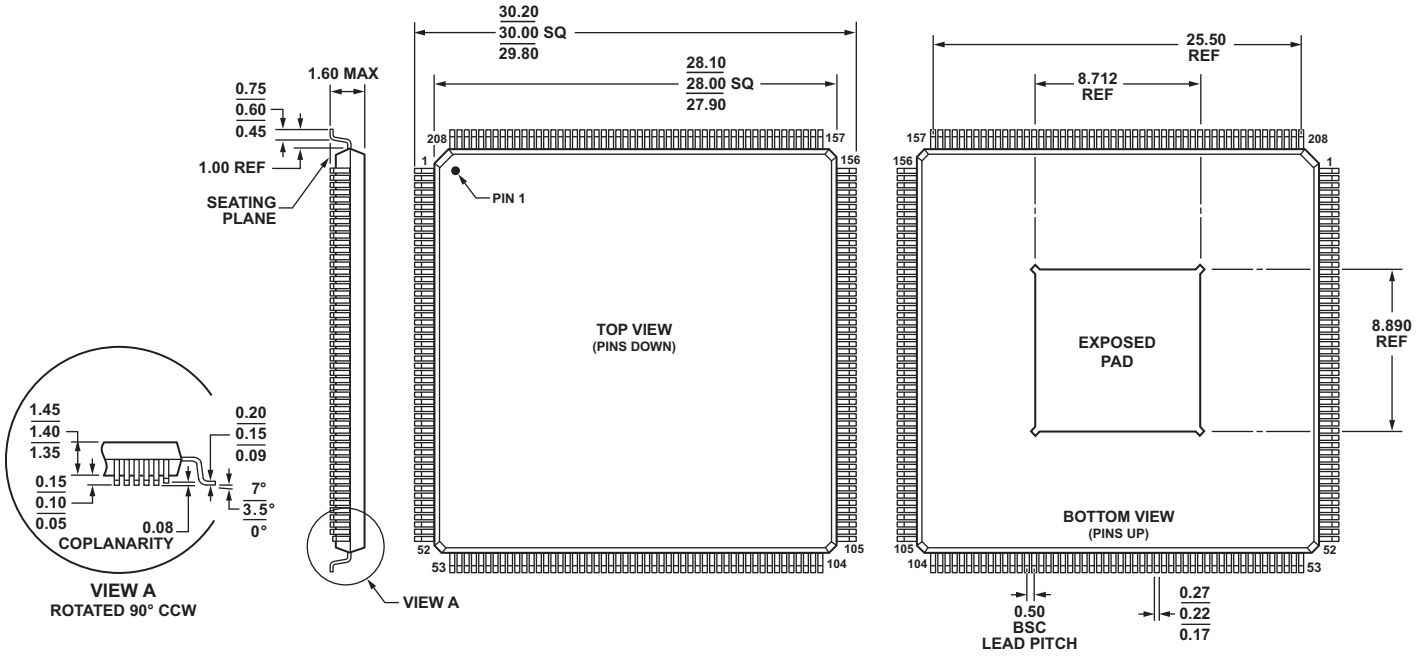
The following table shows the ADSP-2136x's pin names and their default function after reset (in parentheses).

Table 46. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDINT}	43	V_{DDINT}	85	V_{DDEXT}	127	V_{DDINT}	169	CLK_CFG0
2	DATA28	44	DATA4	86	GND	128	GND	170	BOOT_CFG0
3	DATA27	45	DATA5	87	V_{DDINT}	129	V_{DDEXT}	171	CLK_CFG1
4	GND	46	DATA2	88	ADDR14	130	DAI_P19 (SCLK5)	172	$\overline{EMU}$
5	V_{DDEXT}	47	DATA3	89	GND	131	DAI_P18 (SD5B)	173	BOOT_CFG1
6	DATA26	48	DATA0	90	V_{DDEXT}	132	DAI_P17 (SD5A)	174	TDO
7	DATA25	49	DATA1	91	ADDR15	133	DAI_P16 (SD4B)	175	DAI_P04 (SFS0)
8	DATA24	50	V_{DDEXT}	92	ADDR16	134	DAI_P15 (SD4A)	176	DAI_P02 (SD0B)
9	DATA23	51	GND	93	ADDR17	135	DAI_P14 (SFS3)	177	DAI_P03 (SCLK0)
10	GND	52	V_{DDINT}	94	ADDR18	136	DAI_P13 (SCLK3)	178	DAI_P01 (SD0A)
11	V_{DDINT}	53	V_{DDINT}	95	GND	137	DAI_P12 (SD3B)	179	V_{DDEXT}
12	DATA22	54	GND	96	V_{DDEXT}	138	V_{DDINT}	180	GND
13	DATA21	55	V_{DDEXT}	97	ADDR19	139	V_{DDEXT}	181	V_{DDINT}
14	DATA20	56	ADDR0	98	ADDR20	140	GND	182	GND
15	V_{DDEXT}	57	ADDR2	99	ADDR21	141	V_{DDINT}	183	DPI_P14 (TIMER1)
16	GND	58	ADDR1	100	ADDR23	142	GND	184	DPI_P13 (TIMER0)
17	DATA19	59	ADDR4	101	ADDR22	143	DAI_P11 (SD3A)	185	DPI_P12 (TWI_CLK)
18	DATA18	60	ADDR3	102	$\overline{MS1}$	144	DAI_P10 (SD2B)	186	DPI_P11 (TWI_DATA)
19	V_{DDINT}	61	ADDR5	103	$\overline{MS0}$	145	DAI_P08 (SFS1)	187	DPI_P10 (UART0RX)
20	GND	62	GND	104	V_{DDINT}	146	DAI_P09 (SD2A)	188	DPI_P09 (UART0TX)
21	DATA17	63	V_{DDINT}	105	V_{DDINT}	147	DAI_P06 (SD1B)	189	DPI_P08 (SPIFLG3)
22	V_{DDINT}	64	GND	106	GND	148	DAI_P07 (SCLK1)	190	DPI_P07 (SPIFLG2)
23	GND	65	V_{DDEXT}	107	V_{DDEXT}	149	DAI_P05 (SD1A)	191	V_{DDEXT}
24	V_{DDINT}	66	ADDR6	108	$\overline{SDCAS}$	150	V_{DDEXT}	192	GND
25	GND	67	ADDR7	109	$\overline{SDRAS}$	151	GND	193	V_{DDINT}
26	DATA16	68	ADDR8	110	SDCKE	152	V_{DDINT}	194	GND
27	DATA15	69	ADDR9	111	$\overline{SDWE}$	153	GND	195	DPI_P06 (SPIFLG1)
28	DATA14	70	ADDR10	112	$\overline{WR}$	154	V_{DDINT}	196	DPI_P05 (SPIFLG0)
29	DATA13	71	GND	113	SDA10	155	GND	197	DPI_P04 (SPIDS)
30	DATA12	72	V_{DDINT}	114	GND	156	V_{DDINT}	198	DPI_P03 (SPICLK)
31	V_{DDEXT}	73	GND	115	V_{DDEXT}	157	V_{DDINT}	199	DPI_P01 (SPIMOSI)
32	GND	74	V_{DDEXT}	116	SDCLK0	158	V_{DDINT}	200	DPI_P02 (SPIMISO)
33	V_{DDINT}	75	ADDR11	117	GND	159	GND	201	$\overline{RESETOUT}$
34	GND	76	ADDR12	118	V_{DDINT}	160	V_{DDINT}	202	$\overline{RESET}$
35	DATA11	77	ADDR13	119	$\overline{RD}$	161	V_{DDINT}	203	V_{DDEXT}
36	DATA10	78	GND	120	ACK	162	V_{DDINT}	204	GND
37	DATA9	79	V_{DDINT}	121	FLAG3	163	TDI	205	DATA30
38	DATA8	80	A_{VSS}	122	FLAG2	164	$\overline{TRST}$	206	DATA31
39	DATA7	81	A_{VDD}	123	FLAG1	165	TCK	207	DATA29

PACKAGE DIMENSIONS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are available in 256-ball RoHS compliant and leaded BGA_ED, and 208-lead RoHS compliant LQFP_EP packages.



COMPLIANT TO JEDEC STANDARDS MS-026-BJB-HD

NOTE:
THE EXPOSED PAD IS REQUIRED TO BE ELECTRICALLY AND THERMALLY CONNECTED TO VSS. THIS SHOULD BE IMPLEMENTED BY SOLDERING THE EXPOSED PAD TO A VSS PCB LAND THAT IS THE SAME SIZE AS THE EXPOSED PAD. THE VSS PCB LAND SHOULD BE ROBUSTLY CONNECTED TO THE VSS PLANE IN THE PCB WITH AN ARRAY OF THERMAL VIAS FOR BEST PERFORMANCE.

Figure 51. 208-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-208-1)
Dimensions shown in millimeters