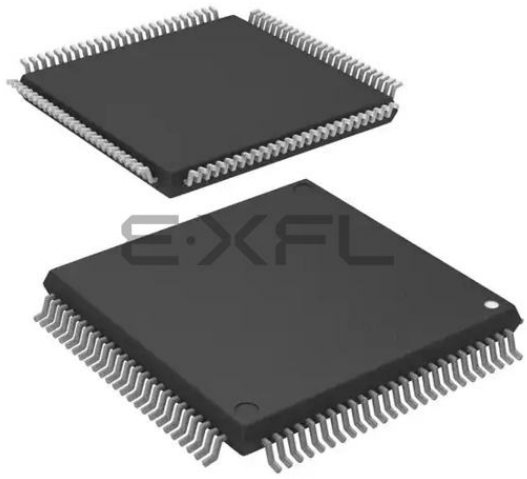

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Core Size	16-Bit
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Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f36camdfb-30

6.4 Operations

6.4.1 Status after Reset

The status of SFRs after reset depends on the reset type. See the Reset Value column in 4. “Special Function Registers (SFRs)”. Table 6.7 lists Pin Status When $\overline{\text{RESET}}$ Pin Level is Low, Figure 6.2 shows CPU Register Status after Reset, and Figure 6.3 shows Reset Sequence.

Table 6.7 Pin Status When $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Status (1)	
	Single-chip mode (CNVSS = VSS)	Boot mode (CNVSS = VCC1, P5_5 = low)
P0	Input port	Input port
P1	Input port	Input port
P2, P3, P4_0 to P4_3	Input port	Input port
P4_4	Input port	Input port
P4_5 to P4_7	Input port	Input port
P5_0	Input port	$\overline{\text{CE}}$ input (2)
P5_1	Input port	Input port
P5_2	Input port	Input port
P5_3	Input port	Input port
P5_4	Input port	Input port
P5_5	Input port	$\overline{\text{EPM}}$ input (3)
P5_6	Input port	Input port
P5_7	Input port	Input port
P6 to P10	Input port	Input port

Notes:
1. The pin status shown here is when the internal power supply voltage has stabilized after power-on. The pin status is undefined until td(P-R) has elapsed after power-on.
2. Input a high-level signal.
3. Input a low-level signal.

Table 9.4 Selecting Clock Division Related Bits (1)

Division	CM1 Register	CM0 Register
	Bits CM17 to CM16	CM06 bit
No division (2)	00b	0
Divide-by-2	01b	0
Divide-by-4	10b	0
Divide-by-8	–	1
Divide-by-16	11b	0

–: Any value from 00b to 11b

Notes:
1. While in high-speed mode, medium-speed mode, PLL operating mode, 125 kHz on-chip oscillator mode, or 125 kHz on-chip oscillator low power mode.
2. Select divide-by-1 (no division) in high-speed mode.

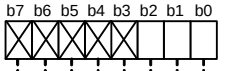
Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits

Division	CPU Clock Frequency	CM1 Register	CM0 Register
		Bits CM17 and CM16	CM06 bit
Divide-by-2	Approx. 20 MHz	00b (no division)	0
Divide-by-4	Approx. 10 MHz	01b (divide-by-2)	0
Divide-by-8	Approx. 5 MHz	10b (divide-by-4)	0
Divide-by-16	Approx. 2.5 MHz	-	1 (divide-by-8)
Divide-by-32	Approx. 1.25 MHz	11b (divide-by-16)	0

–: Any value from 00b to 11b

13.3.7 $\overline{NMI}/\overline{SD}$ Digital Filter Register (NMIDF)

$\overline{NMI}/\overline{SD}$ Digital Filter Register



Symbol	Address	Reset Value
NMIDF	0369h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
NMIDF0	$\overline{NMI}/\overline{SD}$ filter sampling clock select bit	b2 b1 b0 0 0 0 : No filter 0 0 1 : CPU clock divided by 2 0 1 0 : CPU clock divided by 4 0 1 1 : CPU clock divided by 8 1 0 0 : CPU clock divided by 16 1 0 1 : CPU clock divided by 32 1 1 0 : CPU clock divided by 64 1 1 1 : CPU clock divided by 128	RW
NMIDF1			RW
NMIDF2			RW
— (b7-b3)	No register bits. If necessary, set to 0. The read value is undefined.		—

Change the NMIDF register under the following conditions:

- The PM24 bit in the PM2 register is 0 ($\overline{NMI}$ interrupt disabled)
- Bits INV02 and INV03 in the INVC0 register are 0 (three-phase motor control timer function not used, three-phase motor control timer output disabled).

Once the PM24 bit is set to 1 ($\overline{NMI}$ interrupt enabled), it cannot be set to 0 by a program. Change the NMIDF register before setting the PM24 bit to 1.

16.4 Interrupts

Refer to operation examples for interrupt request generation timing.
For details on interrupt control, refer to 14.7 “Interrupt Control”.

Table 16.11 DMAC Interrupt Related Registers

Address	Register	Symbol	Reset Value
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested) (i = 0 to 3). Therefore, set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed. Refer to 14.13 “Notes on Interrupts” for more details.

17.5.6 Timer A (Programmable Output Mode)

17.5.6.1 Changing the Operating Mode

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

17.5.6.2 Stop While Counting

When setting the TAiS bit to 0 (count stopped) during pulse output, the following occur:
When the POFSi bit in the TAPOFS register is 0:

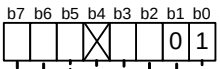
- Counting stops.
- When the TAiOUT pin is high, the output level goes low.
- When the TAiOUT pin is low, the output level remains unchanged.
- The IR bit remains unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Counting stops
- When the TAiOUT pin output is low, the output level goes high.
- When the TAiOUT pin output is high, the output level remains unchanged.
- The IR bit remains unchanged.

Event Counter Mode

Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	Reset Value
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Count polarity select bit	b3 b2 0 0 : Counts falling edges of an external signal 0 1 : Counts rising edges of an external signal 1 0 : Counts falling and rising edges of an external signal 1 1 : Do not set	RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—
MR3	Write 0 in event counter mode. The read value is undefined in event counter mode		RO
TCK0	Disabled in event counter mode. Set 0 or 1.		RW
TCK1	Event clock select bit	0 : Input from TBiIN pin 1 : Timer Bj (j = i - 1; however, j = 2 if i = 0, j = 5 if i = 3)	RW

MR1 and MR0 (Count polarity select bit) (b3-b2)

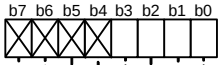
These bits are enabled when the TCK1 bit is 0 (input from TBiIN pin). When the TCK1 bit is 1 (timer Bj), these bits can be set to 0 or 1.

TCK1 (Event clock select bit) (b7)

When the TCK1 bit is 1, an event occurs when an interrupt request of timer Bj (j = i - 1; however, j = 2 if i = 0, j = 5 if i = 3) is generated. An event occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers

19.2.9 Position-Data-Retain Function Control Register (PDRF)

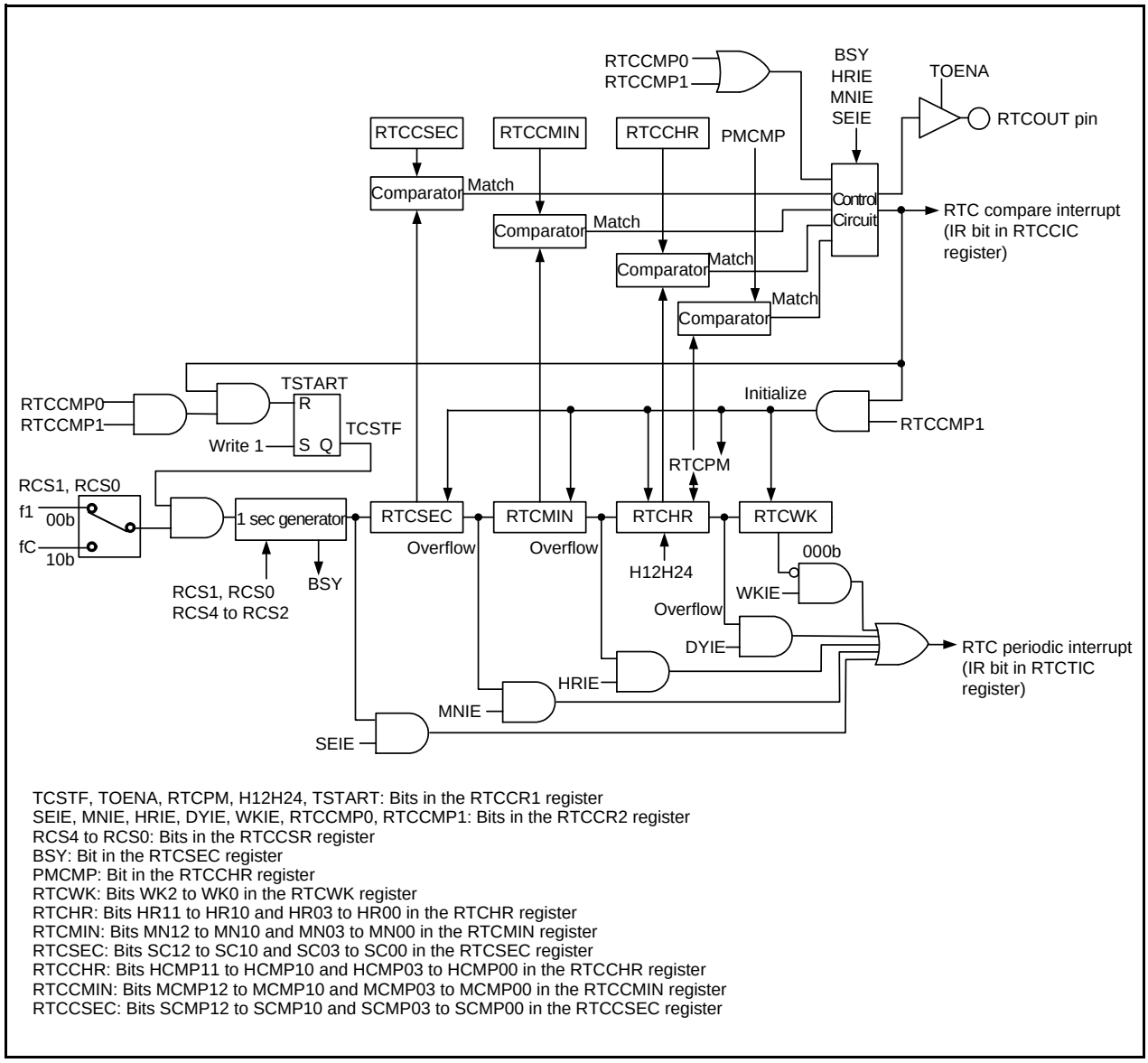
Position-Data-Retain Function Control Register



Symbol	Address	Reset Value
PDRF	030Eh	XXXX 0000b

Bit Symbol	Bit Name	Function	RW
PDRW	W-phase position data retain bit	Input level at IDW pin is retained. 0: Low level 1: High level	RO
PDRV	V-phase position data retain bit	Input level at IDV pin is retained. 0: Low level 1: High level	RO
PDRU	U-phase position data retain bit	Input level at IDU pin is retained. 0: Low level 1: High level	RO
PDRT	Retain-trigger polarity select bit	Select polarity of a retain-trigger When the INV14 bit is 0 (active low): 0: Falling edge of high-side output signal 1: Rising edge of high-side output signal When the INV14 bit is 1 (active high): 0: Rising edge of high-side output signal 1. Falling edge of high-side output signal	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read value is undefined.		—

This register is only enabled in three-phase mode.

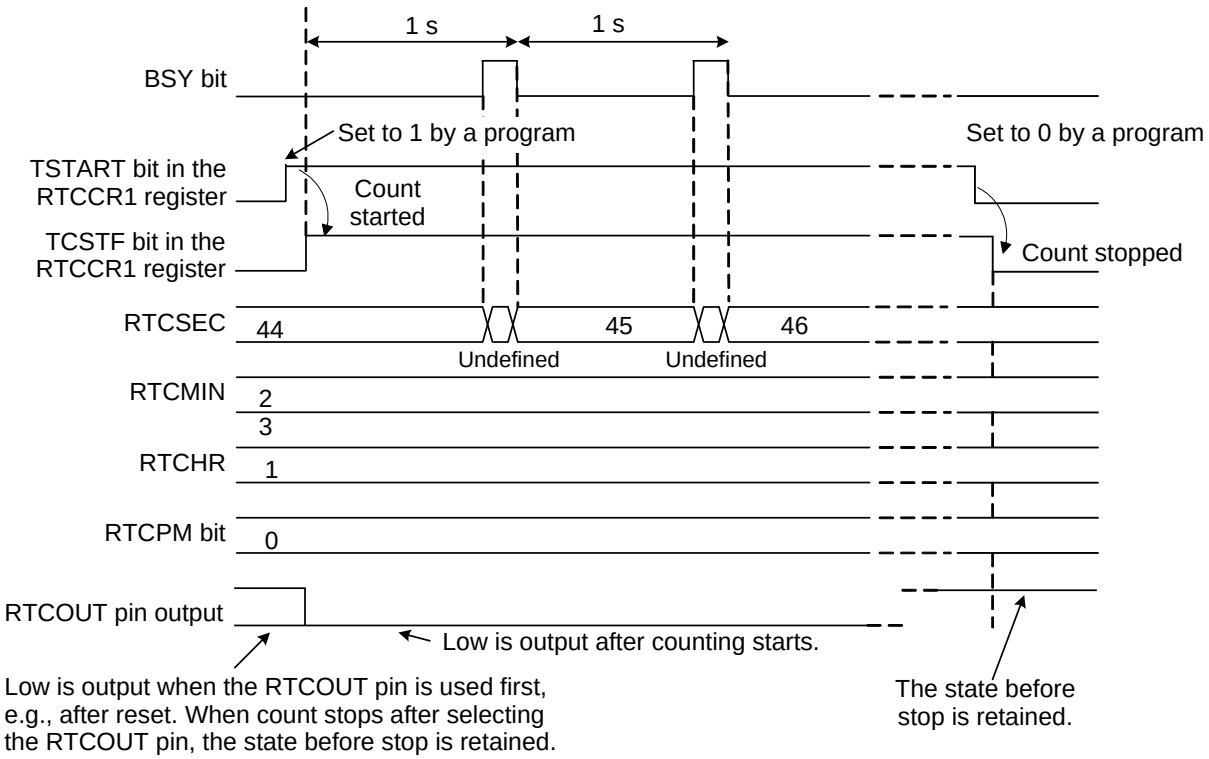


TCSTF, TOENA, RTCPM, H12H24, TSTART: Bits in the RTCCR1 register
SEIE, MNIE, HRIE, DYIE, WKIE, RTCCMP0, RTCCMP1: Bits in the RTCCR2 register
RCS4 to RCS0: Bits in the RTCCSR register
BSY: Bit in the RTCSEC register
PMCMP: Bit in the RTCCHR register
RTCWK: Bits WK2 to WK0 in the RTCWK register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
RTCCHR: Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register
RTCCMIN: Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register
RTCCSEC: Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register

Figure 21.1 Real-Time Clock Block Diagram

Table 21.2 I/O Port

Pin Name	I/O	Function
RTCOUT	Output	Compare output



The above assumes the following:
- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b (compare mode 1).

BSY bit: Bit in RTCSEC register
RTCSEC: Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN: Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR: Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit: Bit in RTCCR1 register

Figure 21.7 Count Start/Stop Operating Example

NCH (Data output select bit) (b5)

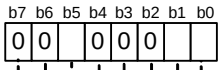
TXD2/SDA2 and SCL2 are N-channel open drain outputs. They cannot be set as CMOS outputs. Nothing is assigned to the NCH bit in the U2C0 register. If necessary, set this bit to 0.
This function is used to set the P-channel transistor of the CMOS output buffer always off, but not to change pins TXDi/SDAi and SCLi to open drain output completely.
Refer to the electrical characteristics for the input voltage range.

UFORM (Bit order select bit) (b7)

The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit character data).
Set the UFORM bit to 1 when bits SMD2 to SMD0 are 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are 100b (UART mode, 7-bit character data) or 110b (UART mode, 9-bit character data).

23.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register



Symbol	Address	Reset Value
PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B and S clock select bit (clock source for timers A, B and S, the dead time timer, and multi-master I2C-bus interface)	0: f2TIMAB/f2IIC/f2TIMS 1: f1TIMAB/f1IIC/f1TIMS	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART5)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Write to the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

23.3.6 Arbitration Lost

When all of the conditions below are met, the SDAMM pin signal level becomes low by an external device and the I2C interface determines that it has lost arbitration.

(a) Transmit/receive (one of the following)
- Slave address transmit (not an ACK clock) in master transmit mode or master receive mode
- Data transmit (not an ACK clock) in master transmit mode
- Start condition generated in master transmit mode or master receive mode
- Stop condition generated in master transmit mode or master receive mode

(b) Internal SDA output: High

(c) SDAMM pin level: Low (sampling at the rising edge of the clock of SCLMM pin.)

Figure 23.12 shows Operation Example When Arbitration Lost is Detected.

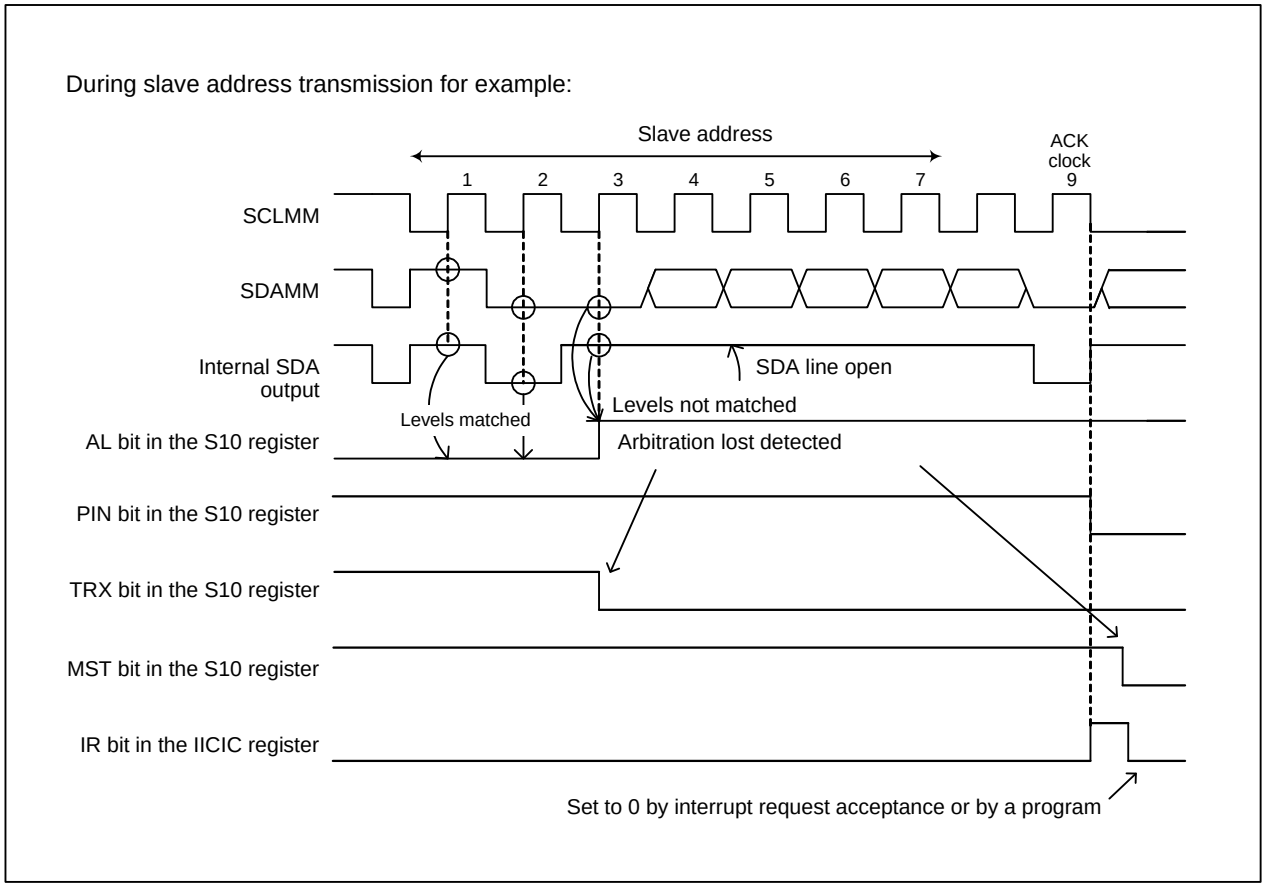


Figure 23.12 Operation Example When Arbitration Lost is Detected

EP6TS (Endpoint 6 transmit complete flag) (b4)

When the EP6TS bit becomes 1, an interrupt request is generated.
Condition to become 0:

- Write 0 to the EP6TS bit.

Condition to become 1:

- Transmit data from endpoint 6 to the host and receive an ACK.

(Writing 1 has no effect.)

EP6TR (Endpoint 6 transfer request flag) (b5)

When the EP6TR bit becomes 1, an interrupt request is generated.
Condition to become 0:

- Write 0 to the EP6TR bit.

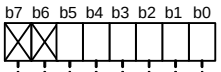
Condition to become 1:

- No valid data is detected in the endpoint 6 transmit FIFO buffer when an IN token for endpoint 6 is received.

(Writing 1 has no effect.)

24.2.12 USB Interrupt Select Register 3 (USBISR3)

USB Interrupt Select Register 3 (USBISR3)



Symbol	Address	Reset Value
USBISR3	D113h	XX00 0000b

Bit Symbol	Bit Name	Function	RW
EP4FULLS	Endpoint 4 FIFO full status interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
EP5ALLEMPS	Endpoint 5 FIFO all empty interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
EP5EMPTYS	Endpoint 5 FIFO empty interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
EP5TRS	Endpoint 5 transfer request interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
EP6TSS	Endpoint 6 transmit complete interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
EP6TRS	Endpoint 6 transfer request interrupt select bit	0: USB interrupt 0 1: USB interrupt 1	RW
— (b7-b6)	No register bits. Should be written with 0 and read as undefined value.		—

Access the USBISR3 register in 8-bit units. Do not access this register in 16-bit units.

Condition to become 0:

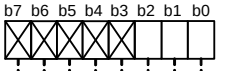
- Transmit all data in the endpoint i (i = 0, 2, 3, 5, 6) transmit FIFO buffer.

Condition to become 1:

- Set data to the endpoint i transmit FIFO buffer and write 1 (transmit data determined) to the EPiIPKTE bit in the USBTRGj register.

24.2.22 USB Trigger Register 0 (USBTRG0)

USB Trigger Register 0 (USBTRG0)



Symbol	Address	Reset Value
USBTRG0	D190h	XXh

Bit Symbol	Bit Name	Function	RW
EP0IPKTE	Endpoint 0 IN packet enable trigger bit	When this bit is set to 1, the endpoint 0 IN transmit data is determined.	WO
EP0ORDFN	Endpoint 0 OUT read complete trigger bit	When this bit is set to 1, the endpoint 0 OUT receive FIFO buffer is initialized and the next packet can be received.	WO
EP0SRDFN	Endpoint 0 S read complete trigger bit	When reading the setup command from the endpoint 0 S receive FIFO buffer, and setting this bit to 1, the host advances to the data stage and the data becomes transmittable/receivable.	WO
— (b7-b3)	No register bits. Should be written with 0 and read as undefined value.		—

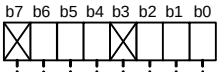
Access the USBTRG0 register in 8-bit units. Use the MOV instruction to access this register.

EP0SRDFN (Endpoint 0 S read complete trigger bit) (b2)

After the setup command is read from the endpoint 0 S reception FIFO buffer, set the EP0SRDFN bit to 1. If the USB module receives the data-stage transmit/receive request before the EP0SRDFN bit is set to 1, a NACK is returned. Values in registers USBEPDR0I and USBEPDR0O can be transmitted/ received when setting this bit to 1 after the setup command is received. The endpoint 0 S reception FIFO buffer can receive data regardless of the EP0SRDFN bit value.

24.2.28 USB Stall Status Register j (USBSTLSRj) (j = 1, 2)

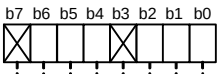
USB Stall Status Register 1 (USBSTLSR1)



Symbol	Address	Reset Value
USBSTLSR1	D1A9h	X000 X000b

Bit Symbol	Bit Name	Function	RW
EP1STLST	Endpoint 1 internal stall status flag	0: Other than STALL state 1: STALL state	RO
EP2STLST	Endpoint 2 internal stall status flag	0: Other than STALL state 1: STALL state	RO
EP3STLST	Endpoint 3 internal stall status flag	0: Other than STALL state 1: STALL state	RO
— (b3)	No register bit. Should be written with 0 and read as undefined value.		—
EP1ASCE	Endpoint 1 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
EP2ASCE	Endpoint 2 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
EP3ASCE	Endpoint 3 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
— (b7)	No register bit. Should be written with 0 and read as undefined value.		—

USB Stall Status Register 2 (USBSTLSR2)



Symbol	Address	Reset Value
USBSTLSR2	D1AAh	X000 X000b

Bit Symbol	Bit Name	Function	RW
EP4STLST	Endpoint 4 internal stall status flag	0: Other than STALL state 1: STALL state	RO
EP5STLST	Endpoint 5 internal stall status flag	0: Other than STALL state 1: STALL state	RO
EP6STLST	Endpoint 6 internal stall status flag	0: Other than STALL state 1: STALL state	RO
— (b3)	No register bit. Should be written with 0 and read as undefined value.		—
EP4ASCE	Endpoint 4 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
EP5ASCE	Endpoint 5 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
EP6ASCE	Endpoint 6 automatic stall clear enable bit	0: Auto-clear disabled 1: Auto-clear enabled	RW
— (b7)	No register bit. Should be written with 0 and read as undefined value.		—

28.9.4 Standard Serial I/O Mode 1

In standard serial I/O mode 1, a serial programmer is connected to the MCU using clock synchronous serial I/O.

Table 28.21 Pin Functions (Flash Memory Standard Serial I/O Mode 1)

Pin	Name	I/O	Power Supply	Description
VCC1, VCC2, VSS	Power input		-	Apply the flash memory program and erase voltage to the VCC1 pin, and VCC2 to the VCC2 pin. The VCC application condition is that VCC2 ≤ VCC1. Apply 0 V to the VSS pin.
CNVSS	CNVSS	I	VCC1	Connect to the VCC1 pin.
$\overline{\text{RESET}}$	Reset input	I	VCC1	Reset input pin.
XIN	Clock input	I	VCC1	Input a high-level signal to the XIN pin and open the XOUT pin when the main clock is not used. Connect a ceramic resonator or crystal between pins XIN and XOUT when the main clock is used. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	O		
UVCC	USB power supply input	I/O		Power supply pin for ATTACH, D+ and D-.
AVCC, AVSS	Analog power supply input			Connect the AVCC pin to VCC1 and the AVSS pin to VSS, respectively.
VREF	Reference voltage input	I		Reference voltage input pin for A/D converter. When using standard serial I/O mode 1, and power supply to VREF is not supplied, connect with VSS.
P0_0 to P0_7	Input port P0	I	VCC2	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	I	VCC2	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	I	VCC2	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	I	VCC2	Input a high- or low-level signal or leave open.
P4_0 to P4_7	Input port P4	I	VCC2	Input a high- or low-level signal or leave open.
P5_1 to P5_4, P5_6, P5_7	Input port P5	I	VCC2	Input a high- or low-level signal or leave open.
P5_0	$\overline{\text{CE}}$ input	I	VCC2	Input a high-level signal.
P5_5	$\overline{\text{EPM}}$ input	I	VCC2	Input a low-level signal.
P6_0 to P6_3	Input port P6	I	VCC1	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	O	VCC1	BUSY signal output pin
P6_5/CLK1	SCLK input	I	VCC1	Serial clock input pin
P6_6 / RXD1	RXD input	I	VCC1	Serial data input pin.
P6_7 / TXD1	TXD output	O	VCC1	Serial data output pin.
P7_0 to P7_7	Input port P7	I	VCC1	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	I	VCC1	Input a high- or low-level signal or leave open.
P9_0 to P9_7	Input port P9	I	VCC1	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	I	VCC1	Input a high- or low-level signal or leave open.

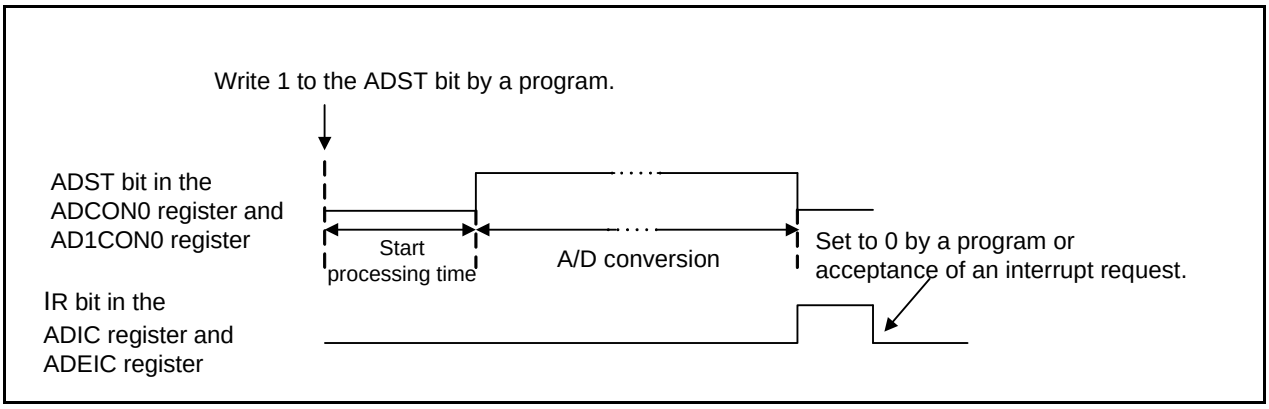


Figure 30.14 ADST Bit Operation

30.20.12 ϕAD

Divide fAD so ϕAD conforms to the standard frequency.
In particular, consider the maximum and minimum values of fOCO40M when the CKS3 bit in the ADCON2 register is 1 (fOCO40M is fAD).

N

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