Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	66MHz
Non-Volatile Memory	External
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2188mbstz-266

ADSP-2188M* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- EZ-ICE® Serial Emulator for ADSP-218x Processor Family

DOCUMENTATION

Application Notes

- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-334: Digital Signal Processing Techniques
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
- EE-131: Booting the ADSP-2191/95/96 DSPs
- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs
- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board

- EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
- EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0++
- EE-153: ADSP-2191 Programmable PLL
- EE-154: ADSP-2191 Host Port Interface
- EE-156: Support for the H.100 protocol on the ADSP-2191
- EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-164: Advanced EPROM Boot and No-boot Scenarios with ADSP-219x DSPs
- EE-168: Using Third Overtone Crystals with the ADSP-218x DSP
- EE-17: ADSP-2187L Memory Organization
- EE-18: Choosing and Using FFTs for ADSP-21xx
- EE-188: Using C To Implement Interrupt-Driven Systems On ADSP-219x DSPs
- EE-2: Using ADSP-218x I/O Space
- EE-226: ADSP-2191 DSP Host Port Booting
- EE-227: CAN Configuration Procedure for ADSP-21992 DSPs
- EE-249: Implementing Software Overlays on ADSP-218x DSPs with VisualDSP++®
- EE-32: Language Extensions: Memory Storage Types, ASM & Inline Constructs
- EE-33: Programming The ADSP-21xx Timer In C
- EE-35: Troubleshooting your ADSP-218x EZ-ICE
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-36: ADSP-21xx Interface to the IOM-2 bus
- EE-38: ADSP-2181 IDMA Port - Cycle Steal Timing
- EE-39: Interfacing 5V Flash Memory to an ADSP-218x (Byte Programming Algorithm)
- EE-48: Converting Legacy 21xx Systems To A 218x System Design
- EE-5: ADSP-218x Full Memory Mode vs. Host Memory Mode
- EE-60: Simulating an RS-232 UART Using the Synchronous Serial Ports on the ADSP-21xx Family DSPs
- EE-64: Setting Mode Pins on Reset
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-71: Minimum Rise Time Specs for Critical Interrupt and Clock Signals on the ADSP-21x1/21x5
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-78: BDMA Usage on 100 pin ADSP-218x DSPs Configured for IDMA Use
- EE-79: EPROM Booting In Host Mode with 100 Pin 218x Processors
- EE-82: Using an ADSP-2181 DSP's IO Space to IDMA Boot Another ADSP-2181
- EE-89: Implementing A Software UART on the ADSP-2181 EZ-Kit-Lite
- EE-90: Using the 21xx C-FFT Library
- EE-96: Interfacing Two AD73311 Codecs to the ADSP-218x

Data Sheet

- ADSP-2188M: 16-bit, 75 MIPS, 2.75v, 2 serial ports, host port, 256 KB RAM Data Sheet

Evaluation Kit Manuals

- ADSP-218x DSP family and ADSP-2192 EZ-KIT Lite® Installation Procedure -Non-USB

Processor Manuals

- ADSP 21xx Processors: Manuals
- ADSP-218x DSP Hardware Reference
- ADSP-218x DSP Instruction Set Reference
- Using the ADSP-2100 Family Volume 1
- Using the ADSP-2100 Family Volume 2

Software Manuals

- VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
- VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
- VisualDSP++ 3.5 C/C++ Compiler and Library Manual for ADSP-219x Processors
- VisualDSP++ 3.5 Component Software Engineering User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Getting Started Guide for 16-Bit Processors
- VisualDSP++ 3.5 Kernel VDK User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
- VisualDSP++ 3.5 Loader Manual for 16-Bit Processors
- VisualDSP++ 3.5 User's Guide for 16-Bit Processors

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

GENERAL DESCRIPTION

The ADSP-2188M is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications.

The ADSP-2188M combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2188M integrates 256K bytes of on-chip memory configured as 48K words (24-bit) of program RAM, and 56K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-2188M is available in a 100-lead LQFP package and 144 Ball Mini-BGA.

In addition, the ADSP-2188M supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (× squared), biased rounding, result-free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility.

Fabricated in a high-speed, low-power, CMOS process, the ADSP-2188M operates with a 13.3 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2188M's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-2188M can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2188M. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

The EZ-KIT Lite is a hardware/software kit offering a complete evaluation environment for the ADSP-218x family: an ADSP-2189M-based evaluation board with PC monitor software plus assembler, linker, simulator, and PROM splitter software. The ADSP-2189M EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demo Programs
- Evaluation Suite of VisualDSP

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-2188M system. The ADSP-2188M integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2188M device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See *Designing An EZ-ICE-Compatible Target System* in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections) as well as the Designing an EZ-ICE-Compatible System section of this data sheet for the exact specifications of the EZ-ICE target board connector.

Additional Information

This data sheet provides a general overview of ADSP-2188M functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the development tools, refer to the ADSP-2100 Family Development Tools data sheet.

EZ-ICE is a registered trademark of Analog Devices, Inc.

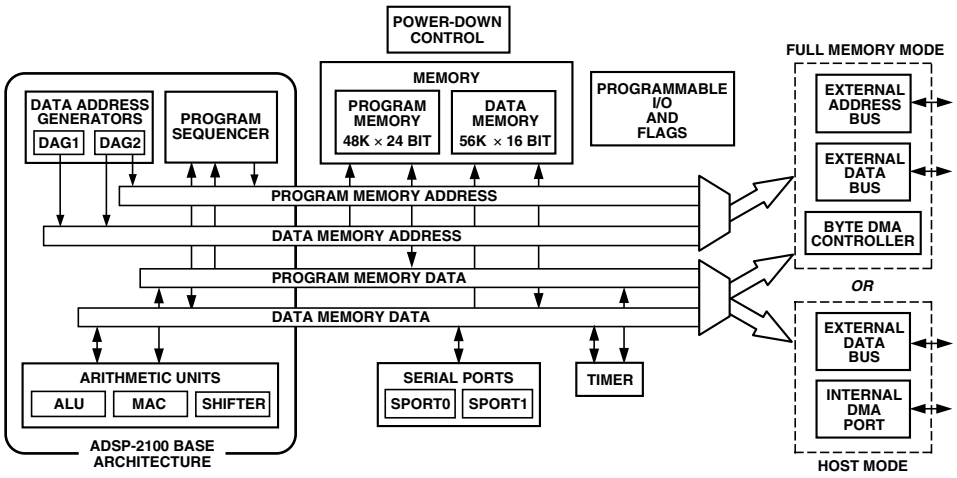


Figure 1. Functional Block Diagram

ARCHITECTURE OVERVIEW

The ADSP-2188M instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2188M assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2188M. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2188M executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2188M to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2188M can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, the ADSP-2188M may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of

Common-Mode Pins

Pin Name	# of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$ *PF7*	1	I I/O	Edge- or Level-Sensitive Interrupt Request[1] Programmable I/O Pin
$\overline{\text{IRQL1}}$ *PF6*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQL0}}$ *PF5*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQE}}$ *PF4*	1	I I/O	Edge-Sensitive Interrupt Requests[1] Programmable I/O Pin
Mode D *PF3*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode C *PF2*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode B *PF1*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode A *PF0*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1 IRQ1:0, FI, FO	5	I/O	Serial Port I/O Pins Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (2.75 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (2.75 V or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (2.75 V) Power (Mini-BGA)
V_{DDEXT}	7	I	External V_{DD} (2.75 V or 3.3 V) Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

NOTES
[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

RESET

The RESET signal initiates a master reset of the ADSP-2188M. The RESET signal must be asserted during the power-up sequence to assure proper initialization. RESET during initial power-up must be held long enough to allow the internal clock to stabilize. If RESET is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the RESET signal should be held low. On any subsequent resets, the RESET signal must meet the minimum pulsewidth specification, t_{RSP}.

The RESET input contains some hysteresis; however, if an RC circuit is used to generate the RESET signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When RESET is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Power Supplies

The ADSP-2188M has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.75 V requirement. The external supply can be connected to either a 2.75 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.75 V and 3.3 V components.

MODES OF OPERATION

Setting Memory Mode

Memory Mode selection for the ADSP-2188M is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's RESET signal such that it only drives the PF2 pin when RESET is active (low). When RESET is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

Table II. Modes of Operation

MODE D	MODE C	MODE B	MODE A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. IACK has active pull-down. (REQUIRES ADDITIONAL HARDWARE).
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; IACK requires external pull down. (REQUIRES ADDITIONAL HARDWARE)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK requires external pull-down.[1]

NOTE

[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

I/O Space (Full Memory Mode)
The ADSP-2188M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

Table V. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)
The ADSP-2188M has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)
The ADSP-2188M's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2188M supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)
The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

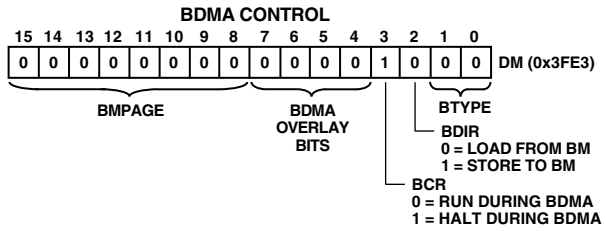


Figure 9. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table VI shows the data formats supported by the BDMA circuit.

Table VI. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ- ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, AND CM
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ- ICE may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst-case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2188M ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ- ICE board's DSP.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DDINT}	2.61	2.89	2.25	2.75	V
V_{DDEXT}	2.61	3.6	2.25	3.6	V
V_{INPUT}[1]	V_{IL} = –0.3	V_{IH} = +3.6	V_{IL} = –0.3	V_{IH} = +3.6	V
T_{AMB}	0	+70	–40	+85	°C

NOTES

[1]The ADSP-2188M is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}; because V_{OH} (max) ≈ V_{DDEXT} (max). This applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DDINT} = max	2.0			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
		@ V_{DDEXT} = min, I_{OH} = –100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 2.75, t_{CK} = 15 ns		9		mA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 2.75, t_{CK} = 13.3 ns		10		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.75, t_{CK} = 15 ns[11], T_{AMB} = 25°C		44		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.75, t_{CK} = 13.3 ns[11], T_{AMB} = 25°C		42		mA
I_{DD}	Supply Current (Power-Down)[12]	@ V_{DDINT} = 2.75, T_{AMB} = 25°C in Lowest Power Mode		100		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 2.75 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.75 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2188M outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$.

[9]Idle refers to ADSP-2188M state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[11]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]See Chapter 9 of the *ADSP-2100 Family User's Manual* for details.

[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK}$ + 10		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK}$ – 5		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK}$ + 4	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag Outputs = PFx, FL0, FL1, FL2, FO.

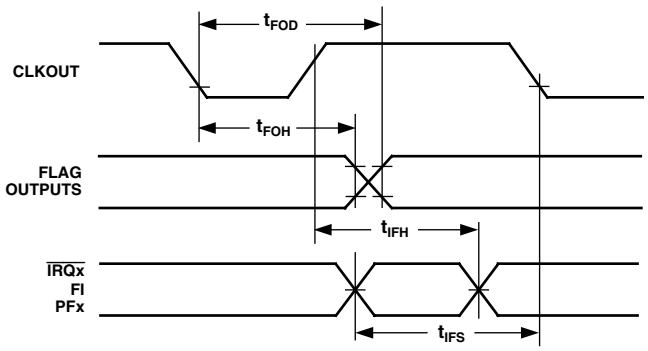


Figure 22. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 10$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

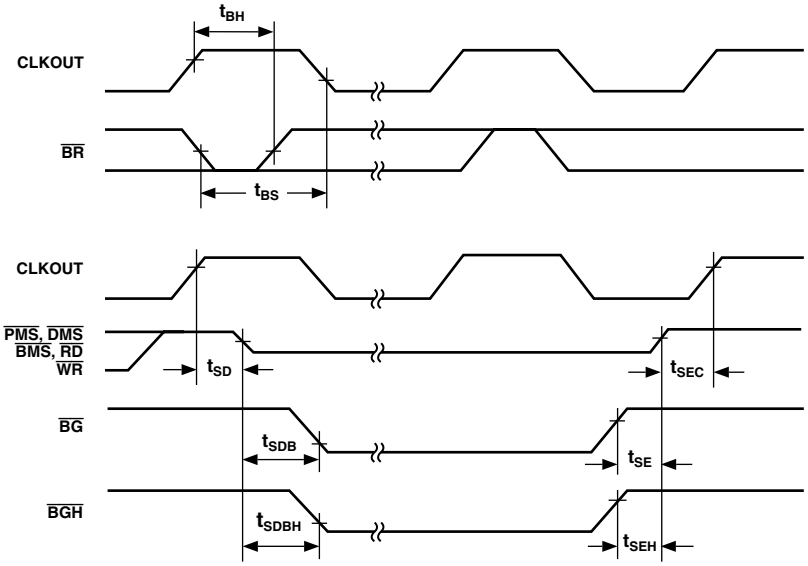


Figure 23. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

NOTES
w = wait states x t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

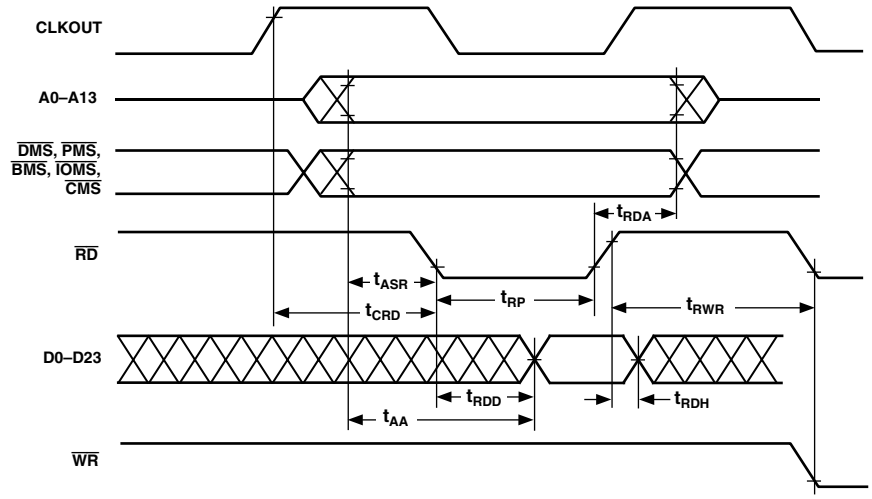


Figure 24. Memory Read

Serial Ports

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	26.6		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK}$ + 6	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		12	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		12	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		12	ns
t_{SCDD}	SCLK High to DT Disable		12	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		12	ns

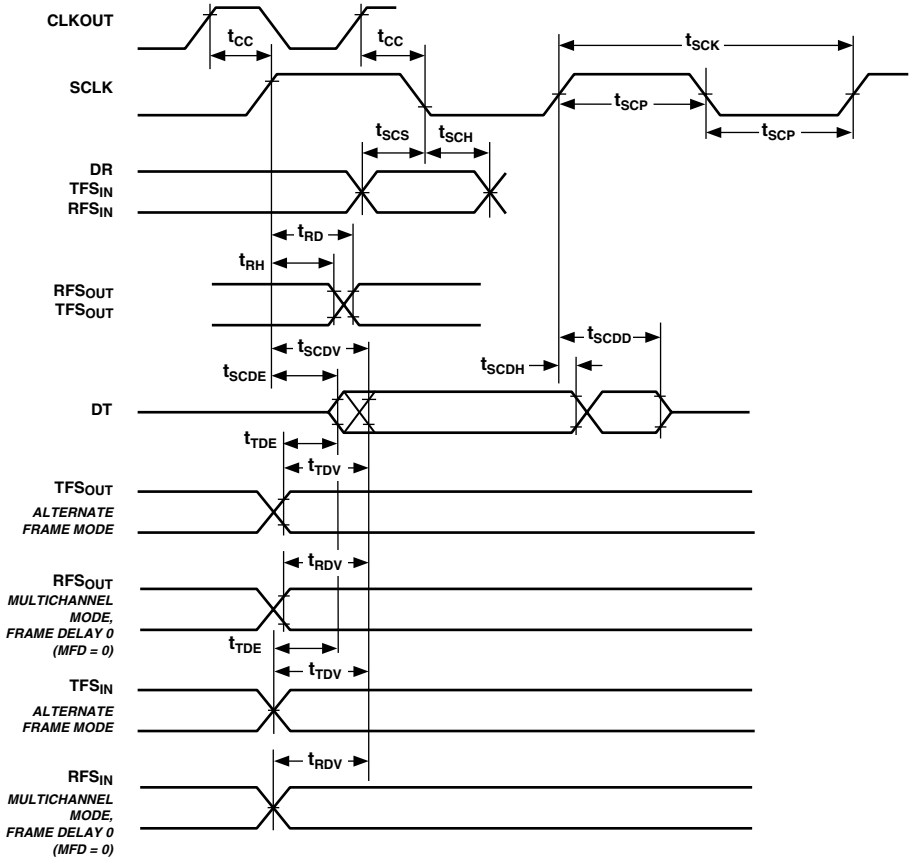


Figure 26. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	3		ns
t_{IKA}	$\overline{\text{IACK}}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{\text{IS}}$ Low and IAL High.
[2]End of Address Latch = $\overline{\text{IS}}$ High or IAL Low.
[3]Start of Write or Read = $\overline{\text{IS}}$ Low and $\overline{\text{IWR}}$ Low or $\overline{\text{IRD}}$ Low.

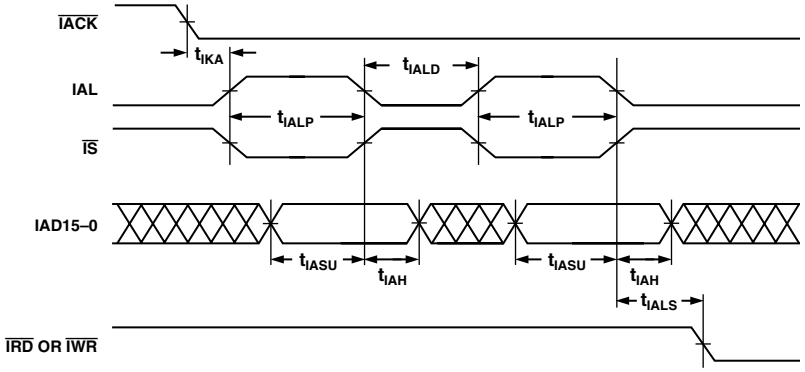


Figure 27. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	$0.5t_{CK} - 2$		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		11	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

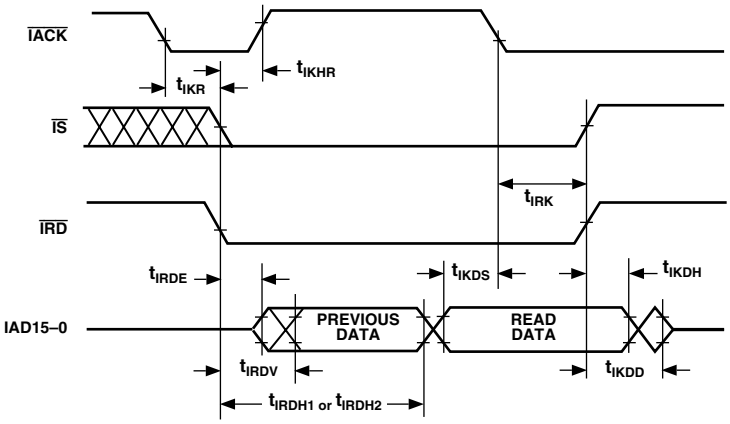


Figure 30. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle[1, 2]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4]	10	$2t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[5]	10	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[6]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[6]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Short Read Only must be disabled in the IDMA Overlay memory mapped register.
[2]Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4]DM Read or first half of PM Read.
[5]Second half of PM Read.
[6]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

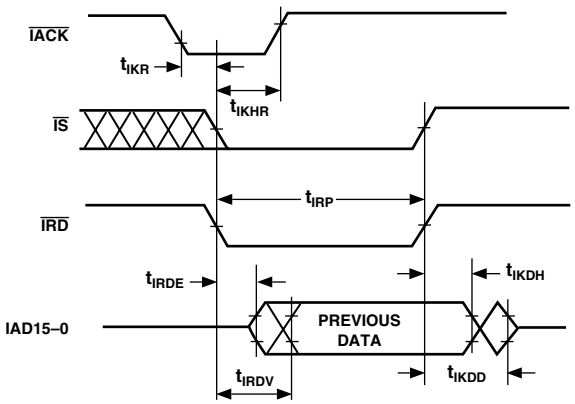


Figure 31. IDMA Read, Short Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle in Short Read Only Mode[1]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

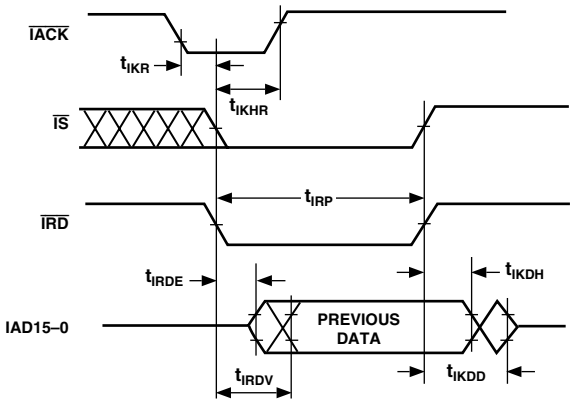
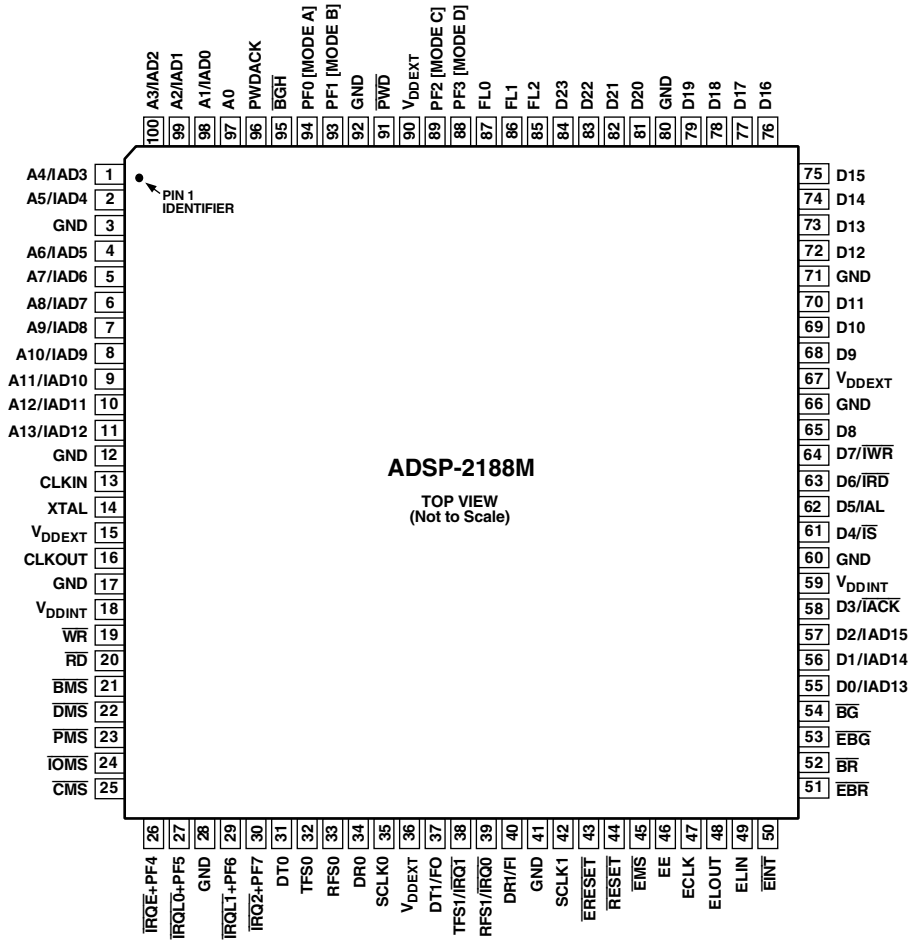


Figure 32. IDMA Read, Short Read Only Cycle

100-LEAD LQFP PIN CONFIGURATION



The LQFP package pinout is shown in the table below. Pin names in bold text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

LQFP Package Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A4/**IAD3**	26	$\overline{\text{IRQE}}$ + PF4	51	$\overline{\text{EBR}}$	76	D16
2	A5/**IAD4**	27	$\overline{\text{IRQL0}}$ + PF5	52	$\overline{\text{BR}}$	77	D17
3	GND	28	GND	53	$\overline{\text{EBG}}$	78	D18
4	A6/**IAD5**	29	$\overline{\text{IRQL1}}$ + PF6	54	$\overline{\text{BG}}$	79	D19
5	A7/**IAD6**	30	$\overline{\text{IRQ2}}$ + PF7	55	D0/**IAD13**	80	GND
6	A8/**IAD7**	31	DT0	56	D1/**IAD14**	81	D20
7	A9/**IAD8**	32	TFS0	57	D2/**IAD15**	82	D21
8	A10/**IAD9**	33	RFS0	58	D3/$\overline{\textbf{IACK}}$	83	D22
9	A11/**IAD10**	34	DR0	59	V_{DDINT}	84	D23
10	A12/**IAD11**	35	SCLK0	60	GND	85	FL2
11	A13/**IAD12**	36	V_{DDEXT}	61	D4/$\overline{\textbf{IS}}$	86	FL1
12	GND	37	DT1/FO	62	D5/**IAL**	87	FL0
13	CLKIN	38	TFS1/$\overline{\text{IRQ1}}$	63	D6/$\overline{\textbf{IRD}}$	88	PF3 [MODE D]
14	XTAL	39	RFS1/$\overline{\text{IRQ0}}$	64	D7/$\overline{\textbf{IWR}}$	89	PF2 [MODE C]
15	V_{DDEXT}	40	DR1/FI	65	D8	90	V_{DDEXT}
16	CLKOUT	41	GND	66	GND	91	$\overline{\text{PWD}}$
17	GND	42	SCLK1	67	V_{DDEXT}	92	GND
18	V_{DDINT}	43	$\overline{\text{ERESET}}$	68	D9	93	PF1 [MODE B]
19	$\overline{\text{WR}}$	44	$\overline{\text{RESET}}$	69	D10	94	PF0 [MODE A]
20	$\overline{\text{RD}}$	45	$\overline{\text{EMS}}$	70	D11	95	$\overline{\text{BGH}}$
21	$\overline{\text{BMS}}$	46	EE	71	GND	96	PWDACK
22	$\overline{\text{DMS}}$	47	ECLK	72	D12	97	A0
23	$\overline{\text{PMS}}$	48	ELOUT	73	D13	98	A1/**IAD0**
24	$\overline{\text{IOMS}}$	49	ELIN	74	D14	99	A2/**IAD1**
25	$\overline{\text{CMS}}$	50	$\overline{\text{EINT}}$	75	D15	100	A3/**IAD2**

144-Ball Mini-BGA Package Pinout (Bottom View)

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{PWD}$	A7/IAD6	A5/IAD4	$\overline{RD}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{BGH}$	NC	$\overline{WR}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{IWR}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{IS}$	NC	NC	D5/IAL	D6/$\overline{IRD}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{IACK}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{BG}$	RFS1/$\overline{IRQ0}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{EBG}$	$\overline{BR}$	$\overline{EBR}$	$\overline{ERESET}$	SCLK1	TFS1/$\overline{IRQ1}$	RFS0	$\overline{DMS}$	$\overline{BMS}$	NC	NC	NC	K
$\overline{EINT}$	ELOUT	ELIN	$\overline{RESET}$	GND	DR0	$\overline{PMS}$	GND	$\overline{IOMS}$	$\overline{IRQL1}$ + PF6	NC	$\overline{IRQE}$ + PF4	L
ECLK	EE	$\overline{EMS}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{CMS}$	NC	$\overline{IRQ2}$ + PF7	$\overline{IRQL0}$ + PF5	M