Microchip Technology - PIC18F1220T-I/SS Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f1220t-i-ss

TABLE 3-3: ACTIVITY AND EXIT DELAY ON WAKE FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Clock in Power Managed Mode	Primary System Clock	Power Managed Mode Exit Delay	Clock Ready Status Bit (OSCCON)	Activity during Wake-up from Power Managed Mode	
				Exit by Interrupt	Exit by Reset
Primary System Clock (PRI_IDLE mode)	LP, XT, HS	5-10 μs(5)	OSTS	CPU and peripherals clocked by primary clock and executing instructions.	Not clocked or Two-Speed Start-up (if enabled)(3).
	HSPLL				
	EC, RC, INTRC(1)		—		
	INTOSC(2)		IOFS		
T1OSC or INTRC(1)	LP, XT, HS	OST	OSTS	CPU and peripherals clocked by selected power managed mode clock and executing instructions until primary clock source becomes ready.	
	HSPLL	OST + 2 ms			
	EC, RC, INTRC(1)	5-10 μs(5)	—		
	INTOSC(2)	1 ms(4)	IOFS		
INTOSC(2)	LP, XT, HS	OST	OSTS		
	HSPLL	OST + 2 ms			
	EC, RC, INTRC(1)	5-10 μs(5)	—		
	INTOSC(2)	None	IOFS		
Sleep mode	LP, XT, HS	OST	OSTS	Not clocked or Two-Speed Start-up (if enabled) until primary clock source becomes ready(3).	
	HSPLL	OST + 2 ms			
	EC, RC, INTRC(1)	5-10 μs(5)	—		
	INTOSC(2)	1 ms(4)	IOFS		

Note 1: In this instance, refers specifically to the INTRC clock source.

2: Includes both the INTOSC 8 MHz source and postscaler derived frequencies.

3: Two-Speed Start-up is covered in greater detail in **Section 19.3 “Two-Speed Start-up”**.

4: Execution continues during the INTOSC stabilization period.

5: Required delay when waking from Sleep and all Idle modes. This delay runs concurrently with any other required delays (see **Section 3.3 “Idle Modes”**).

TABLE 4-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TOSU	1220	1320	---0 0000	---0 0000	---0 uuuu(3)
TOSH	1220	1320	0000 0000	0000 0000	uuuu uuuu(3)
TOSL	1220	1320	0000 0000	0000 0000	uuuu uuuu(3)
STKPTR	1220	1320	00-0 0000	00-0 0000	uu-u uuuu(3)
PCLATU	1220	1320	---0 0000	---0 0000	---u uuuu
PCLATH	1220	1320	0000 0000	0000 0000	uuuu uuuu
PCL	1220	1320	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	1220	1320	--00 0000	--00 0000	--uu uuuu
TBLPTRH	1220	1320	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	1220	1320	0000 0000	0000 0000	uuuu uuuu
TABLAT	1220	1320	0000 0000	0000 0000	uuuu uuuu
PRODH	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	1220	1320	0000 000x	0000 000u	uuuu uuuu(1)
INTCON2	1220	1320	1111 -1-1	1111 -1-1	uuuu -u-u(1)
INTCON3	1220	1320	11-0 0-00	11-0 0-00	uu-u u-uu(1)
INDF0	1220	1320	N/A	N/A	N/A
POSTINC0	1220	1320	N/A	N/A	N/A
POSTDEC0	1220	1320	N/A	N/A	N/A
PREINC0	1220	1320	N/A	N/A	N/A
PLUSW0	1220	1320	N/A	N/A	N/A
FSR0H	1220	1320	---- 0000	---- 0000	---- uuuu
FSR0L	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	1220	1320	N/A	N/A	N/A
POSTINC1	1220	1320	N/A	N/A	N/A
POSTDEC1	1220	1320	N/A	N/A	N/A
PREINC1	1220	1320	N/A	N/A	N/A
PLUSW1	1220	1320	N/A	N/A	N/A
FSR1H	1220	1320	---- 0000	---- 0000	---- uuuu
FSR1L	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 4-2 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the Oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: Bit 5 of PORTA is enabled if $\overline{\text{MCLR}}$ is disabled.

TABLE 4-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TMR3H	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
T3CON	1220	1320	0-00 0000	u-uu uuuu	u-uu uuuu
SPBRGH	1220	1320	0000 0000	0000 0000	uuuu uuuu
SPBRG	1220	1320	0000 0000	0000 0000	uuuu uuuu
RCREG	1220	1320	0000 0000	0000 0000	uuuu uuuu
TXREG	1220	1320	0000 0000	0000 0000	uuuu uuuu
TXSTA	1220	1320	0000 0010	0000 0010	uuuu uuuu
RCSTA	1220	1320	0000 000x	0000 000x	uuuu uuuu
BAUDCTL	1220	1320	-1-1 0-00	-1-1 0-00	-u-u u-uu
EEADR	1220	1320	0000 0000	0000 0000	uuuu uuuu
EEDATA	1220	1320	0000 0000	0000 0000	uuuu uuuu
EECON2	1220	1320	0000 0000	0000 0000	0000 0000
EECON1	1220	1320	xx-0 x000	uu-0 u000	uu-0 u000
IPR2	1220	1320	1--1 -11-	1--1 -11-	u--u -uu-
PIR2	1220	1320	0--0 -00-	0--0 -00-	u--u -uu-(1)
PIE2	1220	1320	0--0 -00-	0--0 -00-	u--u -uu-
IPR1	1220	1320	-111 -111	-111 -111	-uuu -uuu
PIR1	1220	1320	-000 -000	-000 -000	-uuu -uuu(1)
PIE1	1220	1320	-000 -000	-000 -000	-uuu -uuu
OSCTUNE	1220	1320	--00 0000	--00 0000	--uu uuuu
TRISB	1220	1320	1111 1111	1111 1111	uuuu uuuu
TRISA(5)	1220	1320	11-1 1111(5)	11-1 1111(5)	uu-u uuuu(5)
LATB	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATA(5)	1220	1320	xx-x xxxx(5)	uu-u uuuu(5)	uu-u uuuu(5)
PORTB	1220	1320	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA(5,6)	1220	1320	xx0x 0000(5,6)	uu0u 0000(5,6)	uuuu uuuu(5,6)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 4-2 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the Oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: Bit 5 of PORTA is enabled if $\overline{\text{MCLR}}$ is disabled.

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

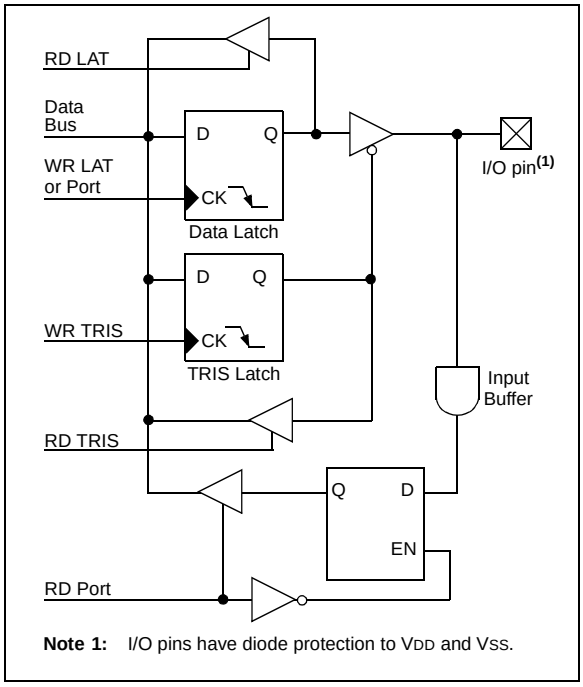
Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch (LATA) register is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port without the interfaces to other peripherals is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin.

The sixth pin of PORTA ($\overline{\text{MCLR}}$/VPP/RA5) is an input only pin. Its operation is controlled by the MCLRE configuration bit in Configuration Register 3H (CONFIG3H<7>). When selected as a port pin (MCLRE = 0), it functions as a digital input only pin; as such, it does not have TRIS or LAT bits associated with its operation. Otherwise, it functions as the device's Master Clear input. In either configuration, RA5 also functions as the programming voltage input during programming.

Note:	On a Power-on Reset, RA5 is enabled as a digital input only if Master Clear functionality is disabled.

Pins RA6 and RA7 are multiplexed with the main oscillator pins; they are enabled as oscillator or I/O pins by the selection of the main oscillator in Configuration Register 1H (see **Section 19.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the LVD input. The operation of pins RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note:	On a Power-on Reset, RA3:RA0 are configured as analog inputs and read as '0'. RA4 is always a digital pin.

The RA4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0x7F    ; Configure A/D
MOVWF   ADCON1  ; for digital inputs
MOVLW   0xD0    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as outputs
                ; RA<7:4> as inputs
```

FIGURE 10-6: $\overline{\text{MCLR}}$/VPP/RA5 PIN BLOCK DIAGRAM

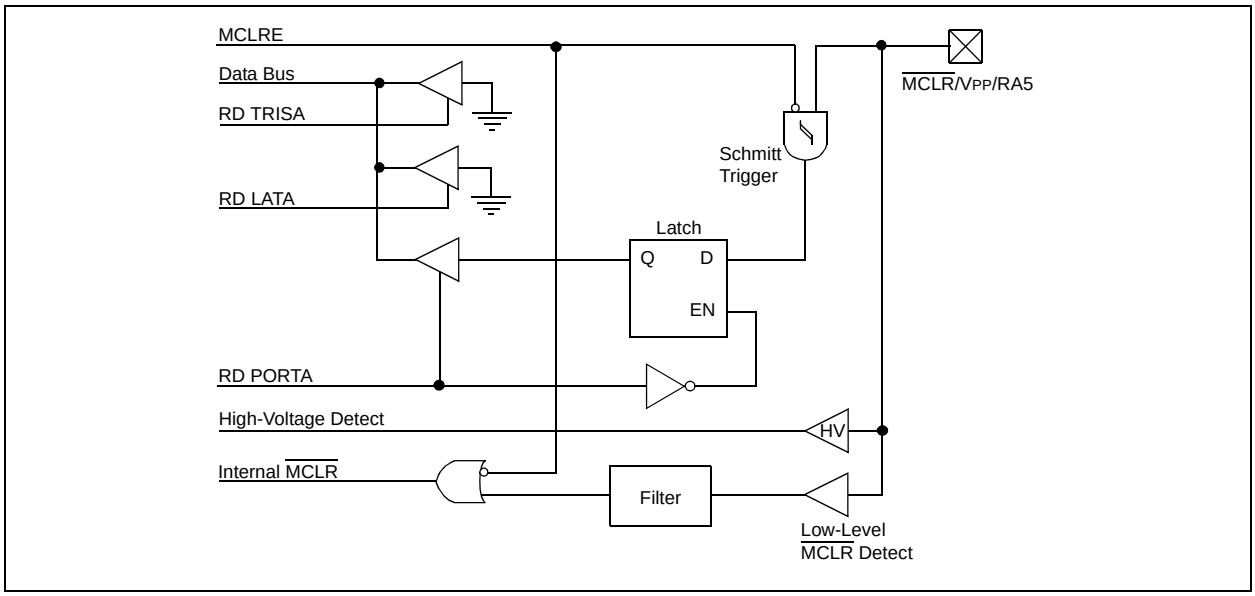


TABLE 10-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	ST	Input/output port pin or analog input.
RA1/AN1/LVDIN	bit 1	ST	Input/output port pin, analog input or Low-Voltage Detect input.
RA2/AN2/VREF-	bit 2	ST	Input/output port pin, analog input or VREF-.
RA3/AN3/VREF+	bit 3	ST	Input/output port pin, analog input or VREF+.
RA4/T0CKI	bit 4	ST	Input/output port pin or external clock input for Timer0. Output is open-drain type.
$\overline{\text{MCLR}}$/VPP/RA5	bit 5	ST	Master Clear input or programming voltage input (if $\overline{\text{MCLR}}$ is enabled); input only port pin or programming voltage input (if $\overline{\text{MCLR}}$ is disabled).
OSC2/CLKO/RA6	bit 6	ST	OSC2, clock output or I/O pin.
OSC1/CLKI/RA7	bit 7	ST	OSC1, clock input or I/O pin.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 10-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

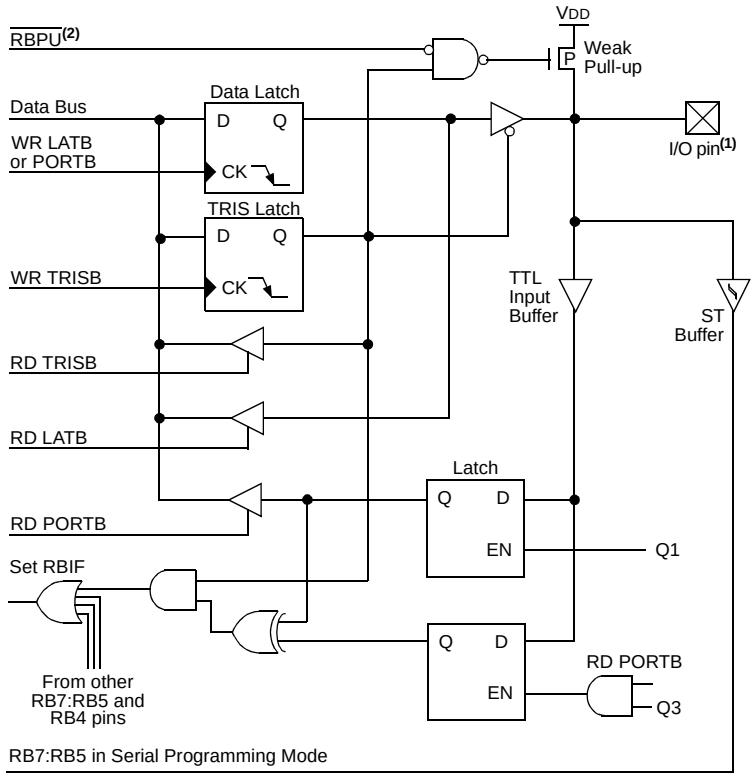
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PORTA	RA7(1)	RA6(1)	RA5(2)	RA4	RA3	RA2	RA1	RA0	xx0x 0000	uu0u 0000
LATA	LATA7(1)	LATA6(1)	—	LATA Data Output Register					xx-x xxxx	uu-u uuuu
TRISA	TRISA7(1)	TRISA6(1)	—	PORTA Data Direction Register					11-1 1111	11-1 1111
ADCON1	—	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: RA7:RA6 and their associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.

2: RA5 is an input only if $\overline{\text{MCLR}}$ is disabled.

FIGURE 10-12: BLOCK DIAGRAM OF RB5/PGM/KBI1 PIN



Note 1: I/O pins have diode protection to VDD and VSS.

2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (INTCON2<7>).

12.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

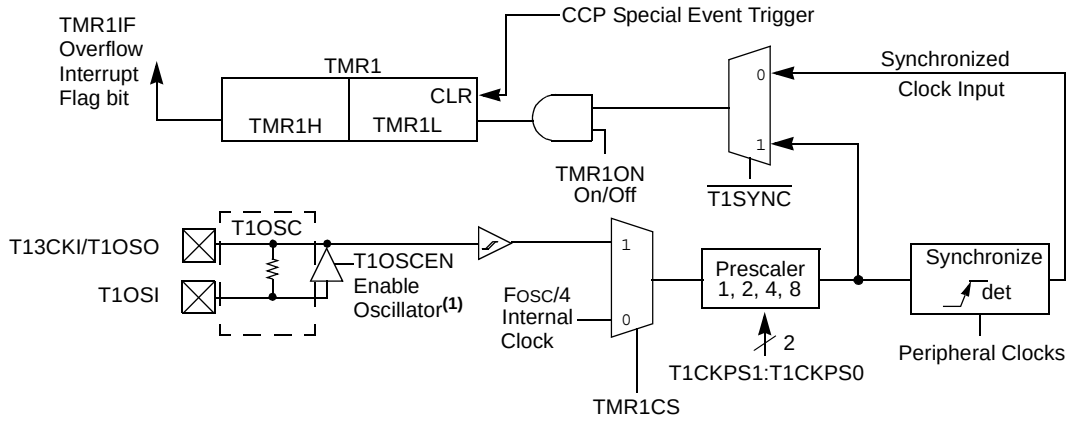
The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

When TMR1CS = 0, Timer1 increments every instruction cycle. When TMR1CS = 1, Timer1 increments on every rising edge of the external clock input, or the Timer1 oscillator, if enabled.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RB7/PGD/T1OSI/P1D/KBI3 and RB6/T1OSO/T13CKI/P1C/KBI2 pins become inputs. That is, the TRISB7:TRISB6 values are ignored and the pins read as '0'.

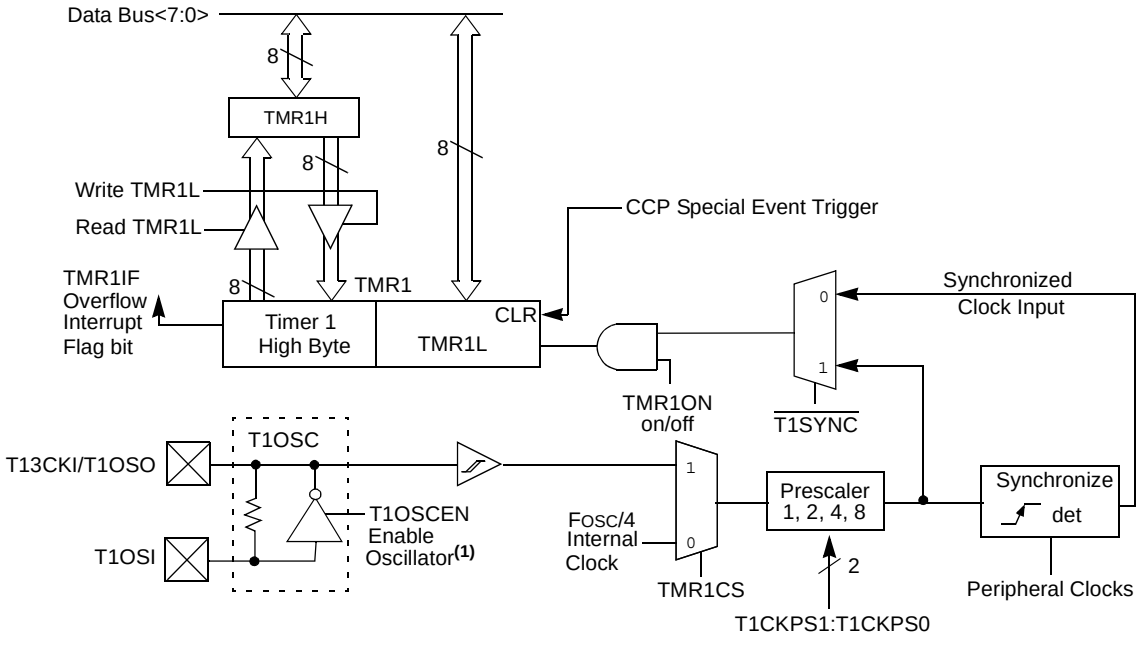
Timer1 also has an internal "Reset input". This Reset can be generated by the CCP module (see **Section 15.4.4 "Special Event Trigger"**).

FIGURE 12-1: TIMER1 BLOCK DIAGRAM



Note 1: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

FIGURE 12-2: TIMER1 BLOCK DIAGRAM: 16-BIT READ/WRITE MODE



Note 1: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

15.0 ENHANCED CAPTURE/ COMPARE/PWM (ECCP) MODULE

The Enhanced CCP module is implemented as a standard CCP module with Enhanced PWM capabilities. These capabilities allow for two or four output channels, user-selectable polarity, dead-band control and automatic shutdown and restart and are discussed in detail in **Section 15.5 "Enhanced PWM Mode"**.

The control register for CCP1 is shown in Register 15-1.

In addition to the expanded functions of the CCP1CON register, the ECCP module has two additional registers associated with Enhanced PWM operation and auto-shutdown features:

- PWM1CON
- ECCPAS

REGISTER 15-1: CCP1CON REGISTER FOR ENHANCED CCP OPERATION

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **P1M<1:0>:** PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as port pins

If CCP1M<3:2> = 11:

00 = Single output; P1A modulated; P1B, P1C, P1D assigned as port pins

01 = Full-bridge output forward; P1D modulated; P1A active; P1B, P1C inactive

10 = Half-bridge output; P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins

11 = Full-bridge output reverse; P1B modulated; P1C active; P1A, P1D inactive

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** ECCP1 Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCP module)

0001 = Unused (reserved)

0010 = Compare mode, toggle output on match (ECCP1IF bit is set)

0011 = Unused (reserved)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (ECCP1IF bit is set)

1001 = Compare mode, clear output on match (ECCP1IF bit is set)

1010 = Compare mode, generate software interrupt on match (ECCP1IF bit is set, ECCP1 pin returns to port pin operation)

1011 = Compare mode, trigger special event (ECCP1IF bit is set; ECCP resets TMR1 or TMR3 and starts an A/D conversion if the A/D module is enabled)

1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high

1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low

1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high

1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

15.5.6 PROGRAMMABLE DEAD-BAND DELAY

In half-bridge applications where all power switches are modulated at the PWM frequency at all times, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (shoot-through current) may flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In the Half-Bridge Output mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 15-6 for an illustration. The lower seven bits of the PWM1CON register (Register 15-2) sets the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

15.5.7 ENHANCED PWM AUTO-SHUTDOWN

When the ECCP is programmed for any of the Enhanced PWM modes, the active output pins may be configured for auto-shutdown. Auto-shutdown immediately places the Enhanced PWM output pins into a defined shutdown state when a shutdown event occurs.

A shutdown event can be caused by the INT0, INT1 or INT2 pins (or any combination of these three sources). The auto-shutdown feature can be disabled by not selecting any auto-shutdown sources. The auto-shutdown sources to be used are selected using the ECCPAS2:ECCPAS0 bits (bits <6:4> of the ECCPAS register).

When a shutdown occurs, the output pins are asynchronously placed in their shutdown states, specified by the PSSAC1:PSSAC0 and PSSBD1:PSSBD0 bits (ECCPAS<3:0>). Each pin pair (P1A/P1C and P1B/P1D) may be set to drive high, drive low or be tri-stated (not driving). The ECCPASE bit (ECCPAS<7>) is also set to hold the Enhanced PWM outputs in their shutdown states.

The ECCPASE bit is set by hardware when a shutdown event occurs. If automatic restarts are not enabled, the ECCPASE bit is cleared by firmware when the cause of the shutdown clears. If automatic restarts are enabled, the ECCPASE bit is automatically cleared when the cause of the auto-shutdown has cleared.

If the ECCPASE bit is set when a PWM period begins, the PWM outputs remain in their shutdown state for that entire PWM period. When the ECCPASE bit is cleared, the PWM outputs will return to normal operation at the beginning of the next PWM period.

Note:	Writing to the ECCPASE bit is disabled while a shutdown condition is active.

REGISTER 15-2: PWM1CON: PWM CONFIGURATION REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **PRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits

Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active.

TABLE 16-3: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0											
	FOSC = 40.000 MHz			FOSC = 20.000 MHz			FOSC = 10.000 MHz			FOSC = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
2.4	—	—	—	—	—	—	2.441	1.73	255	2403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0								
	FOSC = 4.000 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	300	-0.16	207
1.2	1.202	0.16	207	1201	-0.16	103	1201	-0.16	51
2.4	2.404	0.16	103	2403	-0.16	51	2403	-0.16	25
9.6	9.615	0.16	25	9615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 1											
	FOSC = 40.000 MHz			FOSC = 20.000 MHz			FOSC = 10.000 MHz			FOSC = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.00	8332	0.300	0.02	4165	0.300	0.02	2082	300	-0.04	1665
1.2	1.200	0.02	2082	1.200	-0.03	1041	1.200	-0.03	520	1201	-0.16	415
2.4	2.402	0.06	1040	2.399	-0.03	520	2.404	0.16	259	2403	-0.16	207
9.6	9.615	0.16	259	9.615	0.16	129	9.615	0.16	64	9615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 1								
	FOSC = 4.000 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.04	832	300	-0.16	415	300	-0.16	207
1.2	1.202	0.16	207	1201	-0.16	103	1201	-0.16	51
2.4	2.404	0.16	103	2403	-0.16	51	2403	-0.16	25
9.6	9.615	0.16	25	9615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

To set up an Asynchronous Transmission:

1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, set enable bit TXIE.
4. If 9-bit transmission is desired, set transmit bit TX9. Can be used as address/data bit.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 16-2: EUSART TRANSMIT BLOCK DIAGRAM

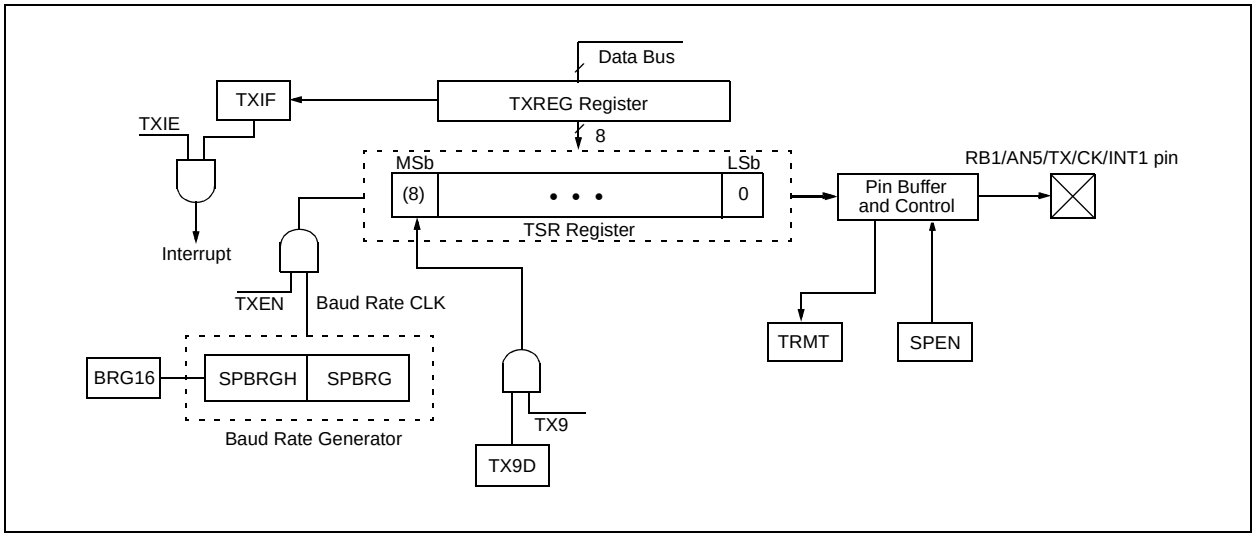
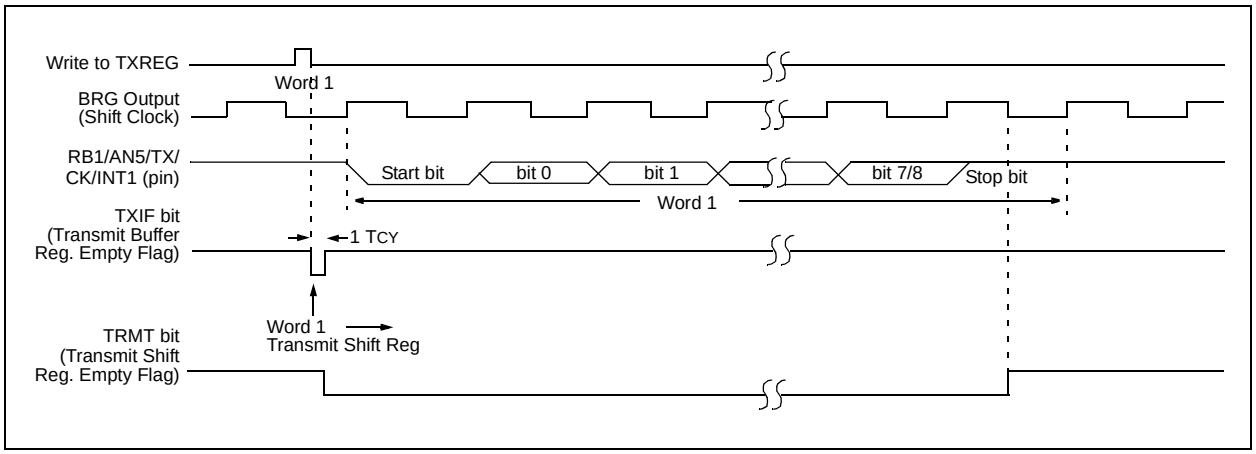


FIGURE 16-3: ASYNCHRONOUS TRANSMISSION



REGISTER 19-8: CONFIG6L: CONFIGURATION REGISTER 6 LOW (BYTE ADDRESS 30000Ah)

U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
—	—	—	—	—	—	WRT1	WRT0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	P = Programmable bit

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **WRT1:** Write Protection bit (PIC18F1320)
1 = Block 1 (001000-001FFFh) not write-protected
0 = Block 1 (001000-001FFFh) write-protected

bit 0 **WRT0:** Write Protection bit (PIC18F1320)
1 = Block 0 (00200-000FFFh) not write-protected
0 = Block 0 (00200-000FFFh) write-protected

bit 1 **WRT1:** Write Protection bit (PIC18F1220)
1 = Block 1 (000800-000FFFh) not write-protected
0 = Block 1 (000800-000FFFh) write-protected

bit 0 **WRT0:** Write Protection bit (PIC18F1220)
1 = Block 0 (000200-0007FFh) not write-protected
0 = Block 0 (000200-0007FFh) write-protected

REGISTER 19-9: CONFIG6H: CONFIGURATION REGISTER 6 HIGH (BYTE ADDRESS 30000Bh)

R/P-1	R/P-1	R-1	U-0	U-0	U-0	U-0	U-0
WRTD	WRTB	WRTC(1)	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	P = Programmable bit

bit 7 **WRTD:** Data EEPROM Write Protection bit
1 = Data EEPROM not write-protected
0 = Data EEPROM write-protected

bit 6 **WRTB:** Boot Block Write Protection bit
1 = Boot Block (000000-0001FFh) not write-protected
0 = Boot Block (000000-0001FFh) write-protected

bit 5 **WRTC:** Configuration Register Write Protection bit(1)
1 = Configuration registers (300000-3000FFh) not write-protected
0 = Configuration registers (300000-3000FFh) write-protected

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is read-only in normal execution mode; it can be written only in Program mode.

21.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

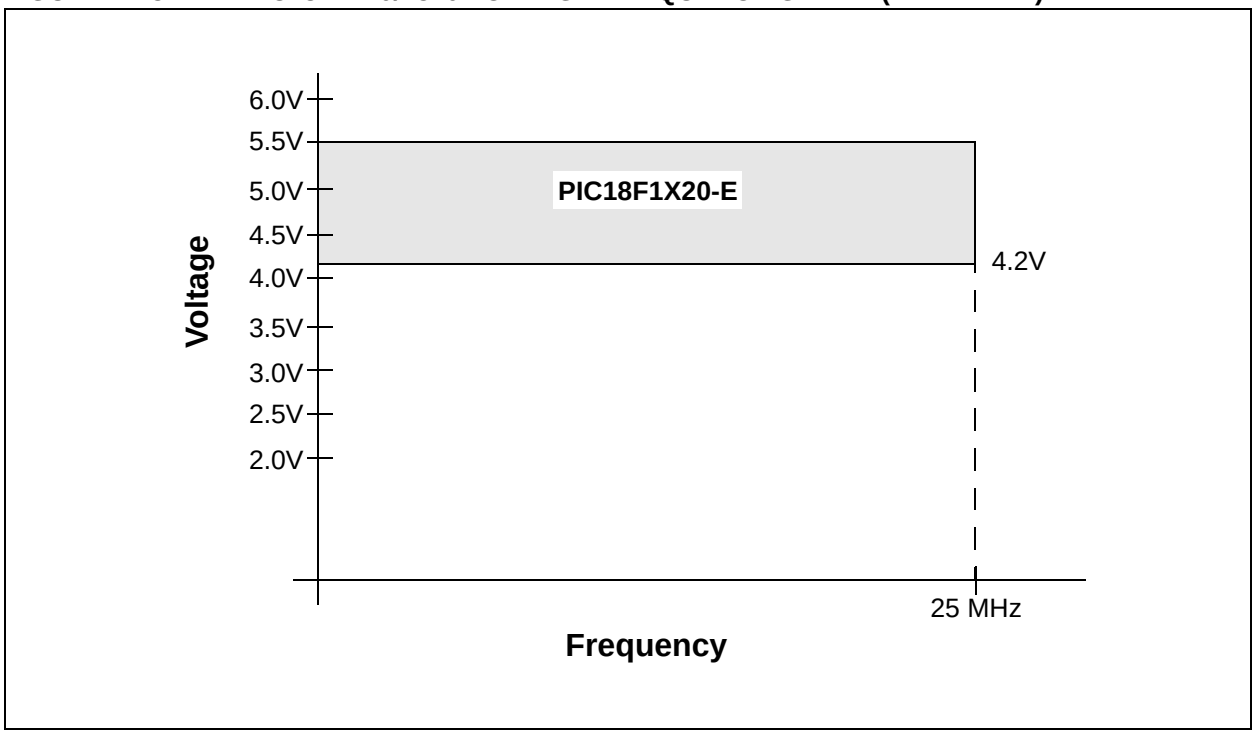
Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

21.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

FIGURE 22-3: PIC18F1220/1320 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



22.2 DC Characteristics: Power-Down and Supply Current PIC18F1220/1320 (Industrial) PIC18LF1220/1320 (Industrial) (Continued)

PIC18LF1220/1320 (Industrial)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F1220/1320 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ.	Max.	Units	Conditions		
	Supply Current (IDD)(2,3)						
	PIC18LF1220/1320	415	600	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**PRI_RUN** mode, EC oscillator)
		425	600	µA	+25°C		
		435	600	µA	+85°C		
	PIC18LF1220/1320	0.87	1.0	mA	-40°C	VDD = 3.0V	
		0.75	1.0	mA	+25°C		
		0.75	1.0	mA	+85°C		
	All devices	1.6	2.0	mA	-40°C	VDD = 5.0V	
		1.6	2.0	mA	+25°C		
		1.5	2.0	mA	+85°C		
	Extended devices	1.5	2.0	mA	+125°C		
	Extended devices	6.3	9.0	mA	+125°C	VDD = 4.2V	FOSC = 25 MHz (**PRI_RUN** mode, EC oscillator)
		9.7	10.0	mA	+125°C	VDD = 5.0V	
	All devices	9.4	12	mA	-40°C	VDD = 4.2V	FOSC = 40 MHz (**PRI_RUN** mode, EC oscillator)
		9.5	12	mA	+25°C		
		9.6	12	mA	+85°C		
	All devices	11.9	15	mA	-40°C	VDD = 5.0V	
		12.1	15	mA	+25°C		
		12.2	15	mA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

FIGURE 23-9: MAXIMUM IDD vs. FOSC OVER VDD PRI_IDLE, EC MODE, -40°C TO +85°C

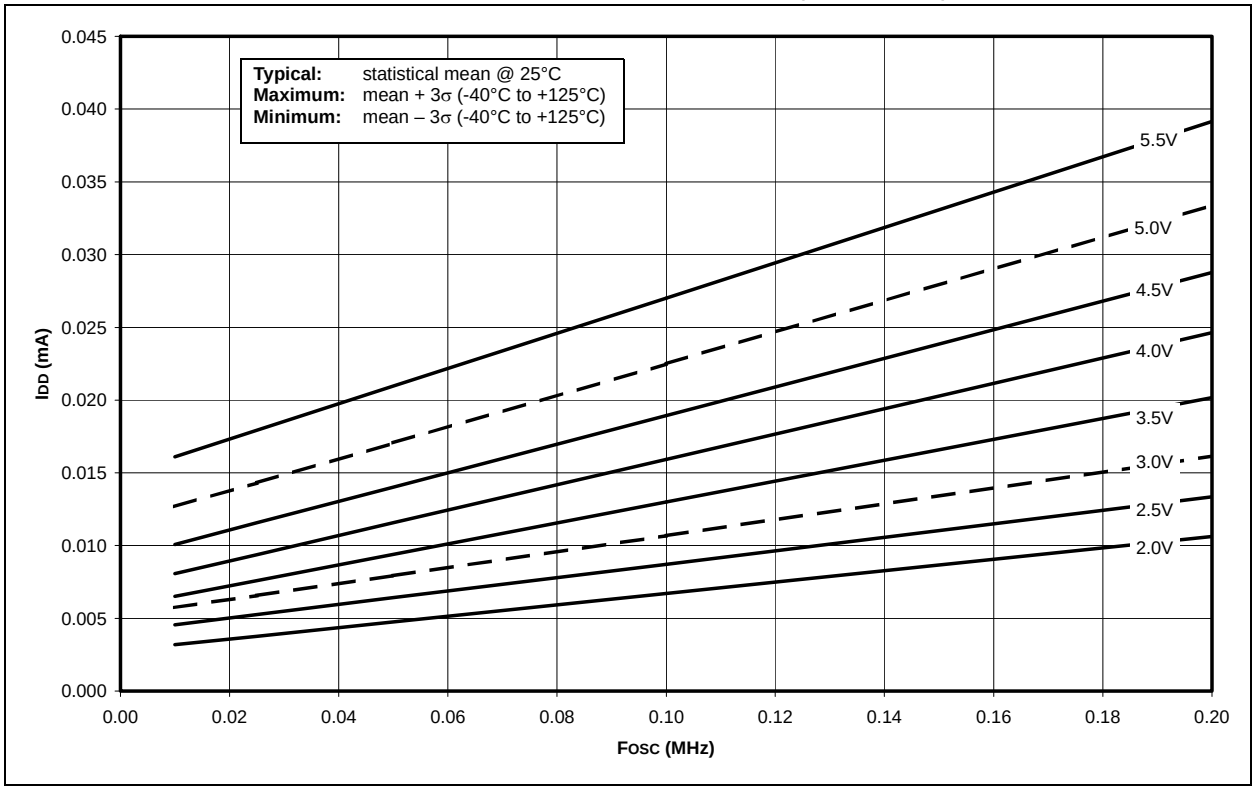


FIGURE 23-10: MAXIMUM IDD vs. FOSC OVER VDD PRI_IDLE, EC MODE, -40°C TO +125°C

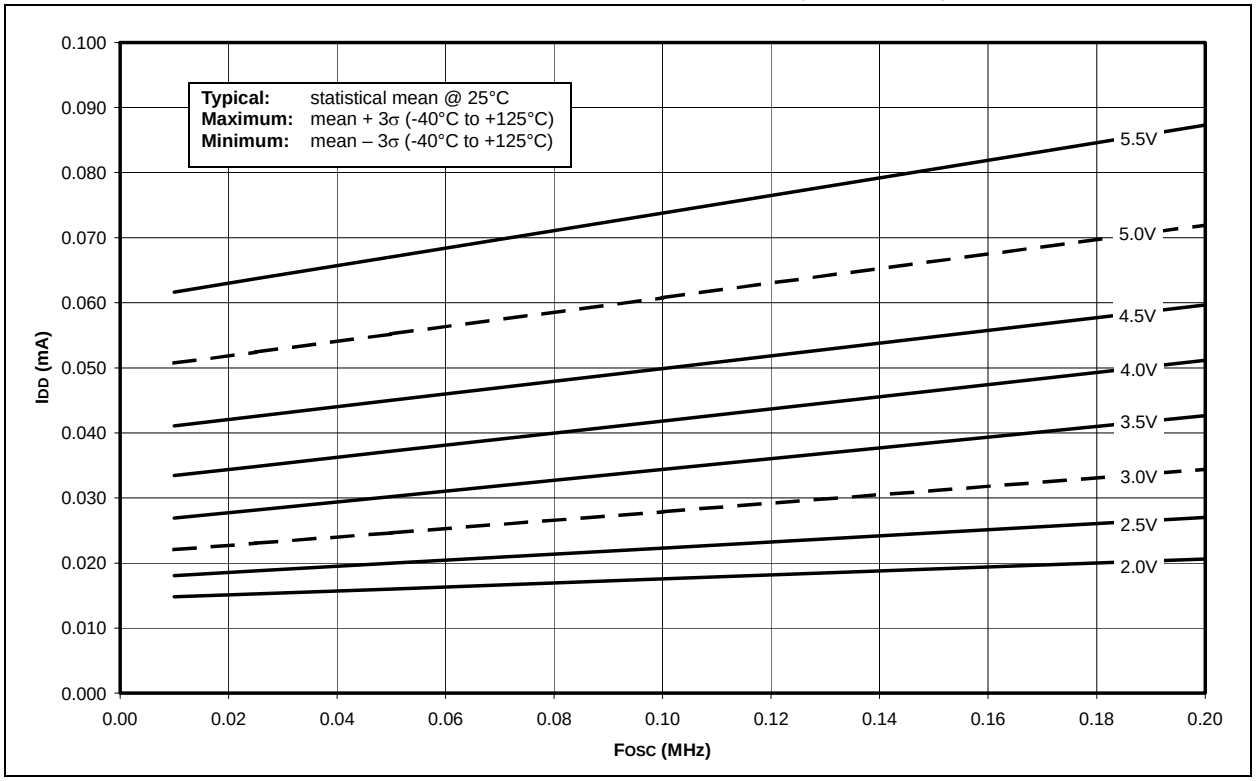


FIGURE 23-13: TYPICAL IDD vs. FOSC OVER VDD PRI_IDLE, EC MODE, +25°C

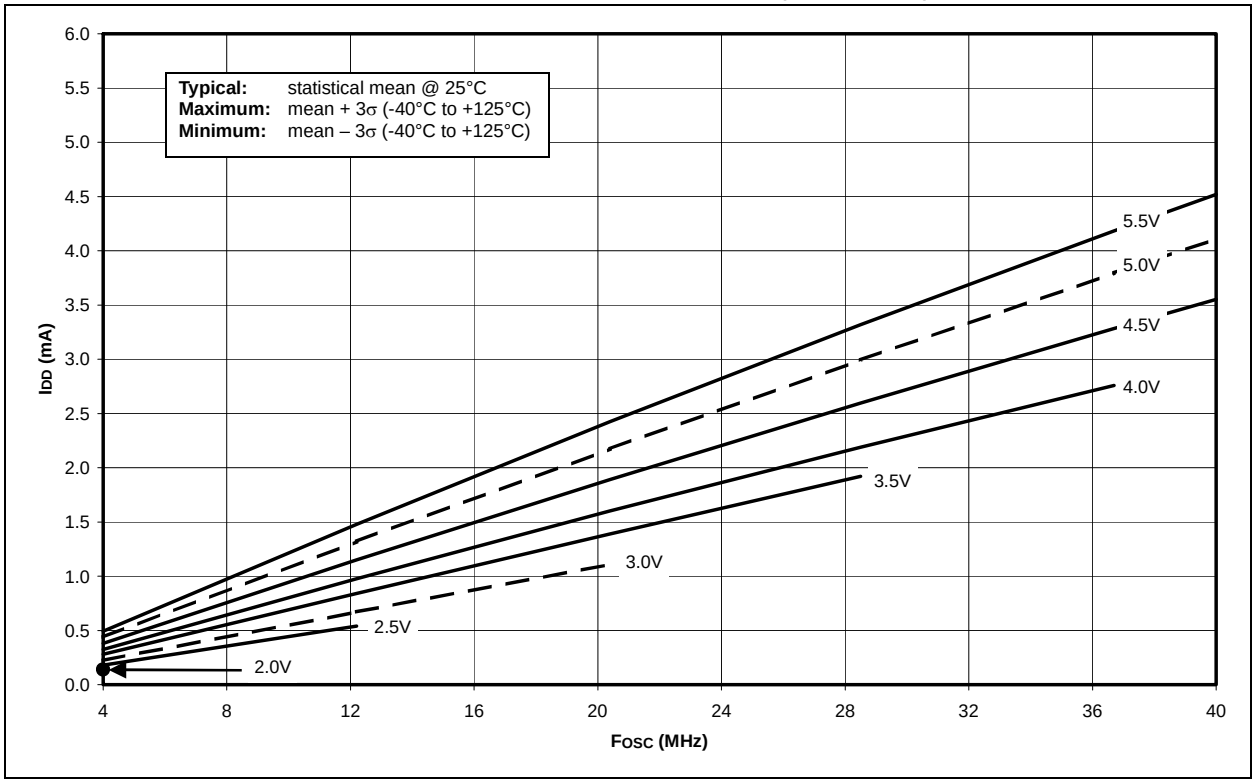


FIGURE 23-14: MAXIMUM IDD vs. FOSC OVER VDD PRI_IDLE, EC MODE, -40°C TO +125°C

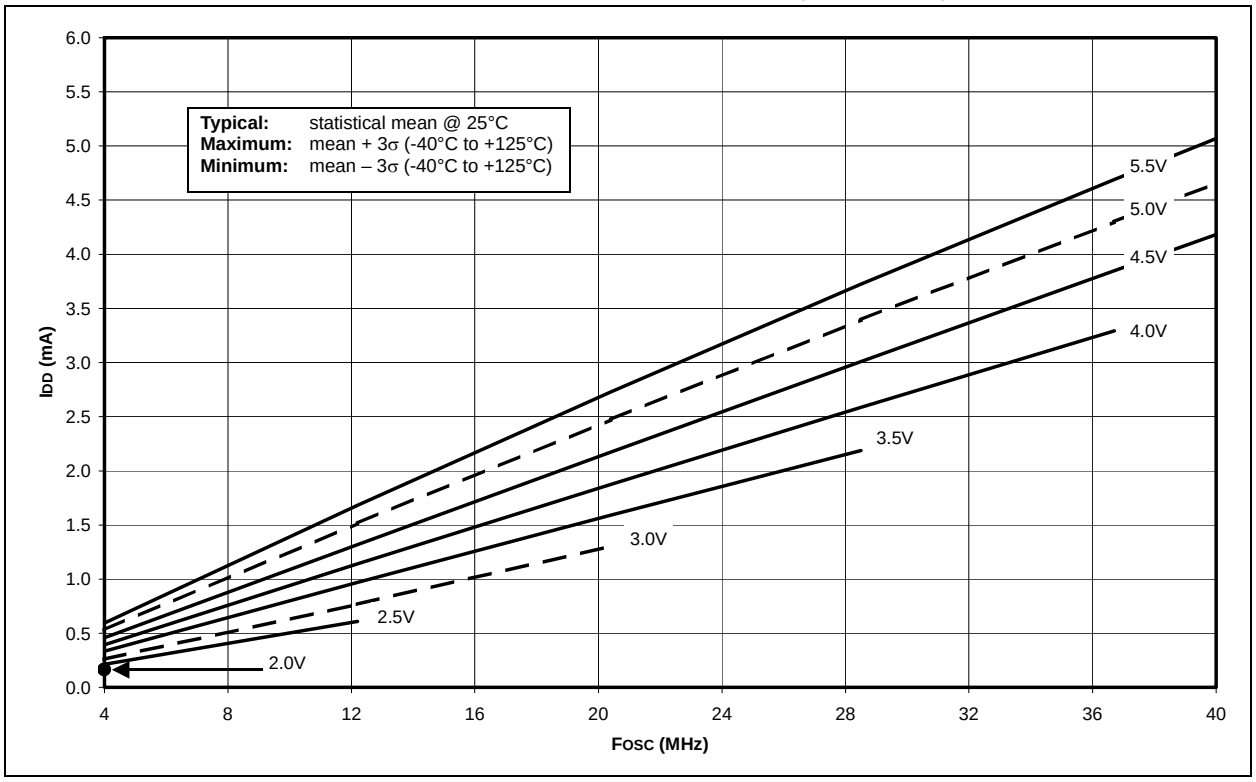


FIGURE 23-19: MAXIMUM IPD vs. VDD (-40°C TO +125°C), 125 kHz TO 8 MHz RC_IDLE MODE, ALL PERIPHERALS DISABLED

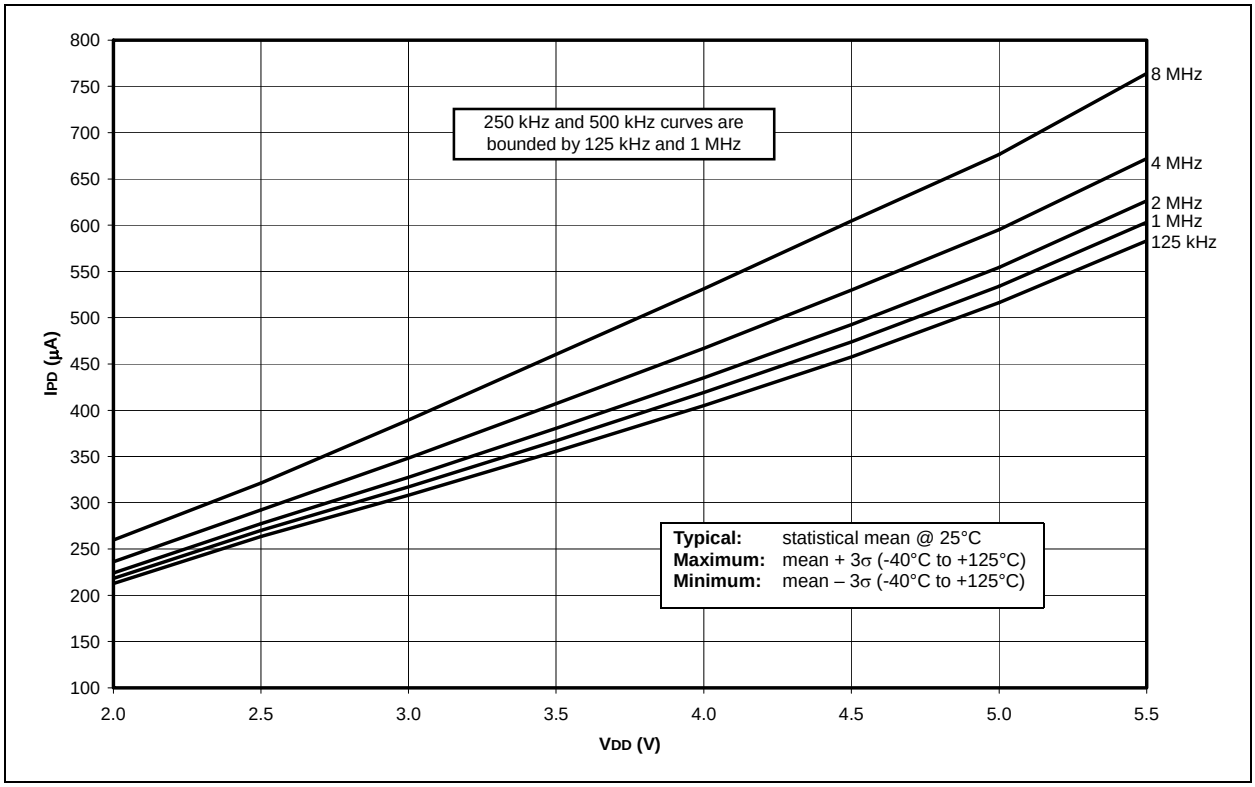
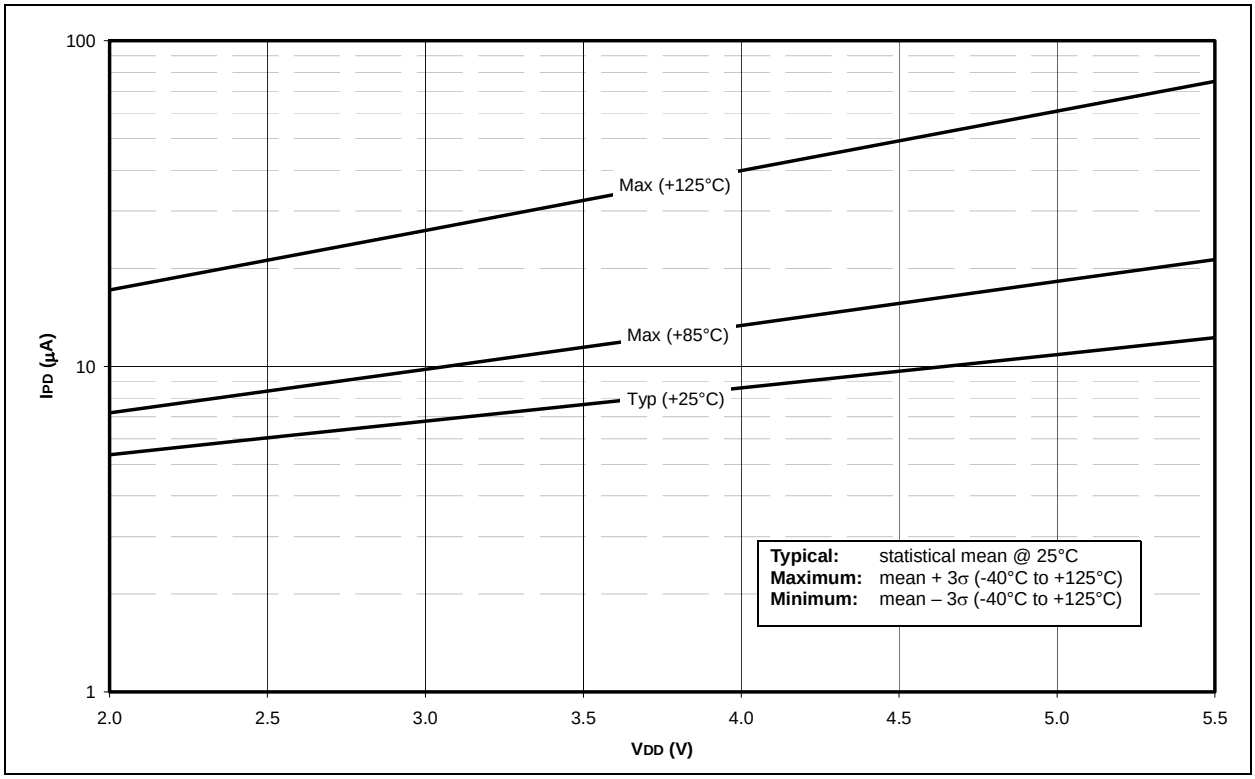
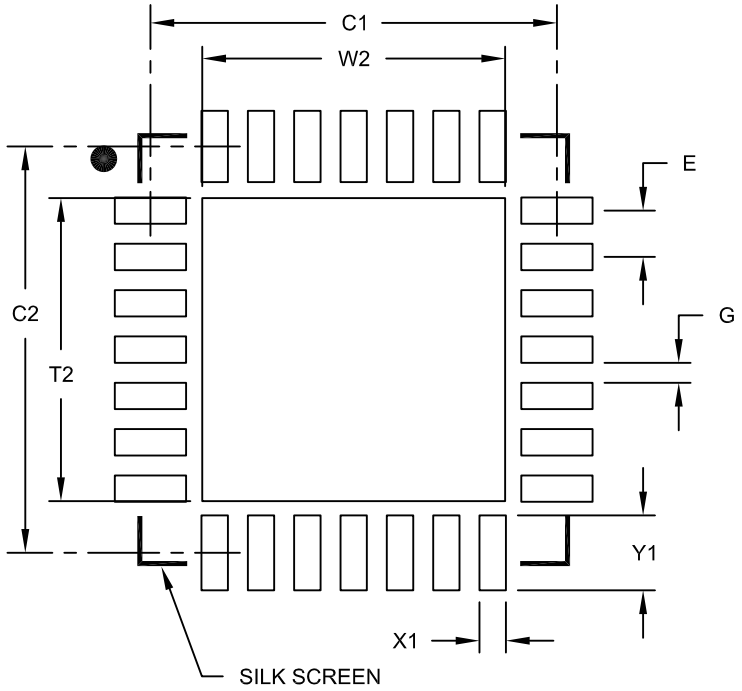


FIGURE 23-20: TYPICAL AND MAXIMUM IPD vs. VDD (-40°C TO +125°C), 31.25 kHz RC_IDLE MODE, ALL PERIPHERALS DISABLED



28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A