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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf1220t-i-ml

[illegible]

Legend:	TTL = TTL compatible input	CMOS = CMOS compatible input or output
	ST = Schmitt Trigger input with CMOS levels	I = Input
	O = Output	P = Power
	OD = Open-drain (no P diode to VDD)	

TABLE 3-2: COMPARISON BETWEEN POWER MANAGED MODES

Power Managed Mode	CPU is Clocked by ...	WDT Time-out causes a ...	Peripherals are Clocked by ...	Clock during Wake-up (while primary becomes ready)
Sleep	Not clocked (not running)	Wake-up	Not clocked	None or INTOSC multiplexer if Two-Speed Start-up or Fail-Safe Clock Monitor are enabled
Any Idle mode	Not clocked (not running)	Wake-up	Primary, Secondary or INTOSC multiplexer	Unchanged from Idle mode (CPU operates as in corresponding Run mode)
Any Run mode	Primary or secondary clocks or INTOSC multiplexer	Reset	Primary or secondary clocks or INTOSC multiplexer	Unchanged from Run mode

3.2 Sleep Mode

The power managed Sleep mode in the PIC18F1220/1320 devices is identical to that offered in all other PIC microcontrollers. It is entered by clearing the IDLEN and SCS1:SCS0 bits (this is the Reset state) and executing the SLEEP instruction. This shuts down the primary oscillator and the OSTS bit is cleared (see Figure 3-1).

When a wake event occurs in Sleep mode (by interrupt, Reset or WDT time-out), the system will not be clocked until the primary clock source becomes ready (see Figure 3-2), or it will be clocked from the internal oscillator block if either the Two-Speed Start-up or the Fail-Safe Clock Monitor are enabled (see Section 19.0 “Special Features of the CPU”). In either case, the OSTS bit is set when the primary clock is providing the system clocks. The IDLEN and SCS bits are not affected by the wake-up.

3.3 Idle Modes

The IDLEN bit allows the microcontroller’s CPU to be selectively shut down while the peripherals continue to operate. Clearing IDLEN allows the CPU to be clocked. Setting IDLEN disables clocks to the CPU, effectively stopping program execution (see Register 2-2). The peripherals continue to be clocked regardless of the setting of the IDLEN bit.

There is one exception to how the IDLEN bit functions. When all the low-power OSCCON bits are cleared (IDLEN:SCS1:SCS0 = 000), the device enters Sleep mode upon the execution of the SLEEP instruction. This is both the Reset state of the OSCCON register and the setting that selects Sleep mode. This maintains compatibility with other PIC devices that do not offer power managed modes.

If the Idle Enable bit, IDLEN (OSCCON<7>), is set to a ‘1’ when a SLEEP instruction is executed, the peripherals will be clocked from the clock source selected using the SCS1:SCS0 bits; however, the CPU will not be clocked. Since the CPU is not executing instructions, the only exits from any of the Idle modes are by interrupt, WDT time-out or a Reset.

When a wake event occurs, CPU execution is delayed approximately 10 μ s while it becomes ready to execute code. When the CPU begins executing code, it is clocked by the same clock source as was selected in the power managed mode (i.e., when waking from RC_IDLE mode, the internal oscillator block will clock the CPU and peripherals until the primary clock source becomes ready – this is essentially RC_RUN mode). This continues until the primary clock source becomes ready. When the primary clock becomes ready, the OSTS bit is set and the system clock source is switched to the primary clock (see Figure 3-4). The IDLEN and SCS bits are not affected by the wake-up.

While in any Idle mode or the Sleep mode, a WDT time-out will result in a WDT wake-up to full-power operation.

16.4 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the RB1/AN5/TX/CK/INT1 and RB4/AN6/RX/DT/KBI0 I/O pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCTL<5>); setting SCKP sets the Idle state on CK as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

16.4.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 16-2. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one T_{CYCLE}), the TXREG is empty and interrupt bit, TXIF (PIR1<4>), is set. The interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit, TXIF, will be set, regardless of the state of enable bit, TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit, TXIF, indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. If interrupts are desired, set enable bit TXIE.
4. If 9-bit transmission is desired, set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

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TABLE 16-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	—	ADIF	RCIF	TXIF	—	CCP1IF	TMR2IF	TMR1IF	-000 -000	-000 -000
PIE1	—	ADIE	RCIE	TXIE	—	CCP1IE	TMR2IE	TMR1IE	-000 -000	-000 -000
IPR1	—	ADIP	RCIP	TXIP	—	CCP1IP	TMR2IP	TMR1IP	-111 -111	-111 -111
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
RCREG	EUSART Receive Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	SENDER	BRGH	TRMT	TX9D	0000 0010	0000 0010
BAUDCTL	—	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	-1-1 0-00	-1-1 0-00
SPBRGH	Baud Rate Generator Register High Byte								0000 0000	0000 0000
SPBRG	Baud Rate Generator Register Low Byte								0000 0000	0000 0000

Legend: x = unknown, — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

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