Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	125
Number of Logic Elements/Cells	1000
Total RAM Bits	65536
Number of I/O	28
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm1k-cm36tr1k

iCE40LM Family Data Sheet Introduction

January 2014 | Data Sheet DS1045

General Description

iCE40LM family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40LM family includes integrated SPI & I^2C blocks to interface with virtually all mobile sensors and application processors. The iCE40LM family also features two Strobe Generators that can generates strobes in Microsecond ranges with the Low-Power Strobe Generator, and also generates strobes in Nanosecond ranges with the High-Speed Strobe Generator.

In addition, the iCE40LM family of devices includes logic to perform other functions such as mobile bridging, antenna tuning, GPIO expansion, motion/gesture recognition, IR remote control, bar code emulation and other custom functions.

The iCE40LM family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
  - Three devices with 1100 to 3520 LUTs
  - 18 I/O pins for 25-pin WLCSP
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - As low as 120 µW standby power typical
- **Embedded and Distributed Memory**
  - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I^2C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Strobe Generators**
  - Low-Power Strobe Generator (Microsecond ranges)
  - High-Speed Strobe Generator (Nanosecond ranges)
- **High Current Drive Outputs for LED**
  - Three High Drive (HD) output in each device
  - Source/sink nominal 24 mA
- **Flexible On-Chip Clocking**
  - Six low-skew global signal resource
- **Flexible Device Configuration**
  - SRAM is configured through SPI
- **Ultra-Small Form Factor**
  - As small as 25-pin WLCSP package 1.71 mm x 1.71 mm

Applications

- Smartphones
- Tablets and Consumer Handheld Devices
- Handheld Commercial and Industrial Devices
- Multi Sensor Management Applications
- Sensor Pre-processing & Sensor Fusion
- Always-On Sensor Applications

Table 1-1. iCE40LM Family Selection Guide

Part Number	iCE40LM1K	iCE40LM2K	iCE40LM4K
Logic Cells (LUT + Flip-Flop)	1100	2048	3520
RAM4K Memory Blocks	16	20	20
RAM4K RAM Bits	64K	80K	80K
Package	Programmable I/O Count		
25-pin WLCSP, 1.71 mm x 1.71 mm, 0.35 mm	18	18	18
36-pin ucBGA, 2.5 mm x 2.5 mm, 0.40 mm	28	28	28
49-pin ucBGA, 3 mm x 3 mm, 0.40 mm	37	37	37

Introduction

The iCE40LM family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), two Strobe Generators (LPSG, HSSG), two hardened I^2C Controllers and two hardened SPI Controllers. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40LM devices are fabricated on a 40nm CMOS low power process. The device architecture has several features such as user configurable I^2C and SPI Controllers, either as master or slave, and two Strobe Generators.

The iCE40LM FPGAs are available in very small form factor packages, with the smallest in 25-pin WLCSP. The 25-pin WLCSP package has a 0.35 mm ball pitch, resulting to an overall package size of 1.71 mm x 1.71 mm that easily fits into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40LM devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

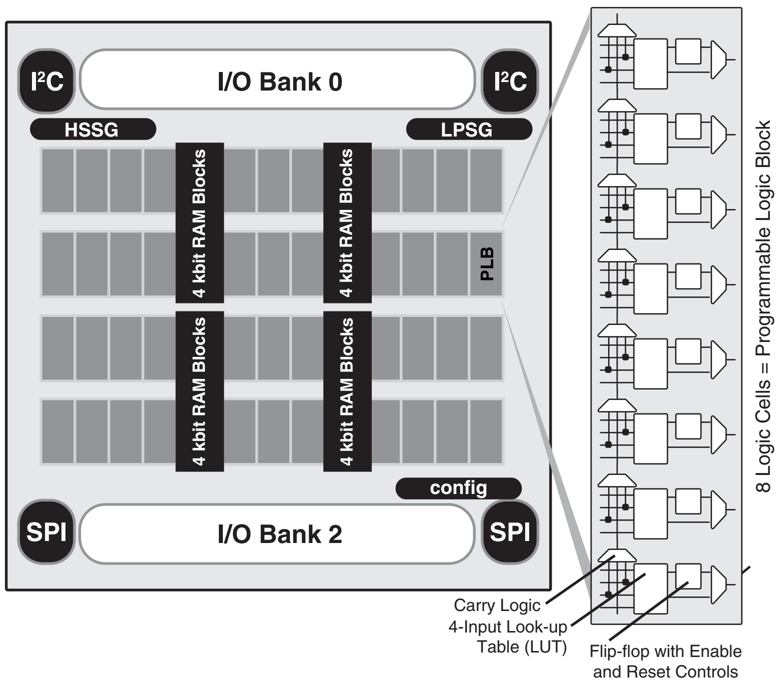
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40LM family of devices. Popular logic synthesis tools provide synthesis library support for iCE40LM. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40LM device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40LM FPGA family. Lattice also can provide fully verified bit-stream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's Reference Designs or fully-verified bitstreams, please contact your local Lattice representative.

Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40LM-4K device.

Figure 2-1. iCE40LM-4K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

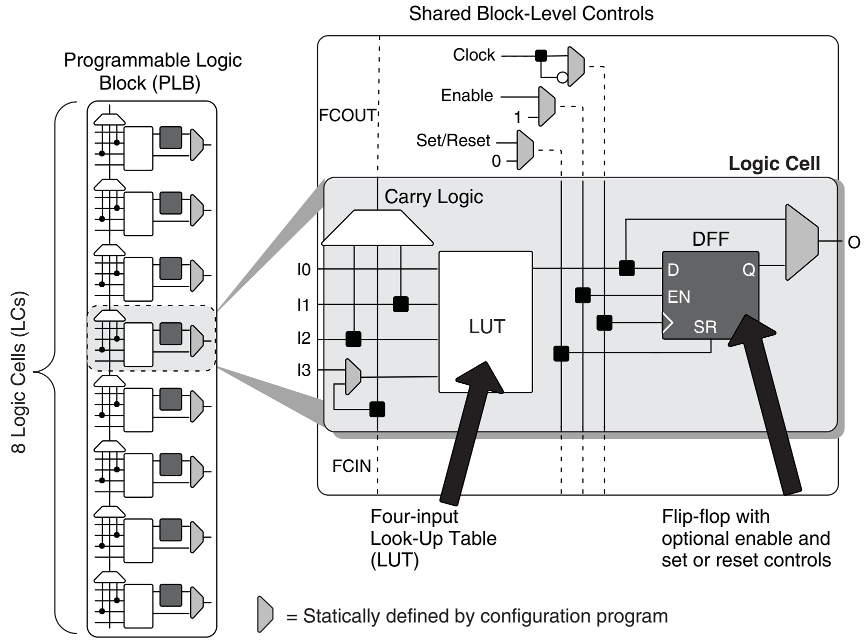
In the iCE40LM family, There are two sysIO banks, one on top and one on bottom. User can connect both V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40LM also includes two user I²C ports, and two Strobe Generators.

PLB Blocks

The core of the iCE40LM device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

sysCLOCK Phase Locked Loops (PLLs) - *NOT SUPPORTED on the 25-Pin WLCSP*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40LM devices have one sysCLOCK PLL (Please note that the 25-pin WLCSP package does not support the PLL). REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal strobe generator or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

The iCE40LM PLL functions the same as the PLLs in the iCE40 family. For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

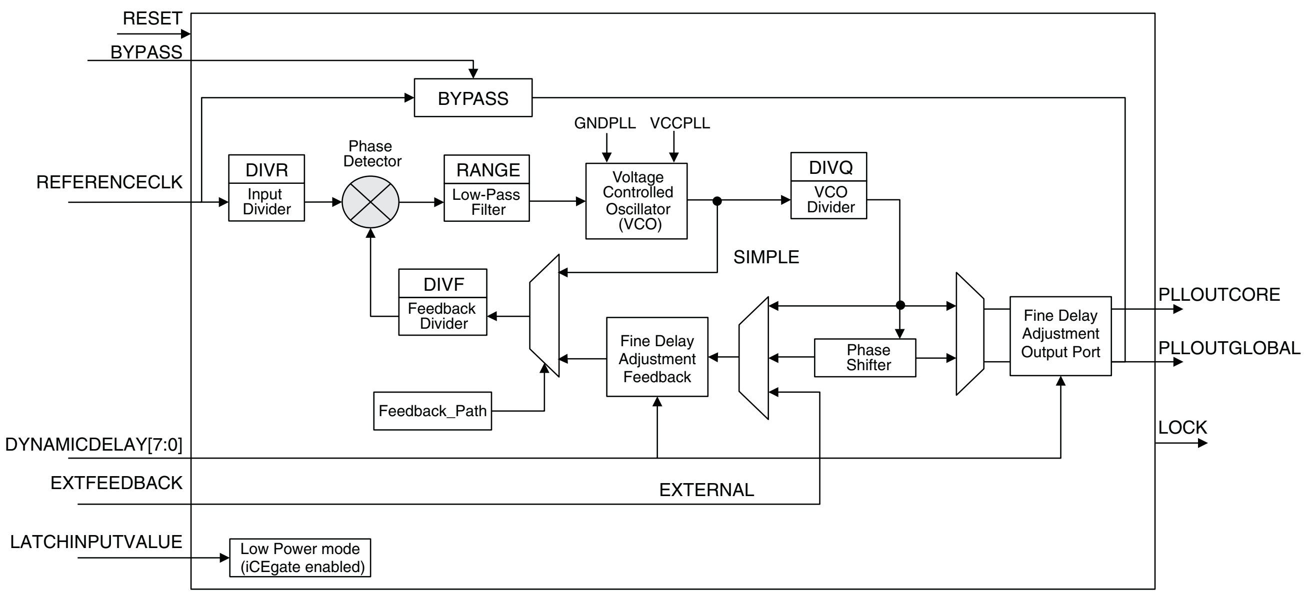


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40LM device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40LM EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

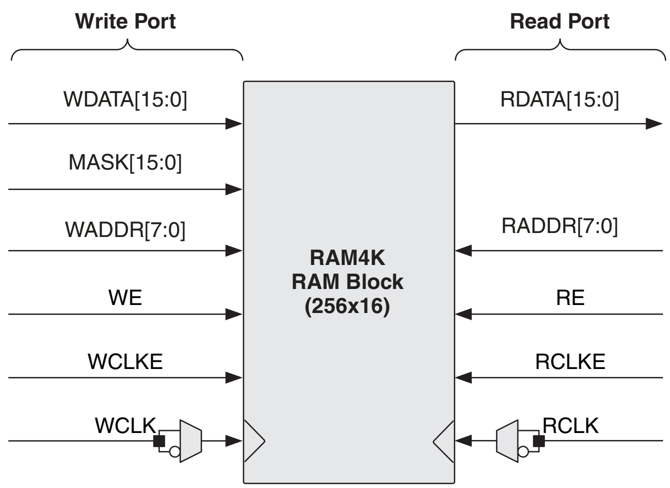


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

The iCE40LM EBR block functions the same as EBR blocks in the iCE40 family. For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

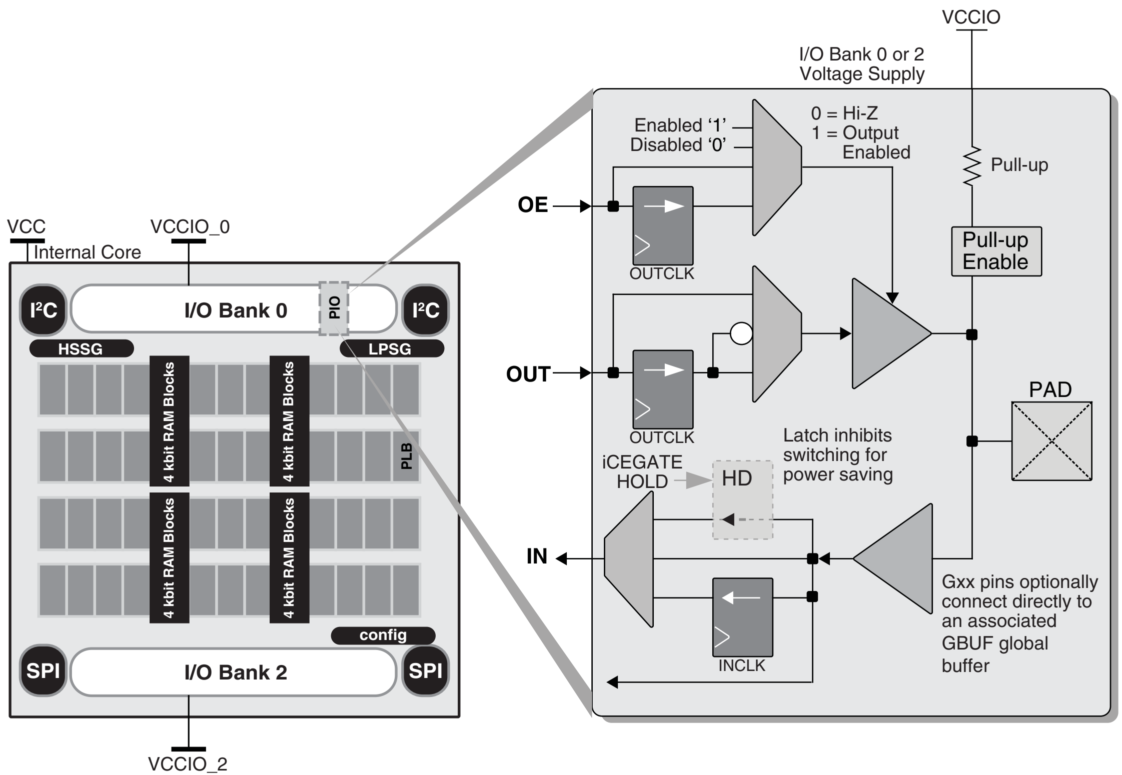
sysIO Buffer Banks

iCE40LM devices have up to two I/O banks with independent V_{CCIO} rails. Configuration bank V_{CC_SPI} for the SPI I/Os is connected to V_{CCIO2} on the 25-pin WLCSP package.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-6 shows the input/output register block for the PIOs.

Figure 2-6. iCE I/O Register Block Diagram

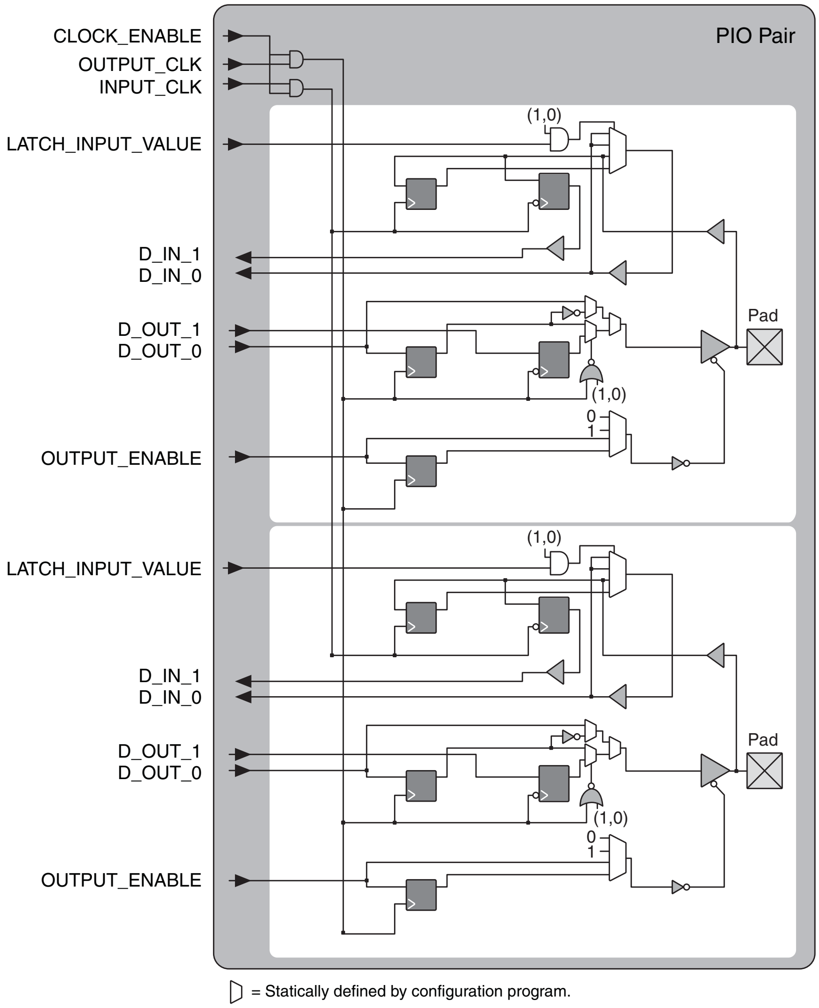


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_0}, V_{CCIO_2} and V_{CC_SPI} (V_{CC_SPI} is connected to V_{CCIO_2} on the 25-pin WLCSP and 36-pin ucBGA packages) reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC} and V_{CCIO_2} reach the defined levels. The I/Os take on the software user-configured settings only after V_{CC_SPI} reaches the level and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40LM sysIO buffer supports all single-ended input and output standards. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40LM devices.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18			Yes

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8

On-Chip Strobe Generators

The iCE40LM devices feature two different Strobe Generators. One is tailored for low-power operation (Low Power Strobe Generator – LPSG), and generates periodic strobes in the Microsecond (µs) ranges. The other is tailored for high speed operation (High Speed Strobe Generator – HSSG), and generates periodic strobes in the Nanosecond (ns) ranges.Add a paragraph:

The Strobe Generators (HSSG and LPSG) provide fixed periodic strobes, and these strobes can be used as a clock source. When used as a clock source, the HSSG can provide strobe frequency in the range of 5 MHz - 20 MHz. The LPSG can provide strobe frequency in the range of 4 kHz - 20 kHz.

For further information on how to use the LPSG and HSSG, please refer to TN1275, iCE40LM On-Chip Strobe Generator Usage Guide.

iCE40LM Configuration

This section describes the programming and configuration of the iCE40LM family.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40LM, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40LM devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-9 describes the function of these features.

Table 2-9. iCE40LM Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40LM Family Data Sheet
DC and Switching Characteristics

March 2016 **Data Sheet DS1045**

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} and V_{CC_SPI} . . . . . –0.5 V to 3.60 V

PLL Power Supply, V_{CCPLL} . . . . . –0.5 V to 1.3 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . . –55 °C to 125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}[4]	PLL Power Supply Voltage		1.14	1.26	V
V_{CC_SPI}[5]	Config SPI port Power Supply Voltage		1.71	3.46	V
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C

1. Like power supplies must be tied together. V_{CCIO_0} to V_{CCIO_2} if they are at same supply voltage and if they meet the power up sequence requirement. Please refer to Power Up Sequence section. V_{CC} and V_{CCPLL} are not recommended to be tied together. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. For 25-pin WLCSP, PLL is not supported.
5. For 25-pin WLCSP and 36-pin ucBGA packages, V_{CC_SPI} is connected to $V_{CCIO\_}2$ on the package. V_{CC_SPI} is used to power the SPI1 ports in both configuration mode and user mode.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power Up Sequence section.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

Typical Building Block Function Performance[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Measured with a toggling pattern.

iCE40LM Family Timing Adders

Over Recommended Commercial Operating Conditions[1, 2, 3]

Buffer Type	Description	Timing (Typ.)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	nS
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	nS
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	nS
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	nS
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	nS
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	nS

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

iCE40LM External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device			Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices		185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	650	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.1	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	450	ps
t_{CO}	Clock to Output - PIO Output Register	All devices	—	11.5	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All devices	–0.23	—	ns
t_H	Clock to Data Hold - PIO Input Register	All devices	5.55	—	ns

1. 25-pin WLCSP package does not support PLL.

sysCLOCK PLL Timing – Preliminary

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} <= 100 MHz	—	450	ps p-p
		f_{OUT} > 100 MHz	—	0.5	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} <= 100 MHz	—	750	ps p-p
		f_{OUT} > 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} <= 25 MHz	—	275	ps p-p
		f_{PFD} > 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	us
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{FDTAP}	Fine Delay adjustment, per Tap		98	226	ps
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	us
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.
6. PLL jitter and lock time measurements are based on an external clean clock source. With different clock source, these values maybe different.

SPI Master Configuration Time[1]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	95	ms
		All devices - Medium frequency	35	ms
		All devices - High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40LM device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	6.5		13	MHz
		Medium Frequency	19.5		38	MHz
		High Frequency	33		66	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs

1. Supported with 1.2 V Vcc and at 25 °C.

Pin Information Summary

Pin Type		iCE40LM-1K			iCE40LM-2K			iCE40LM-4K		
		SWG25	CM36	CM49	SWG25	CM36	CM49	SWG25	CM36	CM49
General Purpose I/O Per Bank	Bank 0	7	15	20	7	15	20	7	15	20
	Bank 2[1]	11	13	17	11	13	17	11	13	17
Total General Purpose I/Os		18	28	37	18	28	37	18	28	37
Vcc		1	1	2	1	1	2	1	1	2
Vccio	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V_{CC_SPI}		0	0	1	0	0	1	0	0	1
V_{CCPLL}		0	1	1	0	1	1	0	1	1
Miscellaneous Dedicated Pins		2	2	2	2	2	2	2	2	2
GND		2	2	4	2	2	4	2	2	4
NC		0	0	0	0	0	0	0	0	0
Reserved		0	0	0	0	0	0	0	0	0
Total Balls		25	36	49	25	36	49	25	36	49
SPI Interfaces	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 2	1	1	1	2	2	2	2	2	2
I^2C Interfaces	Bank 0	1	1	1	2	2	2	2	2	2
	Bank 2	0	0	0	0	0	0	0	0	0

1. Including General Purpose I/Os powered by V_{CC_SPI} and V_{CCPLL}.

iCE40LM Family Data Sheet
Ordering Information

March 2014 | **Data Sheet DS1045**

iCE40LM Part Number Description

iCE40LMXXX - XXXXXXX

Device Family
iCE40LM FPGA

Logic Cells
1K = 1,100 Logic Cells
2K = 2,048 Logic Cells
4K = 3,520 Logic Cells

All parts are shipped in tape-and-reel.

Shipping Method
TR = Tape and Reel
TR1K = Tape and Reel 1,000 units

Package
SWG25 = 25-Ball WLCSP (0.35 mm Ball Pitch)
SWG25TR1K = 25-Ball WLCSP (0.35 mm Ball Pitch) in tape and reel 1,000 units
CM36 = 36-Ball ucBGA (0.4mm Ball Pitch)
CM36TR1K = 36-Ball ucBGA (0.4mm Ball Pitch) in tape and reel 1,000 units
CM49 = 49-Ball ucBGA (0.4mm Ball Pitch)
CM49TR1K = 49-Ball ucBGA (0.4mm Ball Pitch) in tape and reel 1,000 units

Ordering Part Numbers

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
iCE40LM1K-SWG25TR	1100	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM1K-SWG25TR1K	1100	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM1K-CM36TR	1100	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM1K-CM36TR1K	1100	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM1K-CM49TR	1100	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM1K-CM49TR1K	1100	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM2K-SWG25TR	2048	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM2K-SWG25TR1K	2048	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM2K-CM36TR	2048	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM2K-CM36TR1K	2048	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM2K-CM49TR	2048	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM2K-CM49TR1K	2048	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM4K-SWG25TR	3520	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM4K-SWG25TR1K	3520	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM4K-CM36TR	3520	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM4K-CM36TR1K	3520	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM4K-CM49TR	3520	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM4K-CM49TR1K	3520	1.2 V	Halogen-Free ucBGA	49	IND

iCE40LM Family Data Sheet Supplemental Information

January 2014 | Data Sheet DS1045

For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40 I2C and SPI Hardened IP Usage Guide
- TN1275, iCE40LM On-Chip Strobe Generator Usage Guide
- TN1276, Advanced iCE40 I2C and SPI Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- iCE40LM Pinout Files
- iCE40LM Pin Migration Files
- Thermal Management document
- Lattice design tools
- Schematic Symbols