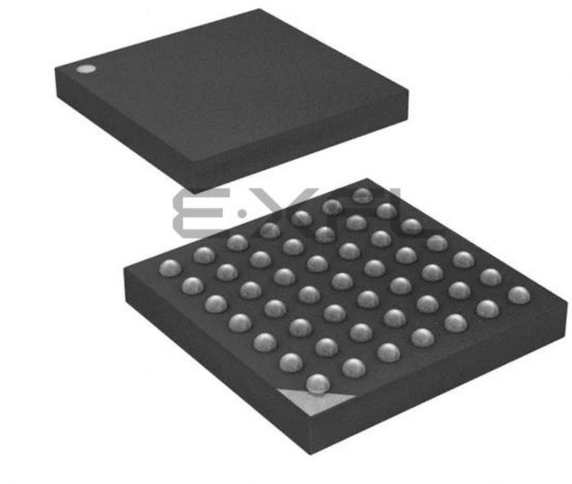
# E·XFL Lattice Semiconductor Corporation - ICE40LM2K-CM49TR1K Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 250 |
| Number of Logic Elements/Cells | 2000 |
| Total RAM Bits | 81920 |
| Number of I/O | 37 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 49-VFBGA |
| Supplier Device Package | 49-UCBGA (3x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm2k-cm49tr1k |

# iCE40LM Family Data Sheet Introduction

January 2014 Data Sheet DS1045

## General Description

iCE40LM family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40LM family includes integrated SPI & I$^2$C blocks to interface with virtually all mobile sensors and application processors. The iCE40LM family also features two Strobe Generators that can generates strobes in Microsecond ranges with the Low-Power Strobe Generator, and also generates strobes in Nanosecond ranges with the High-Speed Strobe Generator.

In addition, the iCE40LM family of devices includes logic to perform other functions such as mobile bridging, antenna tuning, GPIO expansion, motion/gesture recognition, IR remote control, bar code emulation and other custom functions.

The iCE40LM family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I$^2$C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

## Features

- **Flexible Logic Architecture**
  - Three devices with 1100 to 3520 LUTs
  - 18 I/O pins for 25-pin WLCSP
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - As low as 120 µW standby power typical
- **Embedded and Distributed Memory**
  - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I$^2$C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Strobe Generators**
  - Low-Power Strobe Generator (Microsecond ranges)
  - High-Speed Strobe Generator (Nanosecond ranges)
- **High Current Drive Outputs for LED**
  - Three High Drive (HD) output in each device
  - Source/sink nominal 24 mA
- **Flexible On-Chip Clocking**
  - Six low-skew global signal resource
- **Flexible Device Configuration**
  - SRAM is configured through SPI
- **Ultra-Small Form Factor**
  - As small as 25-pin WLCSP package 1.71 mm x 1.71 mm

## Applications

- Smartphones
- Tablets and Consumer Handheld Devices
- Handheld Commercial and Industrial Devices
- Multi Sensor Management Applications
- Sensor Pre-processing & Sensor Fusion
- Always-On Sensor Applications

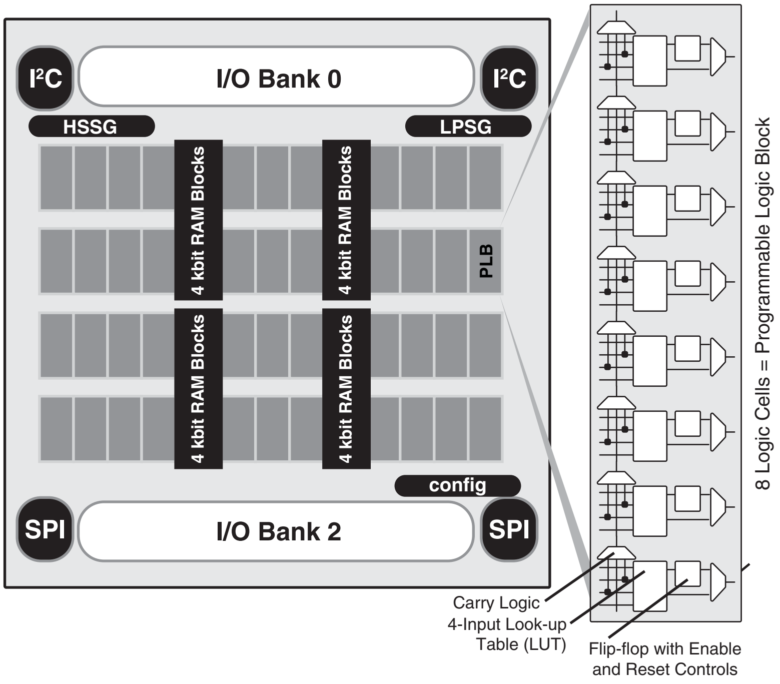
# iCE40LM Family Data Sheet
# Architecture

**March 2016** **Data Sheet DS1045**

## Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I$^2$C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40LM-4K device.

***Figure 2-1. iCE40LM-4K Device, Top View***



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

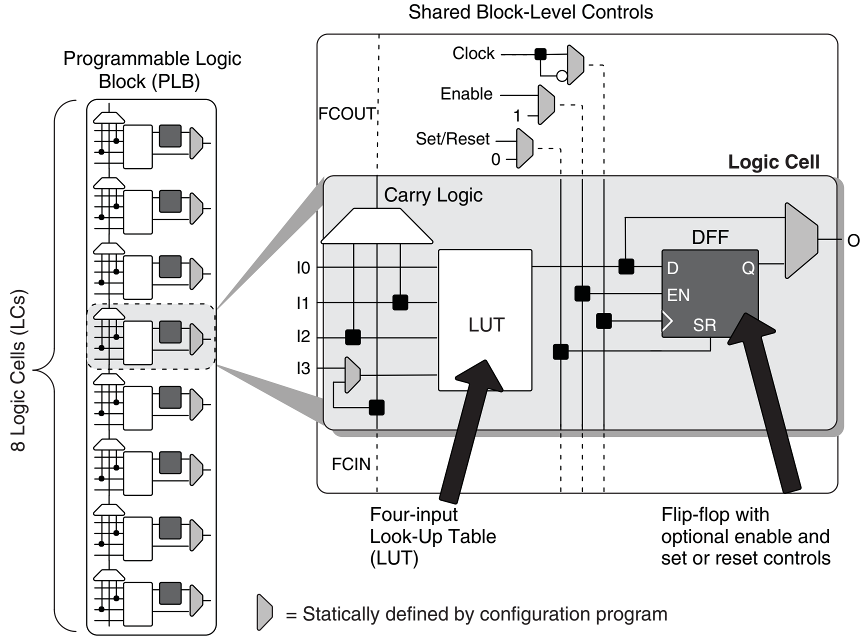
In the iCE40LM family, There are two sysIO banks, one on top and one on bottom. User can connect both $V_{CCIO}$s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40LM also includes two user I$^2$C ports, and two Strobe Generators.

## PLB Blocks

The core of the iCE40LM device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

*Figure 2-2. PLB Block Diagram*



### Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

*Table 2-1. Logic Cell Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | I0, I1, I2, I3 | Inputs to LUT |
| Input | Control signal | Enable | Clock enable shared by all LCs in the PLB |
| Input | Control signal | Set/Reset[1] | Asynchronous or synchronous local set/reset shared by all LCs in the PLB. |
| Input | Control signal | Clock | Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB |
| Input | Inter-PLB signal | FCIN | Fast carry in |
| Output | Data signals | O | LUT or registered output |
| Output | Inter-PFU signal | FCOUT | Fast carry out |

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

## sysCLOCK Phase Locked Loops (PLLs) - *NOT SUPPORTED on the 25-Pin WLCSP*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40LM devices have one sysCLOCK PLL (Please note that the 25-pin WLCSP package does not support the PLL). REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal strobe generator or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

The iCE40LM PLL functions the same as the PLLs in the iCE40 family. For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

***Figure 2-3. PLL Diagram***

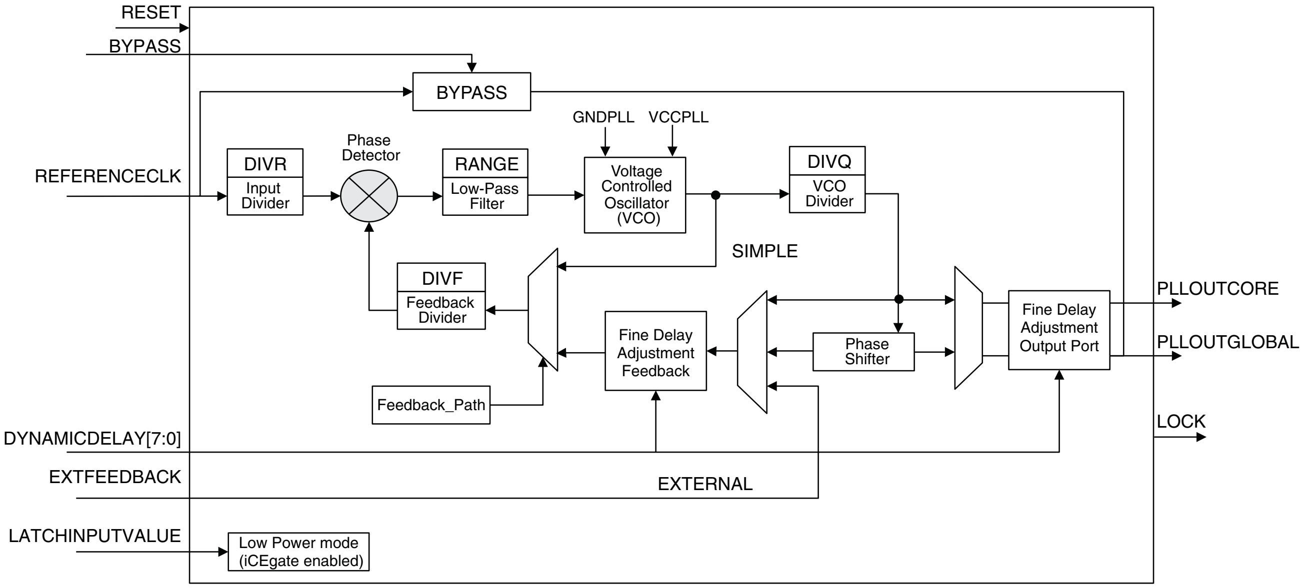


Table 2-3 provides signal descriptions of the PLL block.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

### RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

*Figure 2-4. sysMEM Memory Primitives*

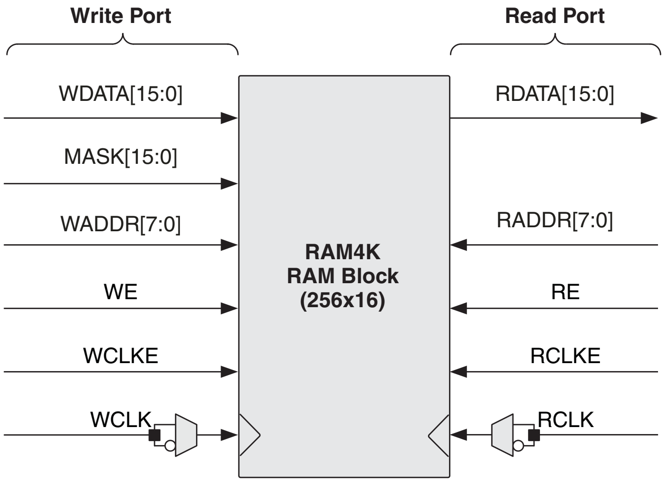


*Table 2-5. EBR Signal Descriptions*

| Signal Name | Direction | Description |
|---|---|---|
| WDATA[15:0] | Input | Write Data input. |
| MASK[15:0] | Input | Masks write operations for individual data bit-lines.<br>0 = write bit; 1 = don’t write bit |
| WADDR[7:0] | Input | Write Address input. Selects one of 256 possible RAM locations. |
| WE | Input | Write Enable input. |
| WCLKE | Input | Write Clock Enable input. |
| WCLK | Input | Write Clock input. Default rising-edge, but with falling-edge option. |
| RDATA[15:0] | Output | Read Data output. |
| RADDR[7:0] | Input | Read Address input. Selects one of 256 possible RAM locations. |
| RE | Input | Read Enable input. |
| RCLKE | Input | Read Clock Enable input. |
| RCLK | Input | Read Clock input. Default rising-edge, but with falling-edge option. |

The iCE40LM EBR block functions the same as EBR blocks in the iCE40 family. For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

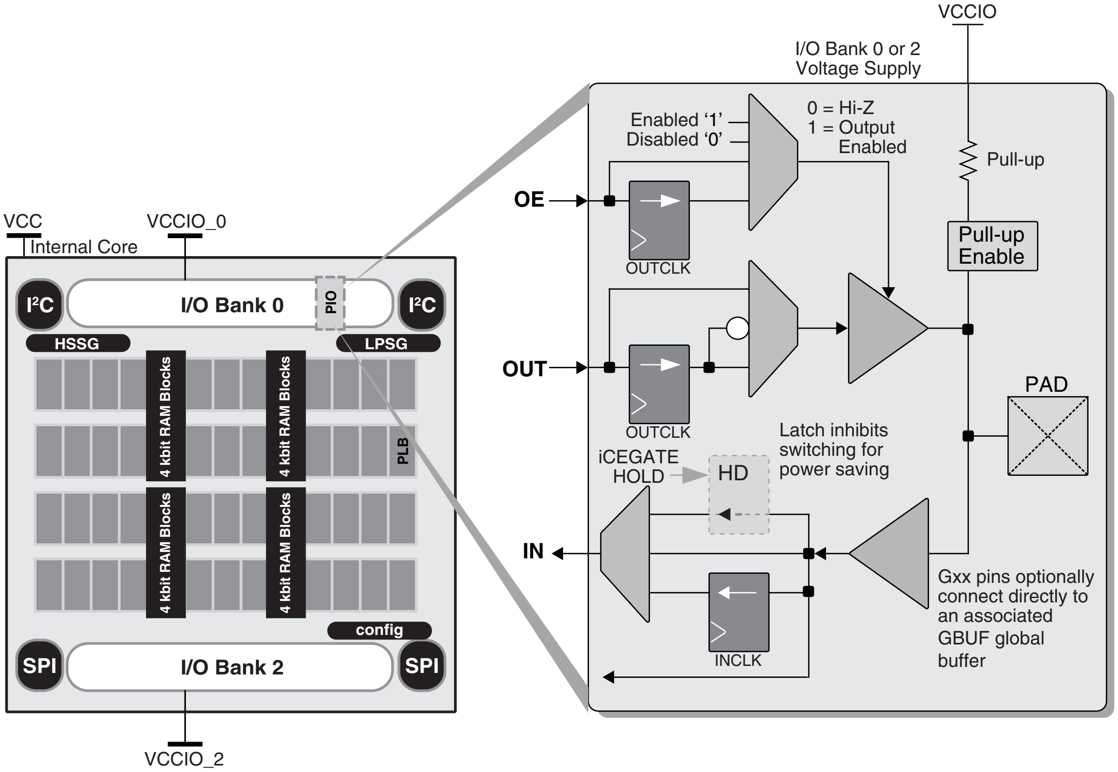
## sysIO Buffer Banks

iCE40LM devices have up to two I/O banks with independent $V_{CCIO}$ rails. Configuration bank $V_{CC\_SPI}$ for the SPI I/Os is connected to $V_{CCIO2}$ on the 25-pin WLCSP package.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

*Figure 2-5. I/O Bank and Programmable I/O Cell*



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-6 shows the input/output register block for the PIOs.

*Figure 2-6. iCE I/O Register Block Diagram*

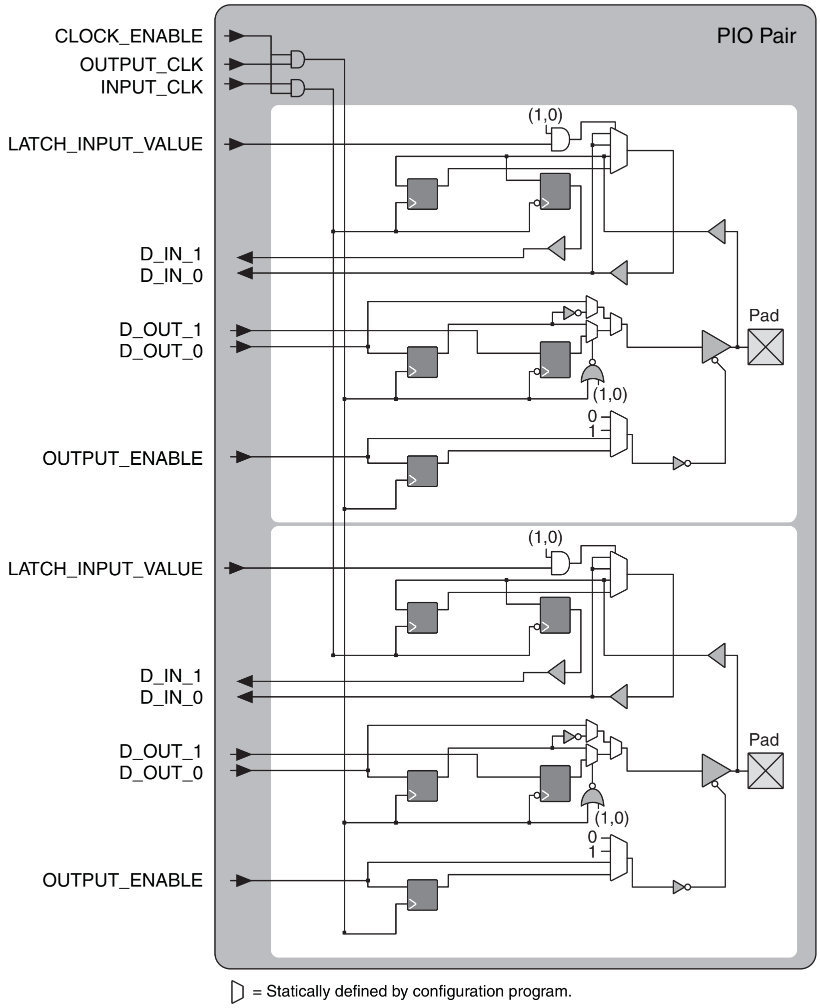


*Table 2-6. PIO Signal List*

| Pin Name | I/O Type | Description |
|---|---|---|
| OUTPUT_CLK | Input | Output register clock |
| CLOCK_ENABLE | Input | Clock enable |
| INPUT_CLK | Input | Input register clock |
| OUTPUT_ENABLE | Input | Output enable |
| D_OUT_0/1 | Input | Data from the core |
| D_IN_0/1 | Output | Data to the core |
| LATCH_INPUT_VALUE | Input | Latches/holds the Input Value |

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today’s systems with LVCMOS interfaces.

## User $I^2C$ IP

The iCE40LM devices have two $I^2C$ IP cores. Either of the two cores can be configured either as an $I^2C$ master or as an $I^2C$ slave. Both $I^2C$ cores have preassigned pins, or user can select different pins, when the core is used.

When the IP core is configured as master, it will be able to control other devices on the $I^2C$ bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an $I^2C$ Master. The $I^2C$ cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support

For further information on the User $I^2C$, please refer to TN1274, iCE40 I2C and SPI Hardened IP Usage Guide.

## User SPI IP

The iCE40LM devices have two SPI IP cores. Both SPI cores have preassigned pins, or user can select different pins, when the SPI core is used. Both SPI IP core can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, iCE40 I2C and SPI Hardened IP Usage Guide.

## High Drive I/O Pins

The iCE40LM family devices offer 3 High Drive (HD) outputs in each device in the family. The HD outputs are ideal to drive LED signals on mobile application.

These HD outputs can be driven in different drive modes. The default is standard drive, which source/sink 8mA current nominally. When HD drive option is selected, these HD outputs can source/sink 24mA current nominally.

The pins on the HD I/Os are labeled with HD in it.

## Power On Reset

iCE40LM devices have power-on reset circuitry to monitor $V_{CC}$, $V_{CCIO\_0}$, $V_{CCIO\_2}$ and $V_{CC\_SPI}$ voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers download from the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

# iCE40LM Configuration

This section describes the programming and configuration of the iCE40LM family.

### Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40LM, please see TN1248, iCE40 Programming and Configuration.

## Power Saving Options

The iCE40LM devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-9 describes the function of these features.

***Table 2-9. iCE40LM Power Saving Features Description***

| Device Subsystem | Feature Description |
|---|---|
| PLL | When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value. |
| iCEGate | To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. |

# iCE40LM Family Data Sheet
# DC and Switching Characteristics

**March 2016** **Data Sheet DS1045**

## Absolute Maximum Ratings[1, 2, 3]

| | |
|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.42 V |
| Output Supply Voltage $V_{CCIO}$ and $V_{CC\_SPI}$ | –0.5 V to 3.60 V |
| PLL Power Supply, $V_{CCPLL}$ | –0.5 V to 1.3 V |
| I/O Tri-state Voltage Applied | –0.5 V to 3.60 V |
| Dedicated Input Voltage Applied | –0.5 V to 3.60 V |
| Storage Temperature (Ambient) | –65 °C to 150 °C |
| Junction Temperature ($T_J$) | –55 °C to 125°C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

## Recommended Operating Conditions[1]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$[1] | Core Supply Voltage | | 1.14 | 1.26 | V |
| $V_{CCIO}$[1, 2, 3] | I/O Driver Supply Voltage | $V_{CCIO\_0}$, $V_{CCIO\_2}$ | 1.71 | 3.46 | V |
| $V_{CCPLL}$[4] | PLL Power Supply Voltage | | 1.14 | 1.26 | V |
| $V_{CC\_SPI}$[5] | Config SPI port Power Supply Voltage | | 1.71 | 3.46 | V |
| $t_{JIND}$ | Junction Temperature Industrial Operation | | –40 | 100 | °C |

1. Like power supplies must be tied together. $V_{CCIO\_0}$ to $V_{CCIO\_2}$ if they are at same supply voltage and if they meet the power up sequence requirement. Please refer to Power Up Sequence section. $V_{CC}$ and $V_{CCPLL}$ are not recommended to be tied together. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.
4. For 25-pin WLCSP, PLL is not supported.
5. For 25-pin WLCSP and 36-pin ucBGA packages, $V_{CC\_SPI}$ is connected to $V_{CCIO_}$2 on the package. $V_{CC\_SPI}$ is used to power the SPI1 ports in both configuration mode and user mode.

## Power Supply Ramp Rates[1, 2]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | 0.01 | 10 | V/ms |

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power Up Sequence section.

## Supply Current [1, 2, 3, 4]

| Symbol | Parameter | Typ. VCC[4] | Units |
|---|---|---|---|
| $I_{CCSTDBY}$ | Core Power Supply Static Current | 100 | uA |
| $I_{CCPLLSTDBY}$ | PLL Power Supply Static Current | 11 | uA |
| $I_{CCIOSTDBY}$, $I_{CC\_SPISTDBY}$ | $V_{CCIO}$, $V_{CC\_SPI}$ Power Supply Static Current | 2.5 | uA |
| $I_{CCPEAK}$ | Core Power Supply Startup Peak Current | 11.2 | mA |
| $I_{CCPLLPEAK}$ | PLL Power Supply Startup Peak Current | 2.8 | mA |
| $I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$ | $V_{CCIO}$, $V_{CC\_SPI}$ Power Supply Startup Peak Current | 21.4 | mA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. For 25-pin WLCSP, $V_{CCPLL}$ is tied internally on the package, and $V_{CC\_SPI}$ is also connected to $V_{CCIO\_}2$ on the package.

## User I$^2$C Specifications

| Parameter Symbol | Parameter Description | spec (STD Mode) | | | spec (FAST Mode) | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{SCL}$ | Maximum SCL clock frequency | — | — | 100 | — | — | 400 | kHz |
| $t_{HI}$ | SCL clock HIGH Time | 4 | — | — | 0.6 | — | — | µs |
| $t_{LO}$ | SCL clock LOW Time | 4.7 | — | — | 1.3 | — | — | µs |
| $t_{SU,DAT}$ | Setup time (DATA) | 250 | — | — | 100 | — | — | ns |
| $t_{HD,DAT}$ | Hold time (DATA) | 0 | — | — | 0 | — | — | ns |
| $t_{SU,STA}$ | Setup time (START condition) | 4.7 | — | — | 0.6 | — | — | µs |
| $t_{HD,STA}$ | Hold time (START condition) | 4 | — | — | 0.6 | — | — | µs |
| $t_{SU,STO}$ | Setup time (STOP condition) | 4 | — | — | 0.6 | — | — | µs |
| $t_{BUF}$ | Bus free time between STOP and START | 4.7 | — | — | 1.3 | — | — | µs |
| $t_{CO,DAT}$ | SCL LOW to DATAOUT valid | — | — | 3.4 | — | — | 0.9 | µs |

## User SPI Specifications

| Parameter Symbol | Parameter Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCK clock frequency | — | — | 45 | MHz |
| $t_{HI}$ | HIGH period of SCK clock | 9 | — | — | ns |
| $t_{LO}$ | LOW period of SCK clock | 9 | — | — | ns |
| $t_{SUmaster}$ | Setup time (master mode) | 2 | — | — | ns |
| $t_{HOLDmaster}$ | Hold time (master mode) | 5 | — | — | ns |
| $t_{SUslave}$ | Setup time (slave mode) | 2 | — | — | ns |
| $t_{HOLDslave}$ | Hold time (slave mode) | 5 | — | — | ns |
| $t_{SCK2OUT}$ | SCK to out (slave mode) | — | — | 13.5 | ns |

# iCE40LM External Switching Characteristics

### Over Recommended Commercial Operating Conditions

| Parameter | Description | Device |  |  | Units |
|---|---|---|---|---|---|
| **Clocks** |  |  |  |  |  |
| **Global Clocks** |  |  |  |  |  |
| $f_{MAX\_GBUF}$ | Frequency for Global Buffer Clock network | All devices |  | 185 | MHz |
| $t_{W\_GBUF}$ | Clock Pulse Width for Global Buffer | All devices | 2 | — | ns |
| $t_{SKEW\_GBUF}$ | Global Buffer Clock Skew Within a Device | All devices | — | 650 | ps |
| **Pin-LUT-Pin Propagation Delay** |  |  |  |  |  |
| $t_{PD}$ | Best case propagation delay through one LUT logic | All devices | — | 9.1 | ns |
| **General I/O Pin Parameters (Using Global Buffer Clock without PLL)**[1] |  |  |  |  |  |
| $t_{SKEW\_IO}$ | Data bus skew across a bank of IOs | All devices | — | 450 | ps |
| $t_{CO}$ | Clock to Output - PIO Output Register | All devices | — | 11.5 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | All devices | –0.23 | — | ns |
| $t_H$ | Clock to Data Hold - PIO Input Register | All devices | 5.55 | — | ns |

1. 25-pin WLCSP package does not support PLL.

## SPI Master Configuration Time[1]

| Symbol | Parameter | Conditions | Max. | Units |
|---|---|---|---|---|
| $t_{CONFIG}$ | POR/CRESET_B to Device I/O Active | All devices - Low Frequency (Default) | 95 | ms |
| | | All devices - Medium frequency | 35 | ms |
| | | All devices - High frequency | 18 | ms |

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

## sysCONFIG Port Timing Specifications

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **All Configuration Modes** | | | | | | |
| $t_{CRESET\_B}$ | Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge | | 200 | — | — | ns |
| $t_{DONE\_IO}$ | Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated | | 49 | — | — | Cycles |
| **Slave SPI** | | | | | | |
| $t_{CR\_SCK}$ | Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40LM device is clearing its internal configuration memory | | 1200 | — | — | µs |
| $f_{MAX}$ | CCLK clock frequency | Write | 1 | — | 25 | MHz |
| | | Read[1] | — | 15 | — | MHz |
| $t_{CCLKH}$ | CCLK clock pulsewidth HIGH | | 20 | — | — | ns |
| $t_{CCLKL}$ | CCLK clock pulsewidth LOW | | 20 | — | — | ns |
| $t_{STSU}$ | CCLK setup time | | 12 | — | — | ns |
| $t_{STH}$ | CCLK hold time | | 12 | — | — | ns |
| $t_{STCO}$ | CCLK falling edge to valid output | | 13 | — | — | ns |
| **Master SPI** | | | | | | |
| $f_{MCLK}$ | MCLK clock frequency | Low Frequency (Default) | 6.5 | | 13 | MHz |
| | | Medium Frequency | 19.5 | | 38 | MHz |
| | | High Frequency | 33 | | 66 | MHz |
| $t_{MCLK}$ | CRESET_B HIGH to first MCLK edge | | 1200 | — | — | µs |

1. Supported with 1.2 V Vcc and at 25 °C.

## Switching Test Conditions

Figure 3-1 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

*Figure 3-1. Output Test Load, LVCMOS Standards*

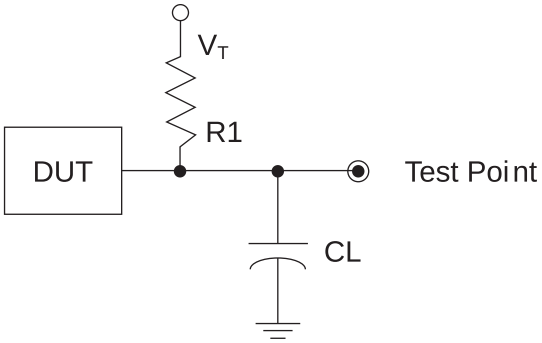


*Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces*

| Test Condition | $R_1$ | $C_L$ | Timing Reference | $V_T$ |
|---|---|---|---|---|
| LVCMOS settings (L -> H, H -> L) | ∞ | 0 pF | LVCMOS 3.3 = 1.5 V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| LVCMOS 3.3 (Z -> H) | 188 | 0 pF | 1.5 | $V_{OL}$ |
| LVCMOS 3.3 (Z -> L) | | | 1.5 | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVCMOS (H -> Z) | | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVCMOS (L -> Z) | | | $V_{OL}$ - 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

# iCE40LM Family Data Sheet
# Pinout Information

**March 2016** **Data Sheet DS1045**

## Signal Descriptions

| Signal Name | | Function | I/O | Description |
|---|---|---|---|---|
| **Power Supplies** | | | | |
| $V_{CC}$ | | Power | — | Core Power Supply |
| $V_{CCIO\_0}$,<br>$V_{CCIO\_2}$ | | Power | — | Power for I/Os in Bank 0 and 2. |
| $V_{CC\_SPI}$ | | Power | — | Power supply for SPI1 ports. For 25-pin WLCSP and 36-pin ucBGA packages, this signal is connected to $V_{CCIO\_2}$. |
| $V_{CCPLL}$ | | Power | — | Power supply for PLL. For 25-pin WLCSP, this is connected internally to $V_{CC}$. |
| GND/GNDPLL | | GROUND | — | Ground |
| **Configuration** | | | | |
| CRESETB | | Configuration | I | Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to $V_{CCIO\_2}$. |
| CDONE | | Configuration | I/O | Configuration Done. Includes a weak pull-up resistor to $V_{CCIO\_2}$. |
| **Config SPI** | | | | |
| Primary | Secondary | | | |
| PIOB_xx[HD] | SPI_SCK | Configuration | I/O | This pin is shared with device configuration. During configuration:<br>In Master SPI mode, this pin outputs the clock to external SPI memory.<br>In Slave SPI mode, this pin inputs the clock from external processor. |
| | | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O. |
| PIOB_xx[HD] | SPI_SDO | Configuration | Output | This pin is shared with device configuration. During configuration:<br>In Master SPI mode, this pin outputs the command data to external SPI memory.<br>In Slave SPI mode, this pin connects to the MISO pin of the external processor. |
| | | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O. |
| PIOB_xx[HD] | SPI_SI | Configuration | Input | This pin is shared with device configuration. During configuration:<br>In Master SPI mode, this pin receives data from external SPI memory.<br>In Slave SPI mode, this pin connects to the MOSI pin of the external processor. |
| | | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O. |

| Signal Name | | Function | I/O | Description |
|---|---|---|---|---|
| PIOB_xx[HD] | SPI_SS_B | Configuration | I/O | This pin is shared with device configuration. During configuration:<br>In Master SPI mode, this pin outputs to the external SPI memory.<br>In Slave SPI mode, this pin inputs from the external processor. |
| | | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O. |
| **Global Signals** | | | | |
| Primary | Secondary | | | |
| PIOT_xx | G0 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer. |
| PIOT_xx | G1 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer. |
| PIOT_xx | G3 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer. |
| PIOT_xx | G4 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer. |
| PIOT_xx | G5 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer. |
| PIOB_xx | G6 | General I/O | I/O | In user mode, after configuration, this pin can be programmed as general I/O in user function. |
| | | Global | Input | Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer. |
| **LED Signals** | | | | |
| PIOT_xx | | General I/O | I/O | In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location). |
| PIOB_xx | | General I/O | I/O | In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location) [HD]=High Drive I/O. |

## Pin Information Summary

| Pin Type | | iCE40LM-1K | | | iCE40LM-2K | | | iCE40LM-4K | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | **SWG25** | **CM36** | **CM49** | **SWG25** | **CM36** | **CM49** | **SWG25** | **CM36** | **CM49** |
| General Purpose I/O Per Bank | Bank 0 | 7 | 15 | 20 | 7 | 15 | 20 | 7 | 15 | 20 |
| | Bank 2[1] | 11 | 13 | 17 | 11 | 13 | 17 | 11 | 13 | 17 |
| Total General Purpose I/Os | | 18 | 28 | 37 | 18 | 28 | 37 | 18 | 28 | 37 |
| Vcc | | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 |
| Vccio | Bank 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CC\_SPI}$ | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| $V_{CCPLL}$ | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| Miscellaneous Dedicated Pins | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GND | | 2 | 2 | 4 | 2 | 2 | 4 | 2 | 2 | 4 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reserved | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Balls | | 25 | 36 | 49 | 25 | 36 | 49 | 25 | 36 | 49 |
| SPI Interfaces | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| $I^2C$ Interfaces | Bank 0 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Including General Purpose I/Os powered by $V_{CC\_SPI}$ and $V_{CCPLL}$.

# iCE40LM Family Data Sheet
# Ordering Information

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## iCE40LM Part Number Description

iCE40LMXXX - XXXXXXX

**Device Family**
iCE40LM FPGA

**Logic Cells**
1K = 1,100 Logic Cells
2K = 2,048 Logic Cells
4K = 3,520 Logic Cells

All parts are shipped in tape-and-reel.

**Shipping Method**
TR = Tape and Reel
TR1K = Tape and Reel 1,000 units

**Package**
SWG25 = 25-Ball WLCSP (0.35 mm Ball Pitch)
SWG25TR1K = 25-Ball WLCSP (0.35 mm Ball Pitch) in tape and reel 1,000 units
CM36 = 36-Ball ucBGA (0.4mm Ball Pitch)
CM36TR1K = 36-Ball ucBGA (0.4mm Ball Pitch) in tape and reel 1,000 units
CM49 = 49-Ball ucBGA (0.4mm Ball Pitch)
CM49TR1K = 49-Ball ucBGA (0.4mm Ball Pitch) in tape and reel 1,000 units

## Ordering Part Numbers

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| iCE40LM1K-SWG25TR | 1100 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM1K-SWG25TR1K | 1100 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM1K-CM36TR | 1100 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM1K-CM36TR1K | 1100 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM1K-CM49TR | 1100 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| iCE40LM1K-CM49TR1K | 1100 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| iCE40LM2K-SWG25TR | 2048 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM2K-SWG25TR1K | 2048 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM2K-CM36TR | 2048 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM2K-CM36TR1K | 2048 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM2K-CM49TR | 2048 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| iCE40LM2K-CM49TR1K | 2048 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| iCE40LM4K-SWG25TR | 3520 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM4K-SWG25TR1K | 3520 | 1.2 V | Halogen-Free caBGA | 25 | IND |
| iCE40LM4K-CM36TR | 3520 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM4K-CM36TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| iCE40LM4K-CM49TR | 3520 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| iCE40LM4K-CM49TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 49 | IND |

# iCE40LM Family Data Sheet Supplemental Information

January 2014 **Data Sheet DS1045**

## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40 I2C and SPI Hardened IP Usage Guide
- TN1275, iCE40LM On-Chip Strobe Generator Usage Guide
- TN1276, Advanced iCE40 I2C and SPI Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- iCE40LM Pinout Files
- iCE40LM Pin Migration Files
- Thermal Management document
- Lattice design tools
- Schematic Symbols

# iCE40LM Family Data Sheet Revision History

**March 2016** **Data Sheet DS1045**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2016 | 1.6 | Architecture | Updated Typical I/O Behavior During Power-up section. Indicated 36-pin ucBGA in package in description. |
| | | DC and Switching Characteristics | Updated Recommended Operating Conditions1 section. Revised footnote 5. |
| | | Pinout Information | Updated Signal Descriptions section. General update of signal names and descriptions. |
| March 2015 | 1.5 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 $V_{OH}$ Min. (V) from 0.5 to 0.4. |
| August 2014 | 1.4 | DC and Switching Characteristics | Updated the Recommended Operating Conditions section. Added $V_{CC}$ and $V_{CCPLL}$ information to footnote 1. |
| | | | Updated Power Up Sequence section.Revised and added information on required power up sequence. |
| March 2014 | 1.3 | Ordering Information | Updated Ordering Part Numbers section. Changed packages from csBGA to ucBGA. |
| | 01.2 | Architecture | Updated Typical I/O Behavior During Power-up section. Added $V_{CCIO\_0}$ to the first statement. |
| | | | Updated Power On Reset section. Added $V_{CCIO\_0}$ to the first statement. |
| | | Ordering Information | Updated iCE40LM Part Number Description section. Added shipping method and packages. |
| | | | Added part numbers in Ordering Part Numbers section. |
| January 2014 | 01.1 | All | Updated document status from Advance. |
| | | Introduction | Updated device features. |
| | | DC and Switching Characteristics | Updated the following tables:<br>— sysCLOCK PLL Timing – Preliminary<br>— Supply Current<br>— sysCONFIG Port Timing Specifications. |
| | | Pinout Information | Updated SPI and Config SPI Ports information in Signal Descriptions table. |
| October 2013 | 01.0 | All | General updates for product launch. |
| | | Pinout Information | Updated ball map to 25-pin WLCSP. |
| September 2013 | 00.2 EAP | All | General updates to all sections. |
| August 2013 | 00.1 EAP | All | Initial release. |