Lattice Semiconductor Corporation - ICE40LM2K-SWG25TR1K Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	250
Number of Logic Elements/Cells	2000
Total RAM Bits	81920
Number of I/O	18
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	25-XFBGA, WLCSP
Supplier Device Package	25-WLCSP (1.7x1.7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm2k-swg25tr1k

iCE40LM Family Data Sheet Introduction

January 2014 Data Sheet DS1045

General Description

iCE40LM family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40LM family includes integrated SPI & I^2C blocks to interface with virtually all mobile sensors and application processors. The iCE40LM family also features two Strobe Generators that can generates strobes in Microsecond ranges with the Low-Power Strobe Generator, and also generates strobes in Nanosecond ranges with the High-Speed Strobe Generator.

In addition, the iCE40LM family of devices includes logic to perform other functions such as mobile bridging, antenna tuning, GPIO expansion, motion/gesture recognition, IR remote control, bar code emulation and other custom functions.

The iCE40LM family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
  - Three devices with 1100 to 3520 LUTs
  - 18 I/O pins for 25-pin WLCSP
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - As low as 120 µW standby power typical
- **Embedded and Distributed Memory**
  - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I^2C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Strobe Generators**
  - Low-Power Strobe Generator (Microsecond ranges)
  - High-Speed Strobe Generator (Nanosecond ranges)
- **High Current Drive Outputs for LED**
  - Three High Drive (HD) output in each device
  - Source/sink nominal 24 mA
- **Flexible On-Chip Clocking**
  - Six low-skew global signal resource
- **Flexible Device Configuration**
  - SRAM is configured through SPI
- **Ultra-Small Form Factor**
  - As small as 25-pin WLCSP package 1.71 mm x 1.71 mm

Applications

- Smartphones
- Tablets and Consumer Handheld Devices
- Handheld Commercial and Industrial Devices
- Multi Sensor Management Applications
- Sensor Pre-processing & Sensor Fusion
- Always-On Sensor Applications

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Table 1-1. iCE40LM Family Selection Guide

Part Number	iCE40LM1K	iCE40LM2K	iCE40LM4K
Logic Cells (LUT + Flip-Flop)	1100	2048	3520
RAM4K Memory Blocks	16	20	20
RAM4K RAM Bits	64K	80K	80K
Package	Programmable I/O Count		
25-pin WLCSP, 1.71 mm x 1.71 mm, 0.35 mm	18	18	18
36-pin ucBGA, 2.5 mm x 2.5 mm, 0.40 mm	28	28	28
49-pin ucBGA, 3 mm x 3 mm, 0.40 mm	37	37	37

Introduction

The iCE40LM family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), two Strobe Generators (LPSG, HSSG), two hardened I^2C Controllers and two hardened SPI Controllers. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40LM devices are fabricated on a 40nm CMOS low power process. The device architecture has several features such as user configurable I^2C and SPI Controllers, either as master or slave, and two Strobe Generators.

The iCE40LM FPGAs are available in very small form factor packages, with the smallest in 25-pin WLCSP. The 25-pin WLCSP package has a 0.35 mm ball pitch, resulting to an overall package size of 1.71 mm x 1.71 mm that easily fits into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40LM devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40LM family of devices. Popular logic synthesis tools provide synthesis library support for iCE40LM. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40LM device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40LM FPGA family. Lattice also can provide fully verified bit-stream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's Reference Designs or fully-verified bitstreams, please contact your local Lattice representative.

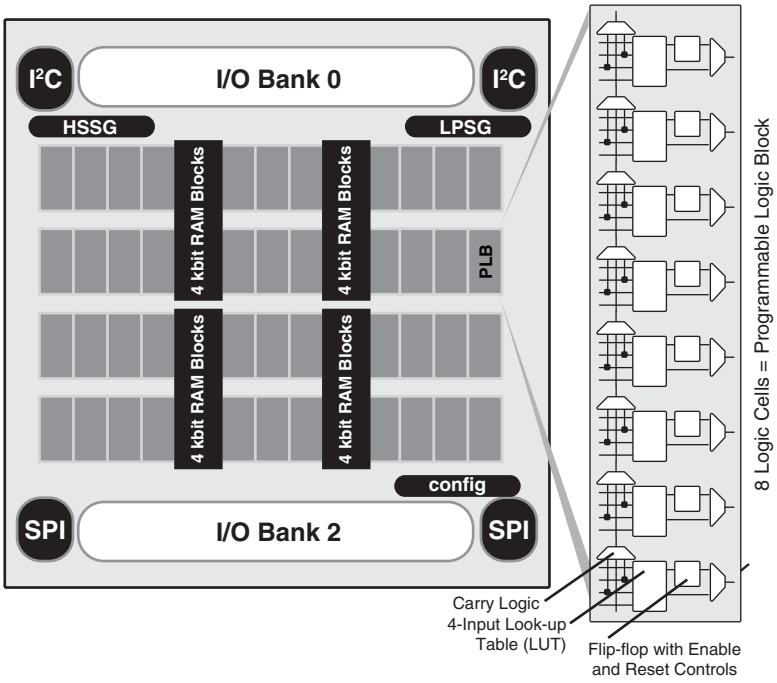
iCE40LM Family Data Sheet Architecture

March 2016 Data Sheet DS1045

Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40LM-4K device.

Figure 2-1. iCE40LM-4K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40LM family, There are two sysIO banks, one on top and one on bottom. User can connect both V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40LM also includes two user I²C ports, and two Strobe Generators.

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