Infineon Technologies - CY9AF316NAPMC-G-MNE2 Datasheet

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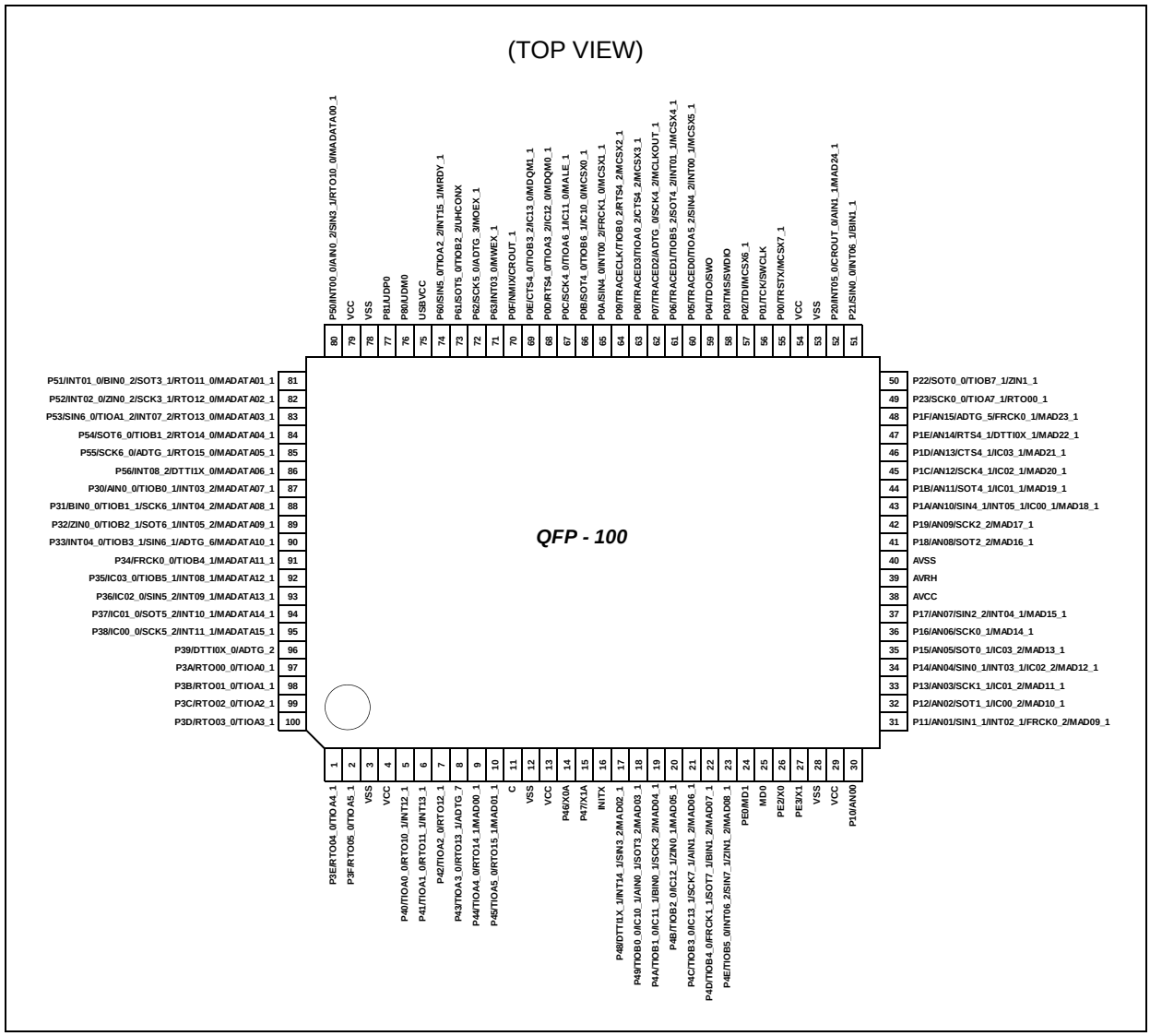
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy9af316napmc-g-mne2

・ FPT-100P-M06



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ SIGNAL DESCRIPTION

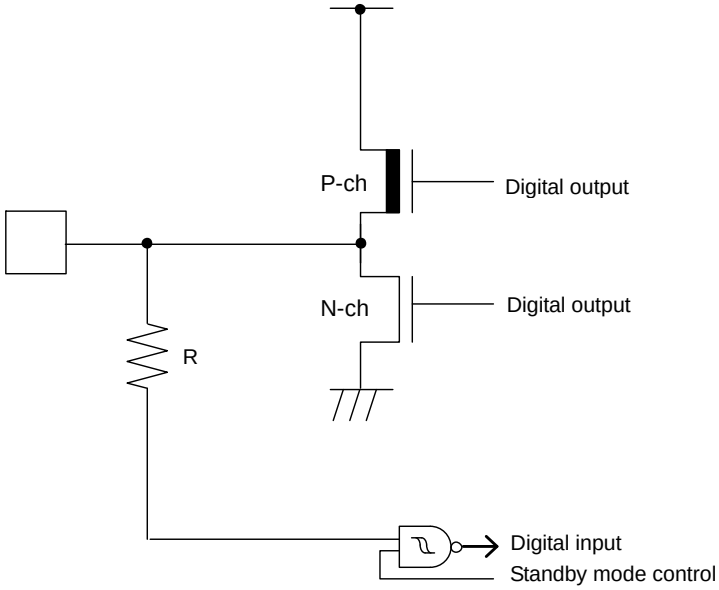
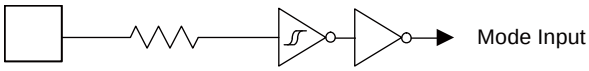
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	-
	ADTG_1		7	85	D3	7	-
	ADTG_2		18	96	F4	13	9
	ADTG_3		94	72	C5	74	58
	ADTG_4		-	-	-	-	-
	ADTG_5		70	48	D11	-	-
	ADTG_6		12	90	E4	12	8
	ADTG_7		30	8	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin ANxx describes ADC ch.xx.	52	30	J11	42	34
	AN01		53	31	J10	43	35
	AN02		54	32	J8	44	36
	AN03		55	33	H10	45	37
	AN04		56	34	H9	46	38
	AN05		57	35	H7	47	39
	AN06		58	36	G10	48	-
	AN07		59	37	G9	49	40
	AN08		63	41	G8	53	44
	AN09		64	42	F10	54	45
	AN10		65	43	F9	55	-
	AN11		66	44	E11	56	-
	AN12		67	45	E10	-	-
	AN13		68	46	F8	-	-
	AN14		69	47	E9	-	-
	AN15		70	48	D11	-	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-
	TIOA0_1		19	97	G3	14	10
	TIOA0_2		85	63	B7	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	22
	TIOB0_1		9	87	E1	9	5
	TIOB0_2		86	64	C7	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-
	TIOA1_1		20	98	H1	15	11
	TIOA1_2		5	83	D1	5	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	23
	TIOB1_1		10	88	E2	10	6
	TIOB1_2		6	84	D2	6	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	7	K5	-	-
	TIOA2_1		21	99	H2	16	12
	TIOA2_2		96	74	C4	76	60
	TIOB2_0	Base timer ch.2 TIOB pin	42	20	K7	32	24
	TIOB2_1		11	89	E3	11	7
	TIOB2_2		95	73	B4	75	59

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Debugger	SWCLK	Serial wire debug interface clock input	78	56	B9	62	50
	SWDIO	Serial wire debug interface data input / output	80	58	A8	64	52
	SWO	Serial wire viewer output	81	59	B8	65	53
	TCK	J-TAG test clock input	78	56	B9	62	50
	TDI	J-TAG test data input	79	57	B11	63	51
	TDO	J-TAG debug data output	81	59	B8	65	53
	TMS	J-TAG test mode state input/output	80	58	A8	64	52
	TRACECLK	Trace CLK output of ETM	86	64	C7	-	-
	TRACED0	Trace data output of ETM	82	60	C8	-	-
	TRACED1		83	61	D9	-	-
	TRACED2		84	62	A7	-	-
	TRACED3		85	63	B7	-	-
	TRSTX	J-TAG test reset Input	77	55	A9	61	49
External Bus	MAD00_1	External bus interface address bus	31	9	H5	21	-
	MAD01_1		32	10	L6	22	-
	MAD02_1		39	17	K6	29	-
	MAD03_1		40	18	J6	30	-
	MAD04_1		41	19	L7	31	-
	MAD05_1		42	20	K7	32	-
	MAD06_1		43	21	H6	33	-
	MAD07_1		44	22	J7	34	-
	MAD08_1		45	23	K8	35	-
	MAD09_1		53	31	J10	43	-
	MAD10_1		54	32	J8	44	-
	MAD11_1		55	33	H10	45	-
	MAD12_1		56	34	H9	46	-
	MAD13_1		57	35	H7	47	-
	MAD14_1		58	36	G10	48	-
	MAD15_1		59	37	G9	49	-
	MAD16_1		63	41	G8	53	-
	MAD17_1		64	42	F10	54	-
	MAD18_1		65	43	F9	55	-
	MAD19_1		66	44	E11	56	-
	MAD20_1		67	45	E10	-	-
	MAD21_1		68	46	F8	-	-
	MAD22_1		69	47	E9	-	-
	MAD23_1		70	48	D11	-	-
	MAD24_1		74	52	C10	60	-

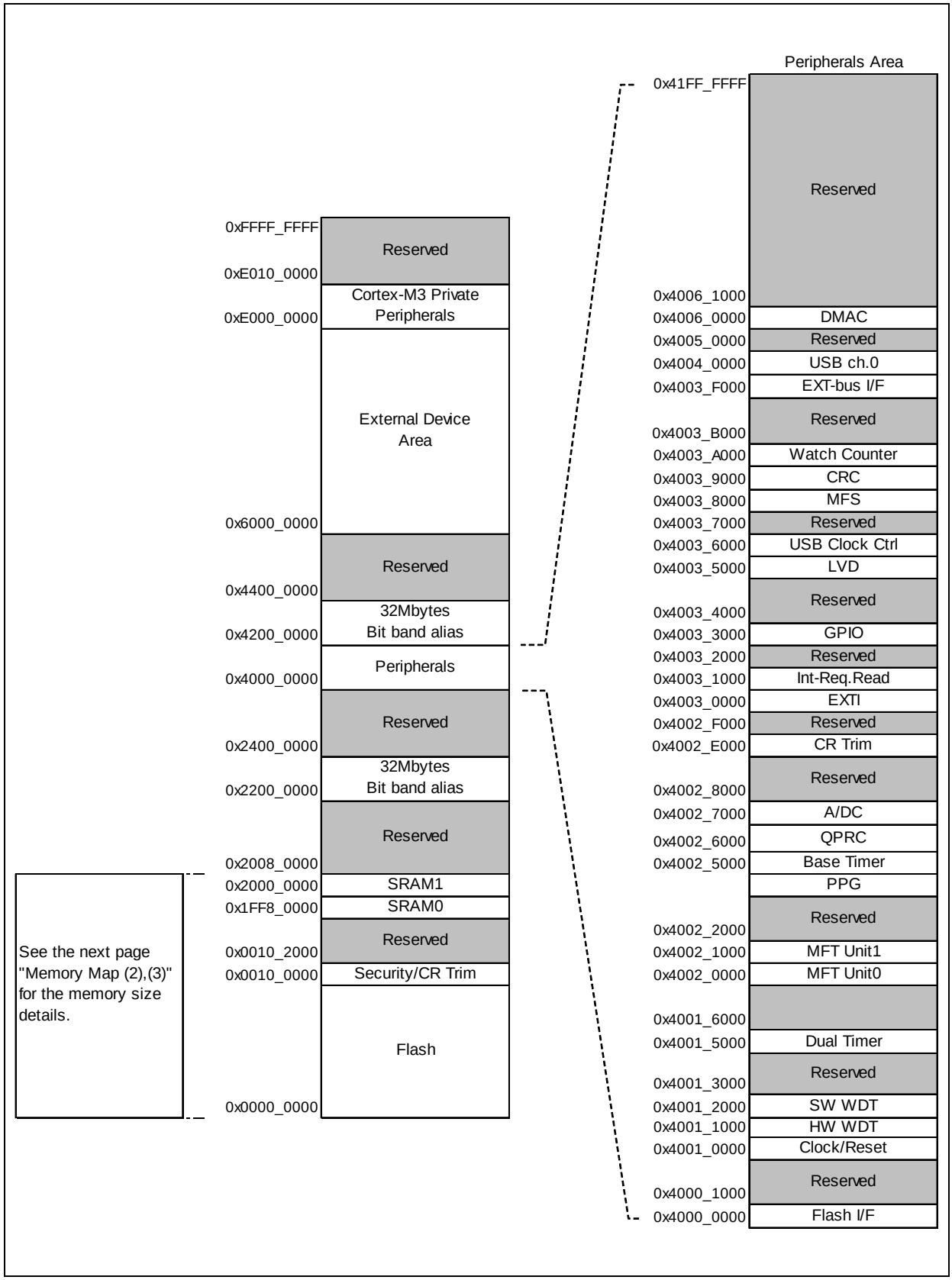
Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P00	General-purpose I/O port 0	77	55	A9	61	49
	P01		78	56	B9	62	50
	P02		79	57	B11	63	51
	P03		80	58	A8	64	52
	P04		81	59	B8	65	53
	P05		82	60	C8	-	-
	P06		83	61	D9	-	-
	P07		84	62	A7	66	-
	P08		85	63	B7	-	-
	P09		86	64	C7	-	-
	P0A		87	65	D7	67	54
	P0B		88	66	A6	68	55
	P0C		89	67	B6	69	56
	P0D		90	68	C6	70	-
	P0E		91	69	A5	71	-
	P0F		92	70	B5	72	57
	P10	General-purpose I/O port 1	52	30	J11	42	34
	P11		53	31	J10	43	35
	P12		54	32	J8	44	36
	P13		55	33	H10	45	37
	P14		56	34	H9	46	38
	P15		57	35	H7	47	39
	P16		58	36	G10	48	-
	P17		59	37	G9	49	40
	P18		63	41	G8	53	44
	P19		64	42	F10	54	45
	P1A		65	43	F9	55	-
	P1B		66	44	E11	56	-
	P1C		67	45	E10	-	-
	P1D		68	46	F8	-	-
	P1E		69	47	E9	-	-
	P1F		70	48	D11	-	-
	P20	General-purpose I/O port 2	74	52	C10	60	-
	P21		73	51	C11	59	48
	P22		72	50	E8	58	47
	P23		71	49	D10	57	46

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 0	DTTI0X_0	Input signal of wave form generator to control outputs RTO00 to RTO05 of multi-function timer 0	18	96	F4	13	9
	DTTI0X_1		69	47	E9	-	-
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	13	91	F1	-	-
	FRCK0_1		70	48	D11	-	-
	FRCK0_2		53	31	J10	43	35
	IC00_0	16-bit input capture input pin of multi-function timer 0 ICxx describes channel number.	17	95	G2	-	-
	IC00_1		65	43	F9	55	-
	IC00_2		54	32	J8	44	36
	IC01_0		16	94	G1	-	-
	IC01_1		66	44	E11	56	-
	IC01_2		55	33	H10	45	37
	IC02_0		15	93	F3	-	-
	IC02_1		67	45	E10	-	-
	IC02_2		56	34	H9	46	38
	IC03_0		14	92	F2	-	-
	IC03_1		68	46	F8	-	-
	IC03_2		57	35	H7	47	39
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG 0 output modes.	19	97	G3	14	10
	RTO00_1 (PPG00_1)		71	49	D10	-	-
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG 0 output modes.	20	98	H1	15	11
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG 0 output modes.	21	99	H2	16	12
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG 0 output modes.	22	100	G4	17	13
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG 0 output modes.	23	1	H3	18	14
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG 0 output modes.	24	2	J2	19	15

Type	Circuit	Remarks
I		・ CMOS level output ・ CMOS level hysteresis input ・ 5V tolerant ・ With standby mode control ・ I_{OH} = -4mA, I_{OL} = 4mA
J		CMOS level hysteresis input

■ MEMORY MAP

・ MB9A310A Series Memory Map(1)



・ Peripheral Address Map

Start address	End address	Bus	Peripherals
$0x4000\_0000_H$	$0x4000\_0FFF_H$	AHB	Flash I/F register
$0x4000\_1000_H$	$0x4000\_FFFF_H$		Reserved
$0x4001\_0000_H$	$0x4001\_0FFF_H$	APB0	Clock/Reset Control
$0x4001\_1000_H$	$0x4001\_1FFF_H$		Hardware Watchdog timer
$0x4001\_2000_H$	$0x4001\_2FFF_H$		Software Watchdog timer
$0x4001\_3000_H$	$0x4001\_4FFF_H$		Reserved
$0x4001\_5000_H$	$0x4001\_5FFF_H$		Dual-Timer
$0x4001\_6000_H$	$0x4001\_FFFF_H$		Reserved
$0x4002\_0000_H$	$0x4002\_0FFF_H$	APB1	Multi-function timer unit0
$0x4002\_1000_H$	$0x4002\_1FFF_H$		Multi-function timer unit1
$0x4002\_2000_H$	$0x4002\_3FFF_H$		Reserved
$0x4002\_4000_H$	$0x4002\_4FFF_H$		PPG
$0x4002\_5000_H$	$0x4002\_5FFF_H$		Base Timer
$0x4002\_6000_H$	$0x4002\_6FFF_H$		Quadrature Position/Revolution Counter
$0x4002\_7000_H$	$0x4002\_7FFF_H$		A/D Converter
$0x4002\_8000_H$	$0x4002\_DFFF_H$		Reserved
$0x4002\_E000_H$	$0x4002\_EFFF_H$		Built-in CR trimming
$0x4002\_F000_H$	$0x4002\_FFFF_H$		Reserved
$0x4003\_0000_H$	$0x4003\_0FFF_H$	APB2	External Interrupt Controller
$0x4003\_1000_H$	$0x4003\_1FFF_H$		Interrupt Source Check Register
$0x4003\_2000_H$	$0x4003\_2FFF_H$		Reserved
$0x4003\_3000_H$	$0x4003\_3FFF_H$		GPIO
$0x4003\_4000_H$	$0x4003\_4FFF_H$		Reserved
$0x4003\_5000_H$	$0x4003\_5FFF_H$		Low-Voltage Detector
$0x4003\_6000_H$	$0x4003\_6FFF_H$		USB clock generator
$0x4003\_7000_H$	$0x4003\_7FFF_H$		Reserved
$0x4003\_8000_H$	$0x4003\_8FFF_H$		Multi-function serial
$0x4003\_9000_H$	$0x4003\_9FFF_H$		CRC
$0x4003\_A000_H$	$0x4003\_AFFF_H$		Watch Counter
$0x4003\_B000_H$	$0x4003\_EFFF_H$		Reserved
$0x4003\_F000_H$	$0x4003\_FFFF_H$		External bus interface
$0x4004\_0000_H$	$0x4004\_FFFF_H$	AHB	USB ch.0
$0x4005\_0000_H$	$0x4005\_FFFF_H$		Reserved
$0x4006\_0000_H$	$0x4006\_0FFF_H$		DMAC register
$0x4006\_1000_H$	$0x4006\_1FFF_H$		Reserved
$0x4006\_2000_H$	$0x4006\_2FFF_H$		Reserved
$0x4006\_3000_H$	$0x4006\_3FFF_H$		Reserved
$0x4006\_4000_H$	$0x41FF\_FFFF_H$		Reserved

(4-1) Operating Conditions of Main and USB PLL (In the case of using main clock for input clock of PLL)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	

*: Time from when the PLL starts operating until the oscillation stabilizes.

(4-2) Operating Conditions of Main PLL (In the case of using the built-in high speed CR for the input clock of the main PLL)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	300	MHz	

*: Time from when the PLL starts operating until the oscillation stabilizes.

Note: Make sure to input the built-in high-speed CR clock that has been trimmed.
When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

(5) Reset Input Characteristics

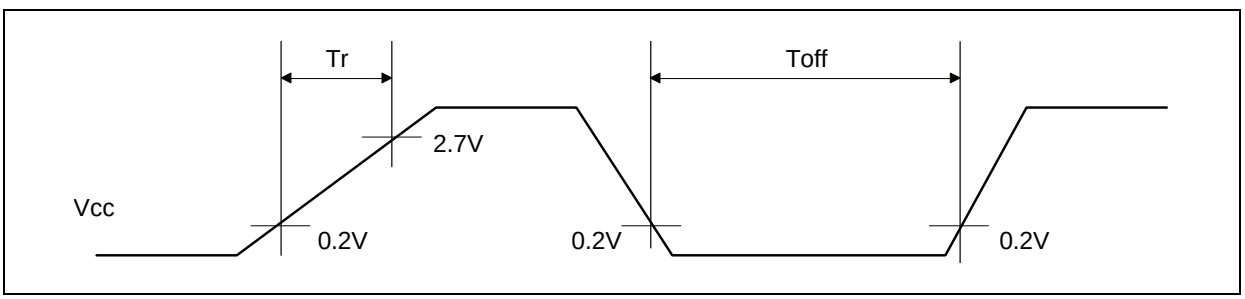
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

(6) Power-on Reset Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	Vcc	0	-	ms	
Power supply shut down time	Toff		1	-	ms	

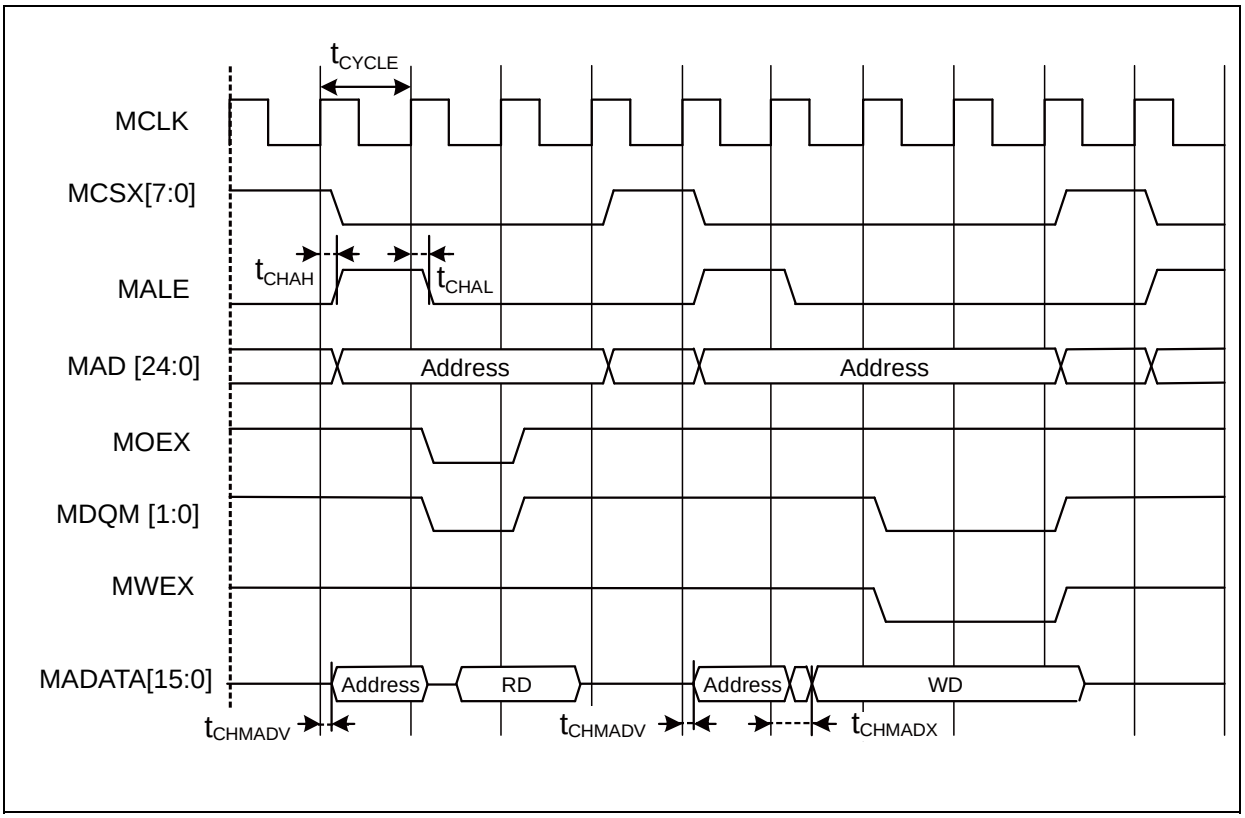


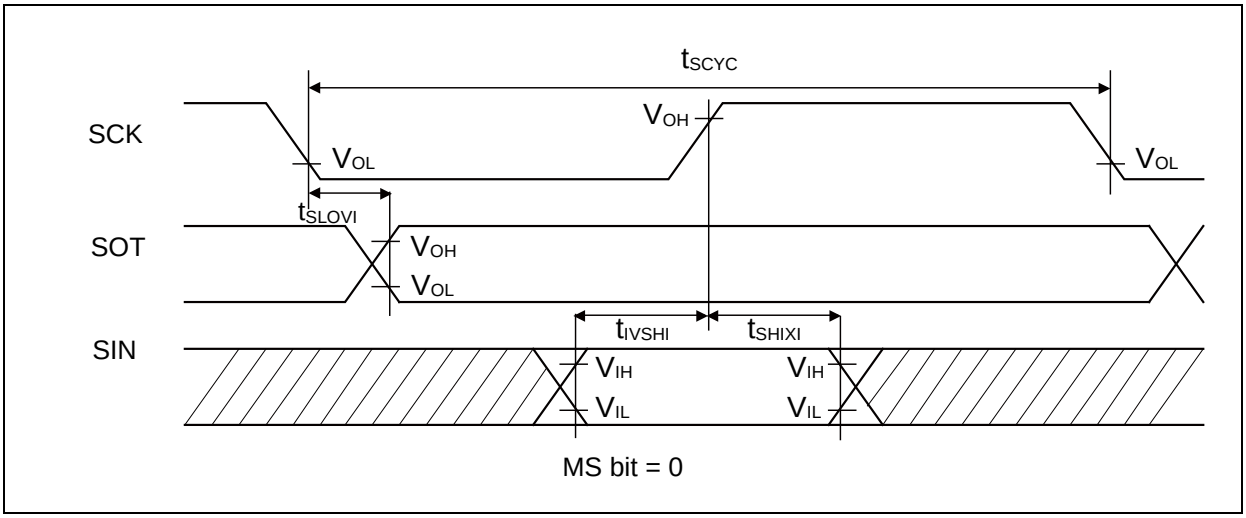
- Multiplexed Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

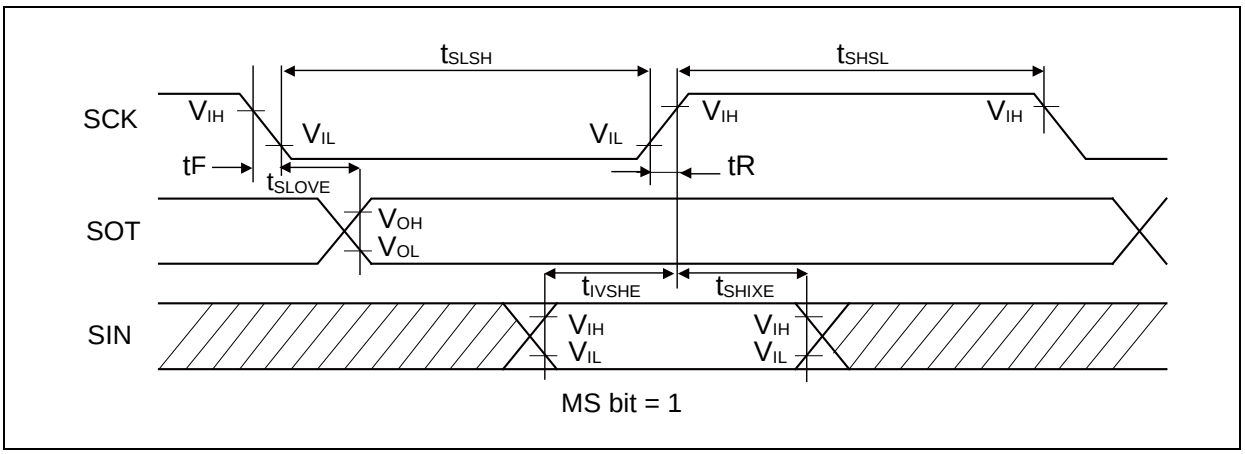
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK ALE	Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
	t_{CHAH}		Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				

Note: When the external load capacitance C_L = 30pF.





MS bit = 0



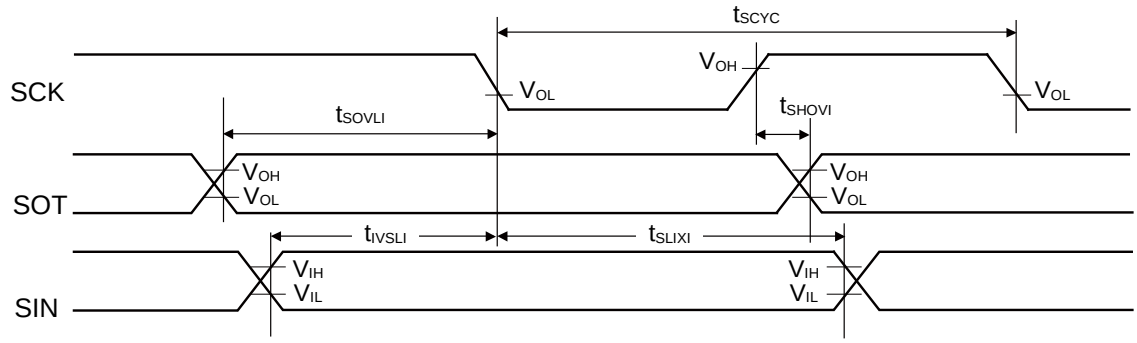
MS bit = 1

・ Synchronous serial(SPI = 1, SCINV = 0)

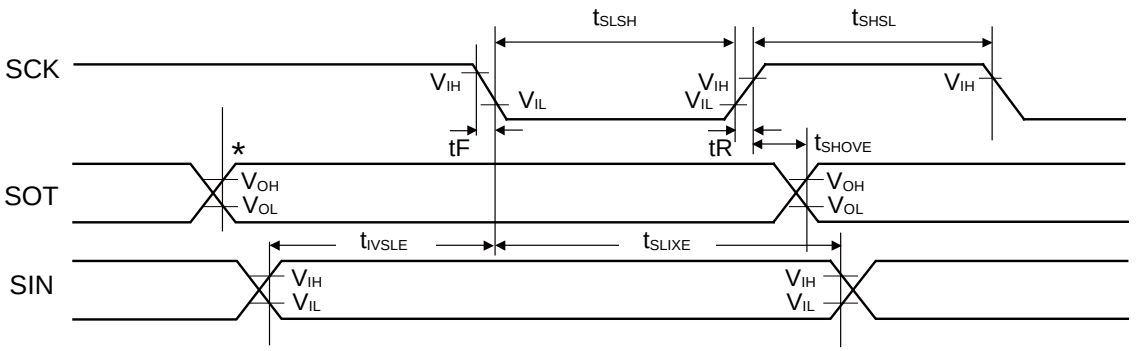
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx SOTx		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- tCYCP indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



MS bit = 0



MS bit = 1

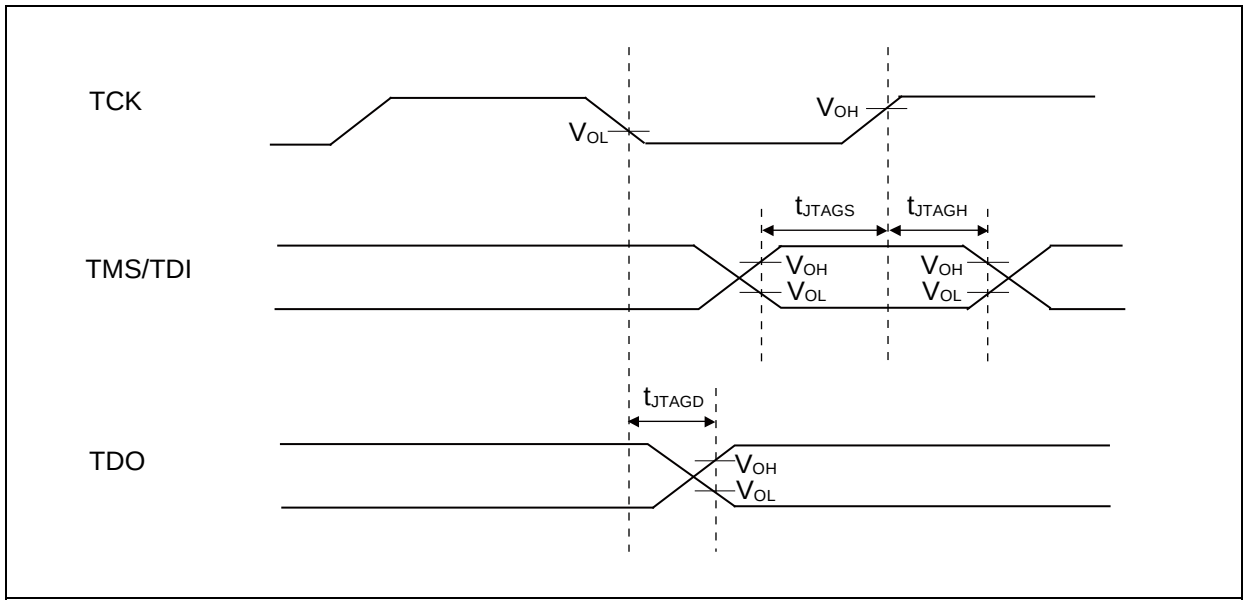
*: Changes when writing to TDR register

(14) JTAG timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TMS, TDI hold time	t_{JTAGH}	TCK TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TDO delay time	t_{JTAGD}	TCK TDO	Vcc ≥ 4.5V	-	25	ns	
			Vcc < 4.5V	-	45		

Note: When the external load capacitance C_L = 30pF.



5. 12-bit A/D Converter

・ Electrical Characteristics for the A/D Converter

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	-	-	-	12	bit	
Non-linearity error	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7V to 5.5V
Differential linearity error	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	AN0 to AN15	- 20	-	+ 20	mV	
Full-scale transition voltage	AN0 to AN15	AVRH-20	-	AVRH+20	mV	
Conversion time	-	1.0*1	-	-	µs	AVcc ≥ 4.5V
Sampling time	Ts	*2	-	-	ns	AVcc ≥ 4.5V
		*2	-	-		AVcc < 4.5V
Compare clock cycle*3	Tcck	50	-	2000	ns	
State transition time to operation permission	Tstt	1.0	-	-	µs	
Power supply current (analog + digital)	AVCC	-	0.57	0.72	mA	A/D 1unit operation
		-	0.06	20	µA	When A/D stops
Reference power supply current (between AVRH and AVSS)	AVRH	-	1.1	1.96	mA	A/D 1unit operation AVRH = 5.5V
		-	0.06	4	µA	When A/D stops
Analog input capacity	Cin	-	-	12.9	pF	
Analog input resistor	Rin	-	-	2	kΩ	AVcc ≥ 4.5V
				3.8		AVcc < 4.5V
Interchannel disparity	-	-	-	4	LSB	
Analog port input current	AN0 to AN15	-	-	5	µA	
Analog input voltage	AN0 to AN15	AVSS	-	AVRH	V	
Reference voltage	AVRH	2.7	-	AVCC	V	

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 300ns, the value of compare time: 700ns (AVcc ≥ 4.5V).
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".
The A/D Converter register is set at APB bus clock timing. The sampling clock and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance.
Ensure that it set the sampling time to satisfy (Equation 1)

*3: The compare time (Tc) is the value of (Equation 2)

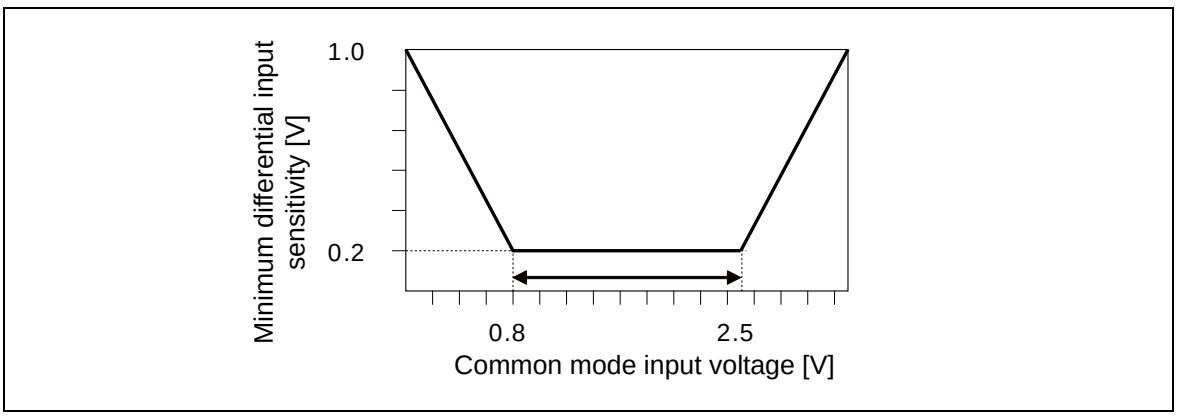
6. USB characteristics

(Vcc = 2.7V to 5.5V,USBVcc = 3.0V to 3.6V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input High level voltage	V_{IH}	UDP0, UDM0	-	2.0	USBVcc + 0.3	V	*1
	Input Low level voltage	V_{IL}		-	Vss - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}		External pull-down resistance = 15kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}		External pull-up resistance = 1.5kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full Speed	4	20	ns	*5
	Falling time	t_{FF}		Full Speed	4	20	ns	*5
	Rise/fall time matching	t_{FRFM}		Full Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low Speed	75	300	ns	*7
	Falling time	t_{LF}		Low Speed	75	300	ns	*7
	Rise/fall time matching	t_{LRFM}		Low Speed	80	125	%	*7

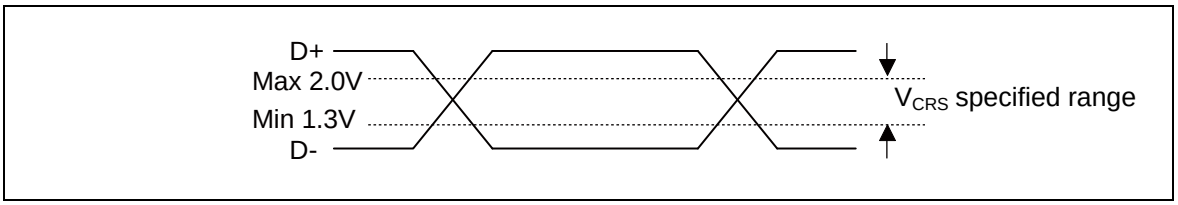
*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2 : Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.

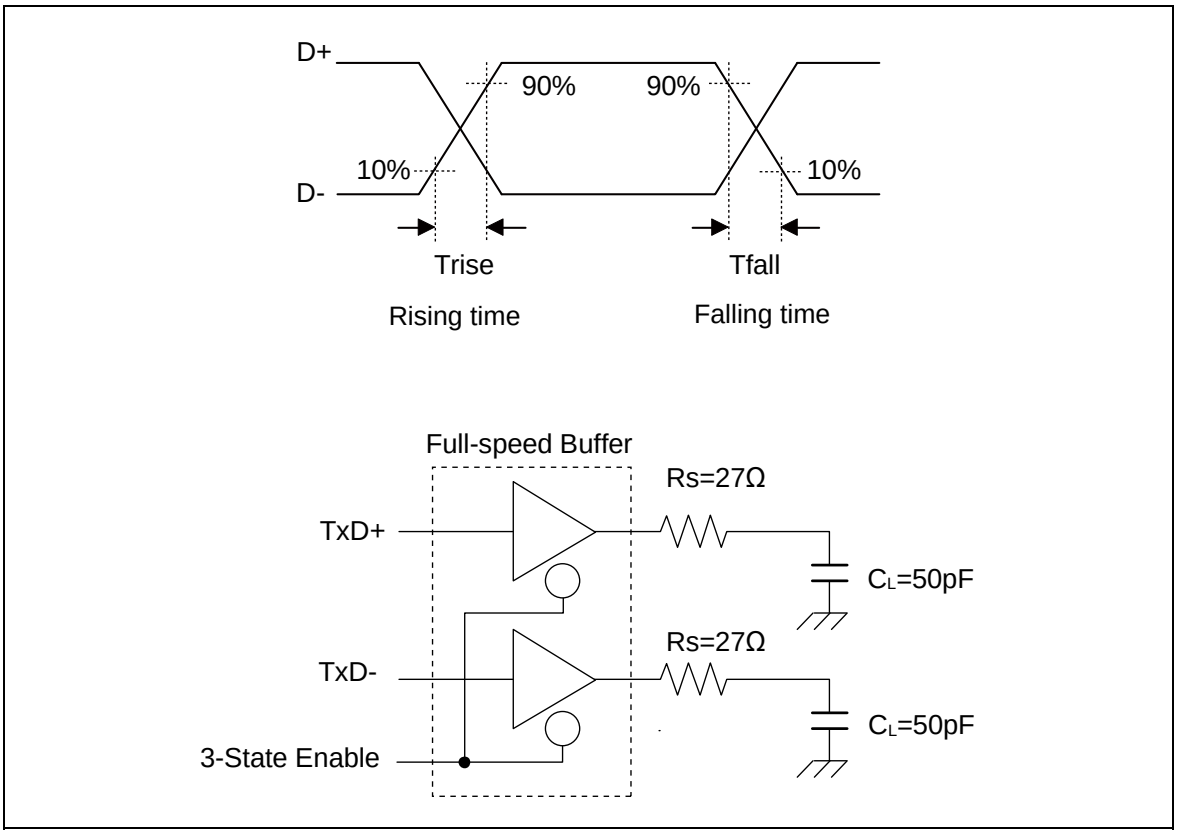


*3 : The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the ground and 1.5 kΩ load) at High-State (V_{OH}).

*4 : The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



*5 : They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.



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