Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af314mapmc-g-jne2

- Watch Counter

  The Watch counter is used for wake up from Low-Power Consumption mode.

  - Interval timer: up to 64s(Max)@ Sub Clock : 32.768kHz

- External Interrupt Controller Unit
  - Up to 16 external interrupt input pins.
  - Include one non-maskable interrupt (NMI) input pin.

- Watch dog Timer (2channels)

  A watchdog timer can generate interrupts or a reset when a time-out value is reached.

  This series consists of two different watchdogs, a "Hardware" watchdog and a, "Software" watchdog.

  The "Hardware" watchdog timer is clocked by the built-in low speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except STOP.

- CRC (Cyclic Redundancy Check) Accelerator

  The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

  CCITT CRC16 and IEEE-802.3 CRC32 are supported.

  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

- Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4MHz to 48MHz
- Sub Clock : 32.768kHz
- Built-in high-speed CR Clock: 4MHz
- Built-in low-speed CR Clock: 100kHz
- Main PLL Clock

[Resets]

Reset requests from INITX pins, Power on reset, Software reset, watchdog timers reset, low-voltage detection reset and clock supervisor reset.

- Clock Super Visor (CSV)

  Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

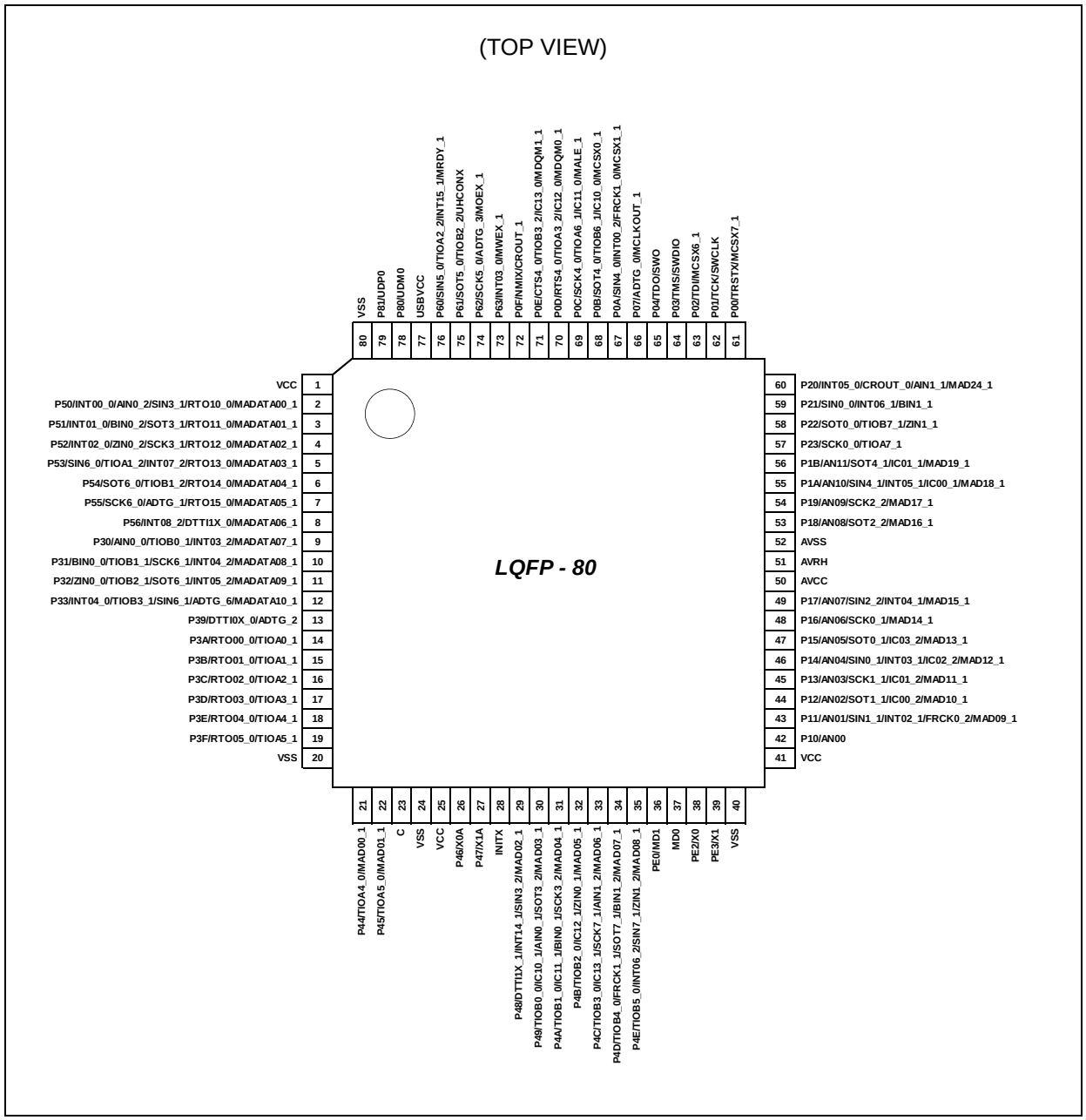
  - External clock failure (clock stop) is detected, reset is asserted.
  - External frequency anomaly is detected, interrupt or reset is asserted.

- Low-Voltage Detector (LVD)

  This Series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

  - LVD1: error reporting via interrupt
  - LVD2: auto-reset operation

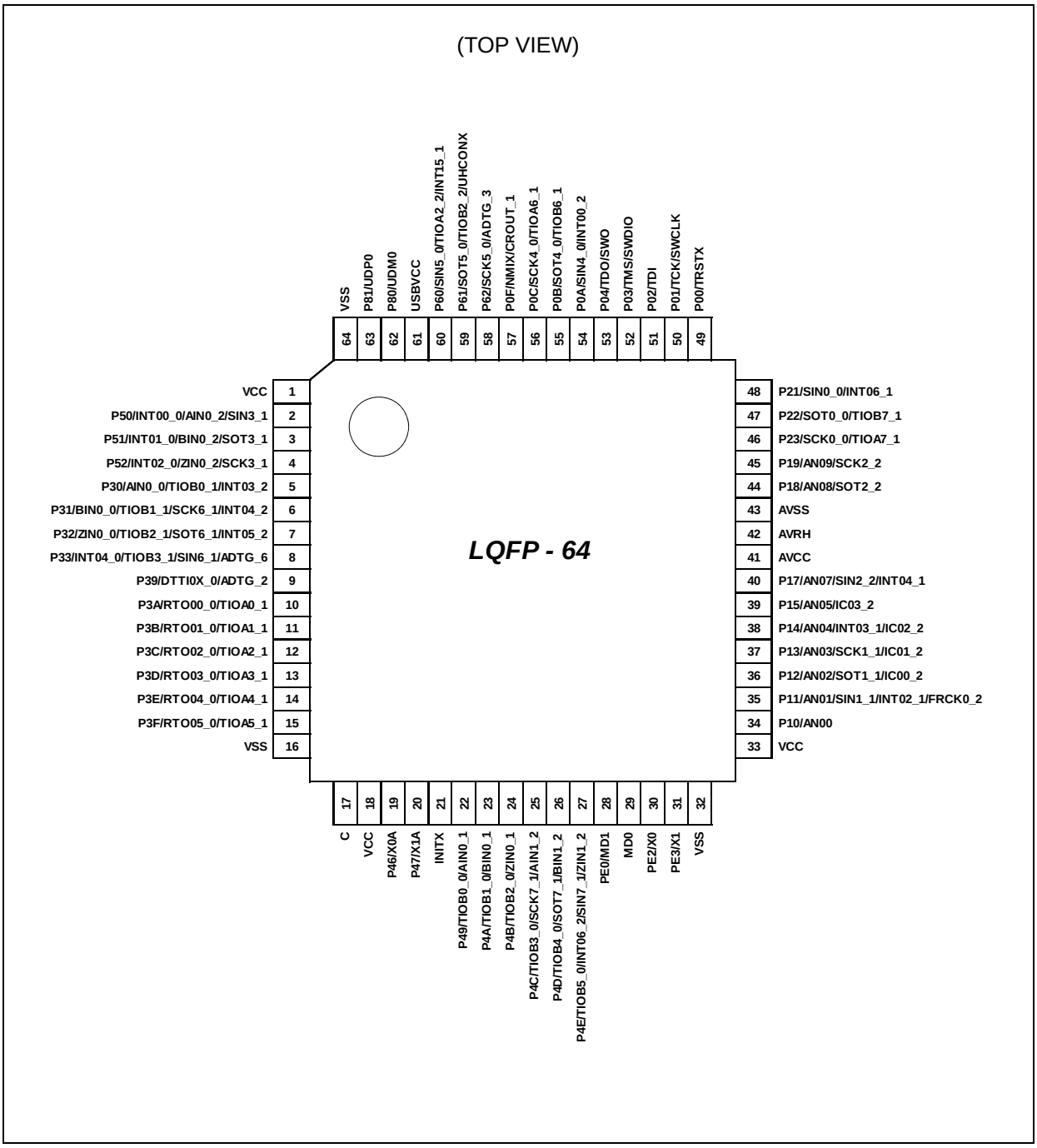
・ FPT-80P-M21/FPT-80P-M37



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

・ FPT-64P-M23/M24/M38/M39



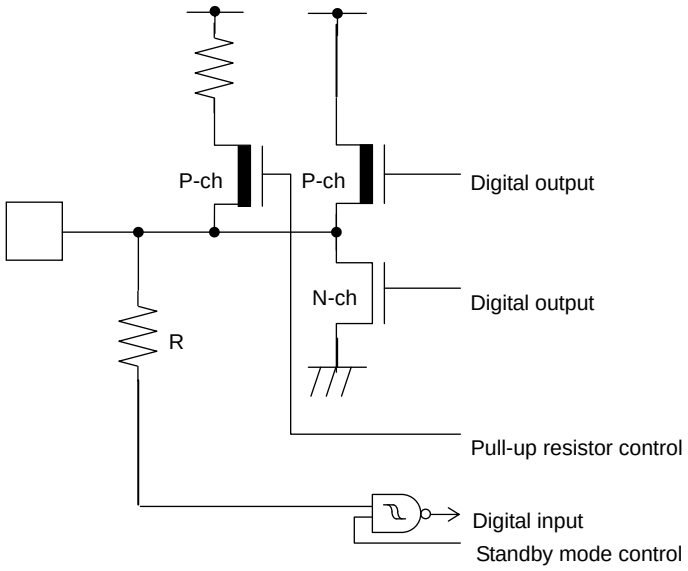
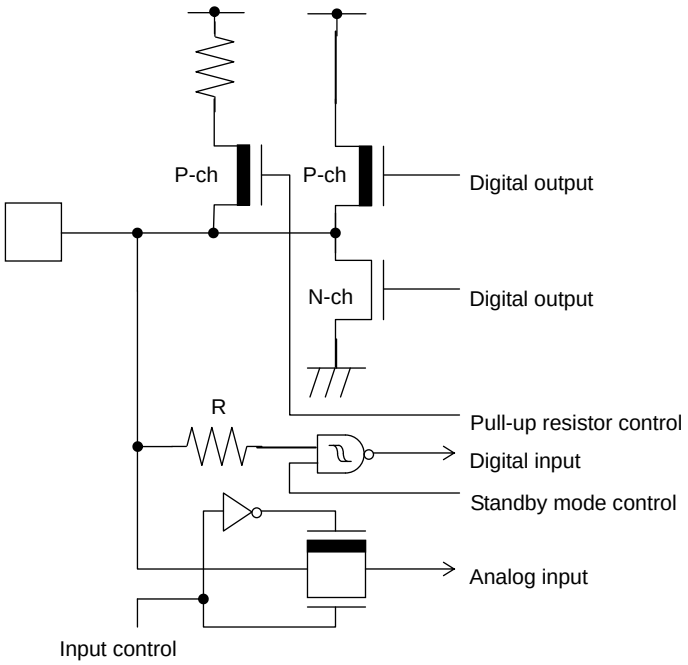
<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P30	General-purpose I/O port 3	9	87	E1	9	5
	P31		10	88	E2	10	6
	P32		11	89	E3	11	7
	P33		12	90	E4	12	8
	P34		13	91	F1	-	-
	P35		14	92	F2	-	-
	P36		15	93	F3	-	-
	P37		16	94	G1	-	-
	P38		17	95	G2	-	-
	P39		18	96	F4	13	9
	P3A		19	97	G3	14	10
	P3B		20	98	H1	15	11
	P3C		21	99	H2	16	12
	P3D		22	100	G4	17	13
	P3E		23	1	H3	18	14
	P3F		24	2	J2	19	15
	P40	General-purpose I/O port 4	27	5	J4	-	-
	P41		28	6	L5	-	-
	P42		29	7	K5	-	-
	P43		30	8	J5	-	-
	P44		31	9	H5	21	-
	P45		32	10	L6	22	-
	P46		36	14	L3	26	19
	P47		37	15	K3	27	20
	P48		39	17	K6	29	-
	P49		40	18	J6	30	22
	P4A		41	19	L7	31	23
	P4B		42	20	K7	32	24
	P4C		43	21	H6	33	25
	P4D		44	22	J7	34	26
	P4E		45	23	K8	35	27
	P50	General-purpose I/O port 5	2	80	C1	2	2
	P51		3	81	C2	3	3
	P52		4	82	B3	4	4
	P53		5	83	D1	5	-
	P54		6	84	D2	6	-
	P55		7	85	D3	7	-
	P56		8	86	D5	8	-
	P60	General-purpose I/O port 6	96	74	C4	76	60
	P61		95	73	B4	75	59
	P62		94	72	C5	74	58
	P63		93	71	D6	73	-
	P80	General-purpose I/O port 8	98	76	A3	78	62
	P81		99	77	A2	79	63
	PE0	General-purpose I/O port E	46	24	K9	36	28
	PE2		48	26	L9	38	30
	PE3		49	27	L10	39	31

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 2	SIN2_2	Multifunction serial interface ch.2 input pin	59	37	G9	49	40
	SOT2_2 (SDA2_2)	Multifunction serial interface ch.2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	63	41	G8	53	44
	SCK2_2 (SCL2_2)	Multifunction serial interface ch.2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	64	42	F10	54	45
Multi Function Serial 3	SIN3_1	Multifunction serial interface ch.3 input pin	2	80	C1	2	2
	SIN3_2		39	17	K6	29	-
	SOT3_1 (SDA3_1)	Multifunction serial interface ch.3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	3	81	C2	3	3
	SOT3_2 (SDA3_2)		40	18	J6	30	-
	SCK3_1 (SCL3_1)	Multifunction serial interface ch.3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	82	B3	4	4
	SCK3_2 (SCL3_2)		41	19	L7	31	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 0	DTTI0X_0	Input signal of wave form generator to control outputs RTO00 to RTO05 of multi-function timer 0	18	96	F4	13	9
	DTTI0X_1		69	47	E9	-	-
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	13	91	F1	-	-
	FRCK0_1		70	48	D11	-	-
	FRCK0_2		53	31	J10	43	35
	IC00_0	16-bit input capture input pin of multi-function timer 0 ICxx describes channel number.	17	95	G2	-	-
	IC00_1		65	43	F9	55	-
	IC00_2		54	32	J8	44	36
	IC01_0		16	94	G1	-	-
	IC01_1		66	44	E11	56	-
	IC01_2		55	33	H10	45	37
	IC02_0		15	93	F3	-	-
	IC02_1		67	45	E10	-	-
	IC02_2		56	34	H9	46	38
	IC03_0		14	92	F2	-	-
	IC03_1		68	46	F8	-	-
	IC03_2		57	35	H7	47	39
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG 0 output modes.	19	97	G3	14	10
	RTO00_1 (PPG00_1)		71	49	D10	-	-
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG 0 output modes.	20	98	H1	15	11
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG 0 output modes.	21	99	H2	16	12
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG 0 output modes.	22	100	G4	17	13
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG 0 output modes.	23	1	H3	18	14
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG 0 output modes.	24	2	J2	19	15

Type	Circuit	Remarks
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 50kΩ ・I_{OH} = -4mA, I_{OL} = 4mA
F		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 50kΩ ・I_{OH} = -4mA, I_{OL} = 4mA

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

・ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

・ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

・ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

・ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

・ Peripheral Address Map

Start address	End address	Bus	Peripherals
$0x4000\_0000_H$	$0x4000\_0FFF_H$	AHB	Flash I/F register
$0x4000\_1000_H$	$0x4000\_FFFF_H$		Reserved
$0x4001\_0000_H$	$0x4001\_0FFF_H$	APB0	Clock/Reset Control
$0x4001\_1000_H$	$0x4001\_1FFF_H$		Hardware Watchdog timer
$0x4001\_2000_H$	$0x4001\_2FFF_H$		Software Watchdog timer
$0x4001\_3000_H$	$0x4001\_4FFF_H$		Reserved
$0x4001\_5000_H$	$0x4001\_5FFF_H$		Dual-Timer
$0x4001\_6000_H$	$0x4001\_FFFF_H$		Reserved
$0x4002\_0000_H$	$0x4002\_0FFF_H$	APB1	Multi-function timer unit0
$0x4002\_1000_H$	$0x4002\_1FFF_H$		Multi-function timer unit1
$0x4002\_2000_H$	$0x4002\_3FFF_H$		Reserved
$0x4002\_4000_H$	$0x4002\_4FFF_H$		PPG
$0x4002\_5000_H$	$0x4002\_5FFF_H$		Base Timer
$0x4002\_6000_H$	$0x4002\_6FFF_H$		Quadrature Position/Revolution Counter
$0x4002\_7000_H$	$0x4002\_7FFF_H$		A/D Converter
$0x4002\_8000_H$	$0x4002\_DFFF_H$		Reserved
$0x4002\_E000_H$	$0x4002\_EFFF_H$		Built-in CR trimming
$0x4002\_F000_H$	$0x4002\_FFFF_H$		Reserved
$0x4003\_0000_H$	$0x4003\_0FFF_H$	APB2	External Interrupt Controller
$0x4003\_1000_H$	$0x4003\_1FFF_H$		Interrupt Source Check Register
$0x4003\_2000_H$	$0x4003\_2FFF_H$		Reserved
$0x4003\_3000_H$	$0x4003\_3FFF_H$		GPIO
$0x4003\_4000_H$	$0x4003\_4FFF_H$		Reserved
$0x4003\_5000_H$	$0x4003\_5FFF_H$		Low-Voltage Detector
$0x4003\_6000_H$	$0x4003\_6FFF_H$		USB clock generator
$0x4003\_7000_H$	$0x4003\_7FFF_H$		Reserved
$0x4003\_8000_H$	$0x4003\_8FFF_H$		Multi-function serial
$0x4003\_9000_H$	$0x4003\_9FFF_H$		CRC
$0x4003\_A000_H$	$0x4003\_AFFF_H$		Watch Counter
$0x4003\_B000_H$	$0x4003\_EFFF_H$		Reserved
$0x4003\_F000_H$	$0x4003\_FFFF_H$		External bus interface
$0x4004\_0000_H$	$0x4004\_FFFF_H$	AHB	USB ch.0
$0x4005\_0000_H$	$0x4005\_FFFF_H$		Reserved
$0x4006\_0000_H$	$0x4006\_0FFF_H$		DMAC register
$0x4006\_1000_H$	$0x4006\_1FFF_H$		Reserved
$0x4006\_2000_H$	$0x4006\_2FFF_H$		Reserved
$0x4006\_3000_H$	$0x4006\_3FFF_H$		Reserved
$0x4006\_4000_H$	$0x41FF\_FFFF_H$		Reserved

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

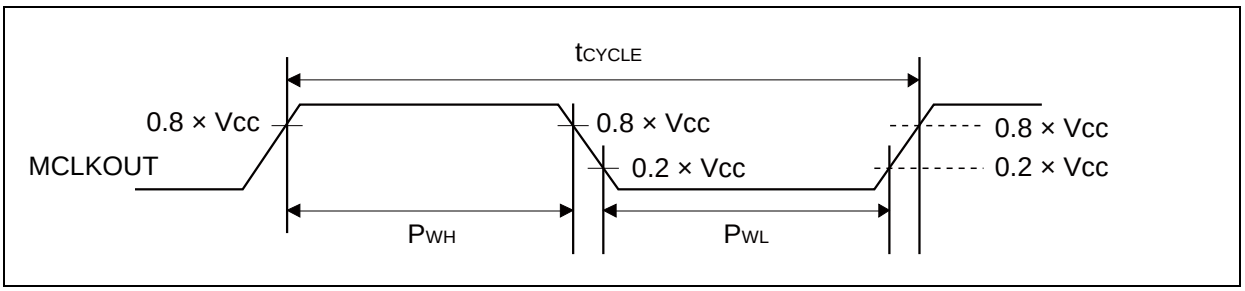
(7) External Bus Timing

・ External bus clock output Characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT	Vcc ≥ 4.5 V	-	40	MHz
			Vcc < 4.5 V	-	32	MHz
Minimum clock cycle time	-		Vcc ≥ 4.5 V	25	-	ns
			Vcc < 4.5 V	31.25	-	ns

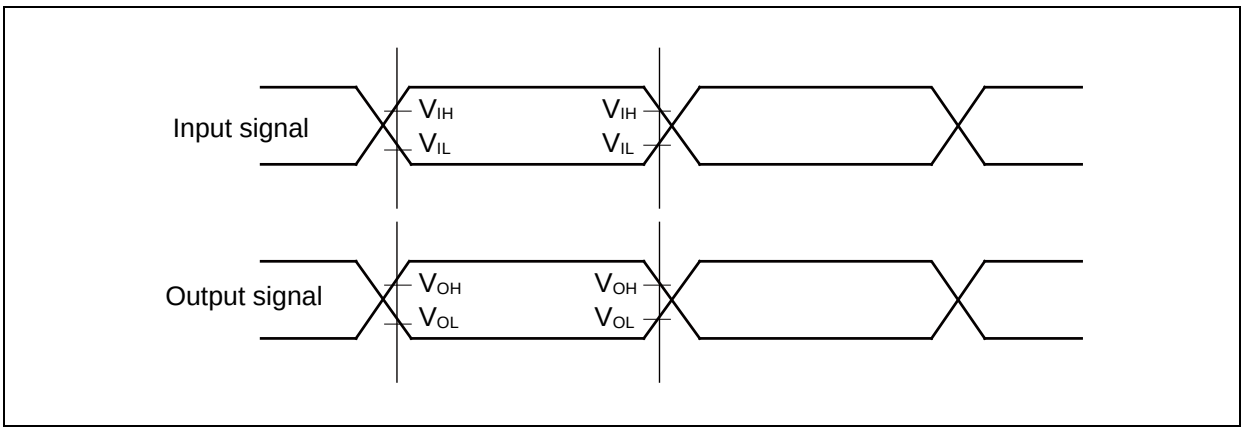
Note: The external bus clock output is a divided clock of HCLK. For more information about setting of clock divider, see "Chapter: External Bus Interface" in "FM3 Family PERIPHERAL MANUAL"
When external bus clock is not output, this characteristics does not give any effect on external bus operation.

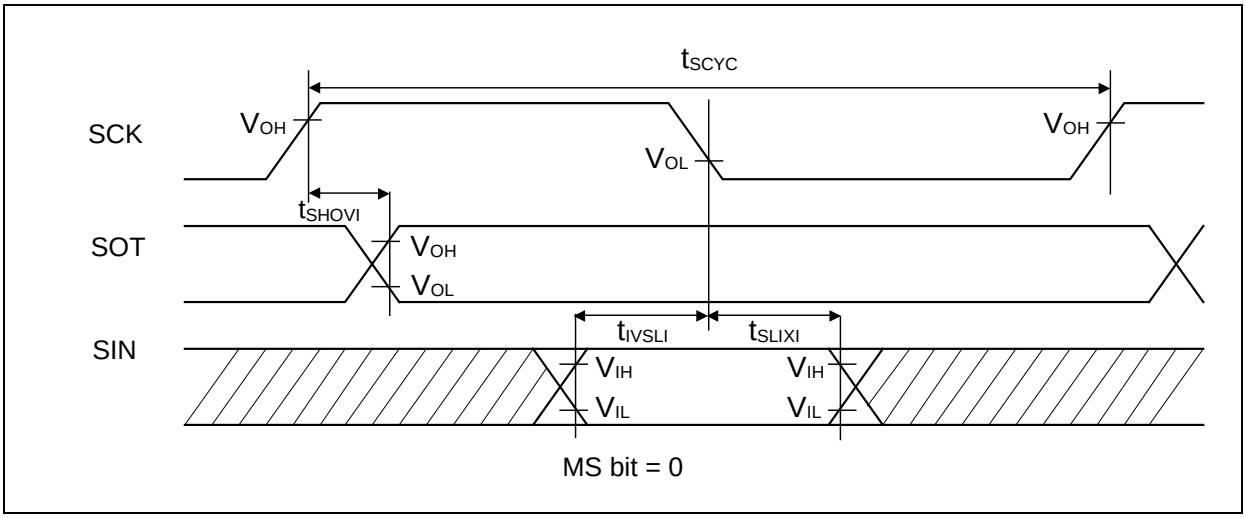


・ External bus signal input/output Characteristics

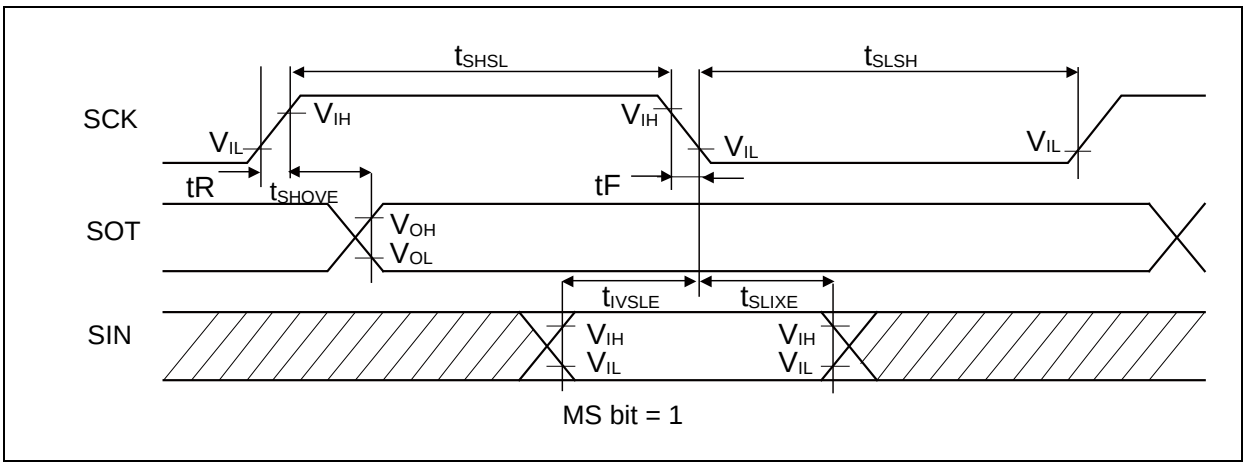
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × VCC	V	
	V_{IL}		0.2 × VCC	V	
Signal output characteristics	V_{OH}		0.8 × VCC	V	
	V_{OL}		0.2 × VCC	V	





MS bit = 0



MS bit = 1

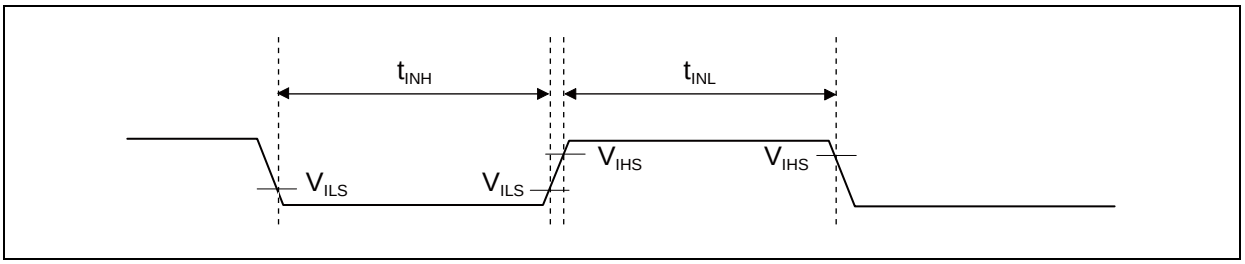
(10) External input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Wave form generator
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt
				500*2	-	ns	NMI

*1 : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode, in timer mode.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "■BLOCK DIAGRAM" in this data sheet.

*2 : When in stop mode, in timer mode.



(12) I^2C timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

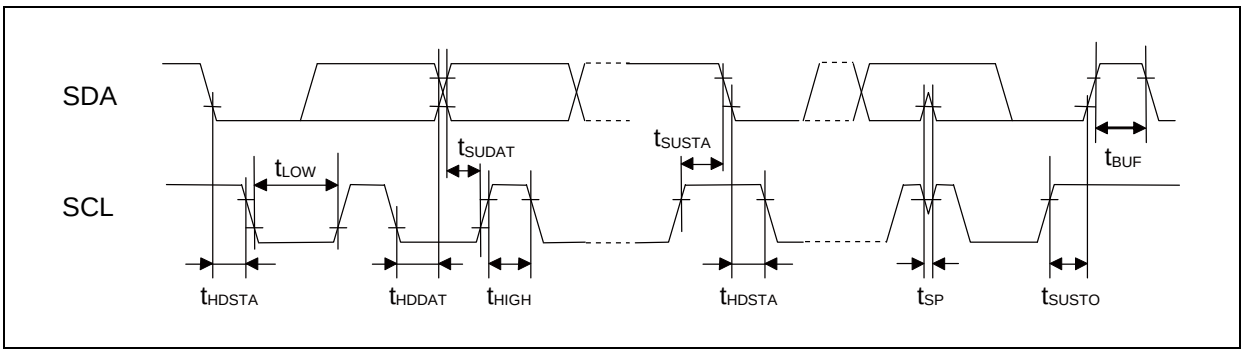
Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓→ SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1 : R and C represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4 : t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "■BLOCK DIAGRAM" in this data sheet.
To use I^2C, set the APB bus clock at 8 MHz or more.



5. 12-bit A/D Converter

・ Electrical Characteristics for the A/D Converter

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

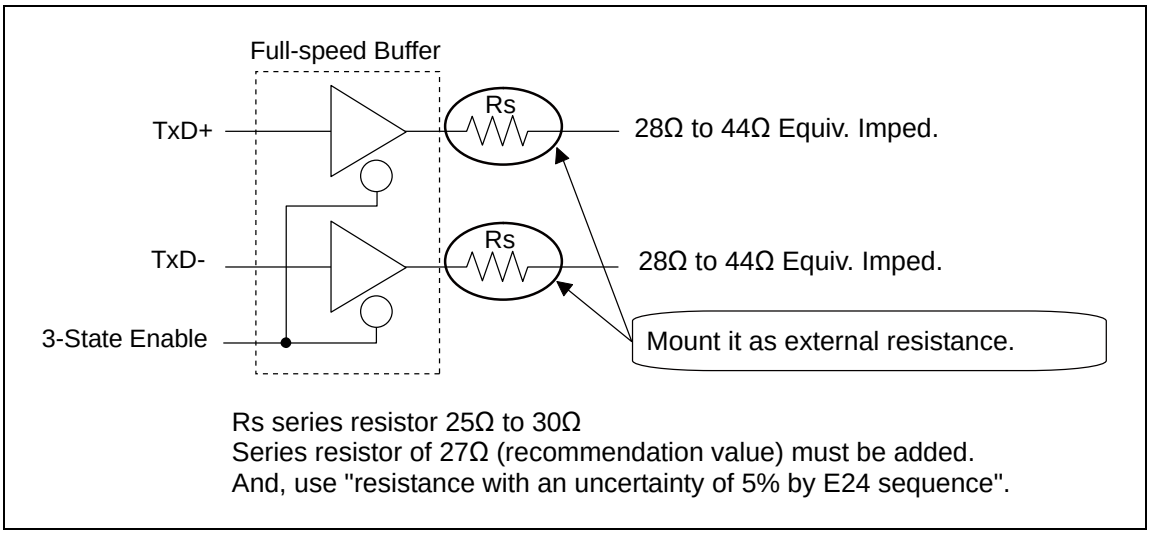
Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	-	-	-	12	bit	
Non-linearity error	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7V to 5.5V
Differential linearity error	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	AN0 to AN15	- 20	-	+ 20	mV	
Full-scale transition voltage	AN0 to AN15	AVRH-20	-	AVRH+20	mV	
Conversion time	-	1.0*1	-	-	µs	AVcc ≥ 4.5V
Sampling time	Ts	*2	-	-	ns	AVcc ≥ 4.5V
		*2	-	-		AVcc < 4.5V
Compare clock cycle*3	Tcck	50	-	2000	ns	
State transition time to operation permission	Tstt	1.0	-	-	µs	
Power supply current (analog + digital)	AVCC	-	0.57	0.72	mA	A/D 1unit operation
		-	0.06	20	µA	When A/D stops
Reference power supply current (between AVRH and AVSS)	AVRH	-	1.1	1.96	mA	A/D 1unit operation AVRH = 5.5V
		-	0.06	4	µA	When A/D stops
Analog input capacity	Cin	-	-	12.9	pF	
Analog input resistor	Rin	-	-	2	kΩ	AVcc ≥ 4.5V
				3.8		AVcc < 4.5V
Interchannel disparity	-	-	-	4	LSB	
Analog port input current	AN0 to AN15	-	-	5	µA	
Analog input voltage	AN0 to AN15	AVSS	-	AVRH	V	
Reference voltage	AVRH	2.7	-	AVCC	V	

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 300ns, the value of compare time: 700ns (AVcc ≥ 4.5V).
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".
The A/D Converter register is set at APB bus clock timing. The sampling clock and compare clock are set at Base clock (HCLK).

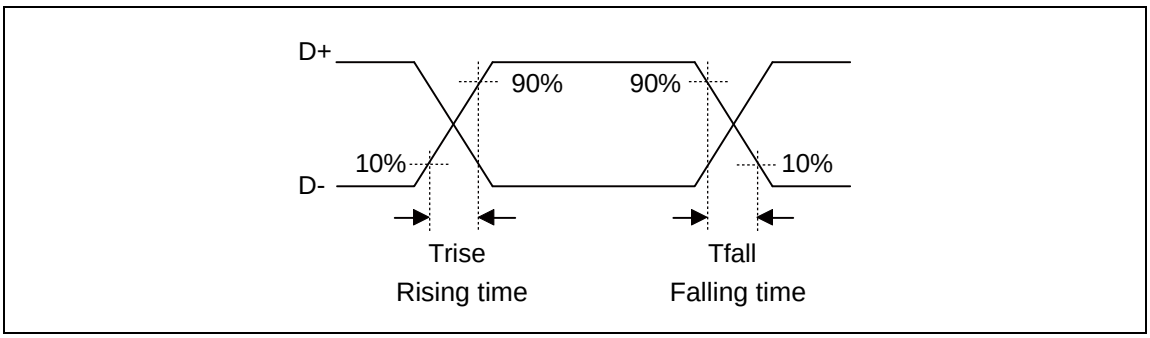
*2: A necessary sampling time changes by external impedance.
Ensure that it set the sampling time to satisfy (Equation 1)

*3: The compare time (Tc) is the value of (Equation 2)

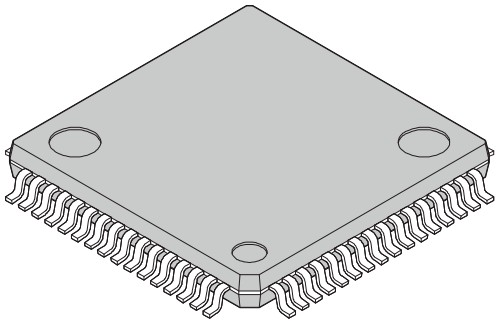
*6 : USB Full-speed connection is performed via twist pair cable shield with 90Ω ± 15% characteristic impedance(Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28Ωto 44Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB FLS I/O, use it with 25Ω to 30Ω (recommendation value 27Ω) series resistor Rs.



*7 : They indicate rising time (Trise) and falling time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.

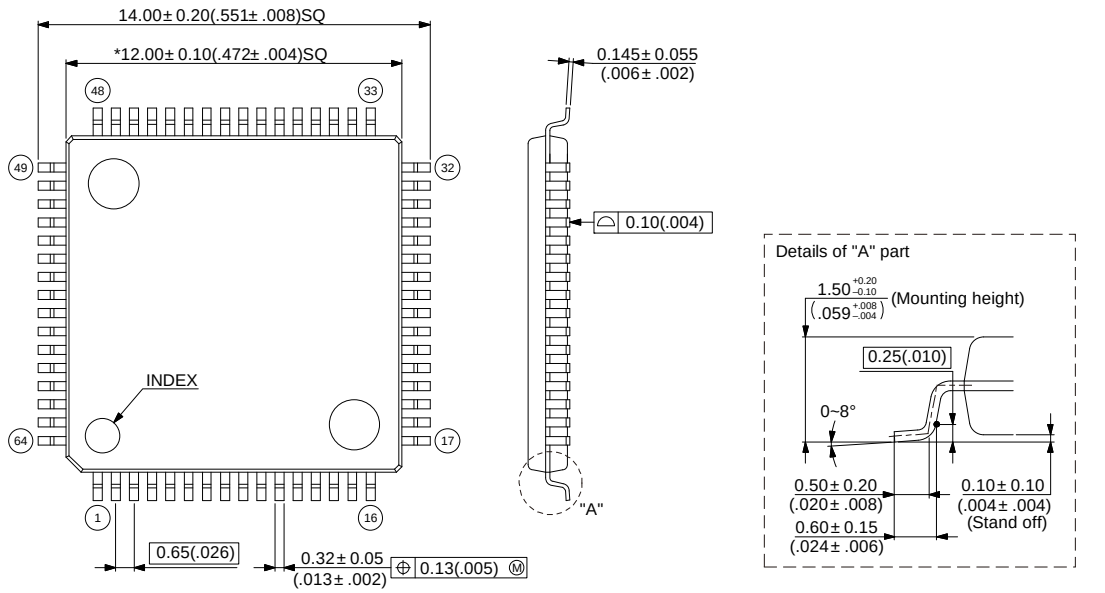


See "· Low-Speed Load (Compliance Load)" for conditions of external load.

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M23)	Code (Reference)	P-LQFP64-12 × 12-0.65

64-pin plastic LQFP
(FPT-64P-M23)

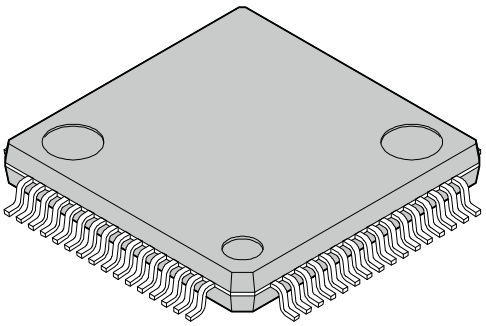
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP

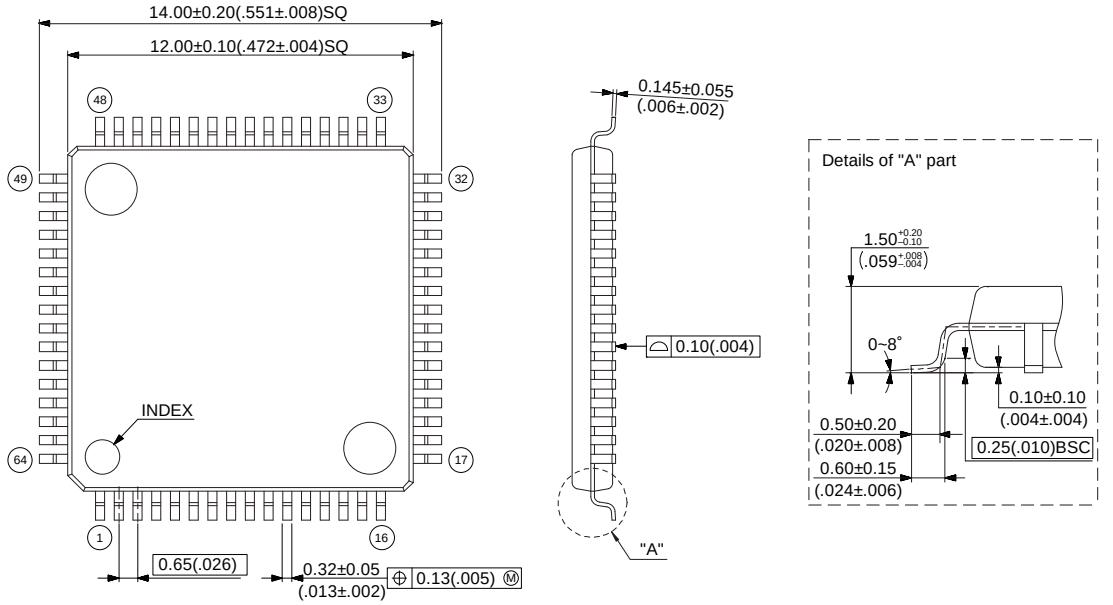


(FPT-64P-M39)

Lead pitch	0.65 mm
Package width × package length	12.00 mm × 12.00 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.47 g

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO