Infineon Technologies - MB9AF314NAPMC-G-JNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af314napmc-g-jne2

- Base Timer (Max 8channels)

  Operation mode is selectable from the followings for each channel.

  - 16-bit PWM timer
  - 16-bit PPG timer
  - 16/32-bit reload timer
  - 16/32-bit PWC timer

- General-Purpose I/O Port

  This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

  - Capable of pull-up control per pin
  - Capable of reading pin level directly
  - Built-in the port relocate function
  - Up to 83 fast General Purpose I/O Ports @ 100pin Package
  - Some ports are 5V tolerant I/O (MB9AF315MA/NA, MB9AF316MA/NA only)
    Please see "■PIN DESCRIPTION" to confirm the corresponding pins.

- Multi-function Timer (Max 2unit)

  The Multi-function timer is composed of the following blocks.

  - 16-bit free-run timer × 3ch/unit
  - Input capture × 4ch/unit
  - Output compare × 6ch/unit
  - A/D activating compare × 3ch/unit
  - Waveform generator × 3ch/unit
  - 16-bit PPG timer × 3ch/unit

  The following function can be used to achieve the motor control.

  - PWM signal output function
  - DC chopper waveform output function
  - Dead timer function
  - Input capture function
  - A/D converter activate function
  - DTIF (Motor emergency stop) interrupt function

- Quadrature Position/Revolution Counter (QPRC) (Max 2unit)

  The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

  - The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers

- Dual Timer (32/16bit Down Counter)

  The Dual Timer consists of two programmable 32/16-bit down counters.
  Operation mode is selectable from the followings for each timer channel.

  - Free-running
  - Periodic (=Reload)
  - One-shot

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
1	79	B1	1	1	VCC	-	
2	80	C1	2	2	P50	E	H
					INT00_0		
					AIN0_2		
					SIN3_1		
				-	RTO10_0 (PPG10_0)		
					MADATA00_1		
3	81	C2	3	3	P51	E	H
					INT01_0		
					BIN0_2		
					SOT3_1 (SDA3_1)		
				-	RTO11_0 (PPG10_0)		
					MADATA01_1		
4	82	B3	4	4	P52	E	H
					INT02_0		
					ZIN0_2		
					SCK3_1 (SCL3_1)		
				-	RTO12_0 (PPG12_0)		
					MADATA02_1		
5	83	D1	5	-	P53	E	H
					SIN6_0		
					TIOA1_2		
					INT07_2		
					RTO13_0 (PPG12_0)		
					MADATA03_1		
6	84	D2	6	-	P54	E	I
					SOT6_0 (SDA6_0)		
					TIOB1_2		
					RTO14_0 (PPG14_0)		
					MADATA04_1		

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
55	33	H10	45	37	P13	F	K
					AN03		
					SCK1_1 (SCL1_1)		
					IC01_2		
				-	MAD11_1		
56	34	H9	46	38	P14	F	L
					AN04		
					INT03_1		
					IC02_2		
				-	SIN0_1		
					MAD12_1		
57	35	H7	47	39	P15	F	K
					AN05		
					IC03_2		
				-	SOT0_1 (SDA0_1)		
					MAD13_1		
58	36	G10	48	-	P16	F	K
					AN06		
					SCK0_1 (SCL0_1)		
					MAD14_1		
59	37	G9	49	40	P17	F	L
					AN07		
					SIN2_2		
					INT04_1		
				-	MAD15_1		
60	38	H11	50	41	AVCC	-	
61	39	F11	51	42	AVRH	-	
62	40	G11	52	43	AVSS	-	
63	41	G8	53	44	P18	F	K
					AN08		
					SOT2_2 (SDA2_2)		
				-	MAD16_1		
64	42	F10	54	45	P19	F	K
					AN09		
					SCK2_2 (SCL2_2)		
				-	MAD17_1		
-	-	H8	-	-	VSS	-	

■ SIGNAL DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	-
	ADTG_1		7	85	D3	7	-
	ADTG_2		18	96	F4	13	9
	ADTG_3		94	72	C5	74	58
	ADTG_4		-	-	-	-	-
	ADTG_5		70	48	D11	-	-
	ADTG_6		12	90	E4	12	8
	ADTG_7		30	8	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin ANxx describes ADC ch.xx.	52	30	J11	42	34
	AN01		53	31	J10	43	35
	AN02		54	32	J8	44	36
	AN03		55	33	H10	45	37
	AN04		56	34	H9	46	38
	AN05		57	35	H7	47	39
	AN06		58	36	G10	48	-
	AN07		59	37	G9	49	40
	AN08		63	41	G8	53	44
	AN09		64	42	F10	54	45
	AN10		65	43	F9	55	-
	AN11		66	44	E11	56	-
	AN12		67	45	E10	-	-
	AN13		68	46	F8	-	-
	AN14		69	47	E9	-	-
	AN15		70	48	D11	-	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-
	TIOA0_1		19	97	G3	14	10
	TIOA0_2		85	63	B7	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	22
	TIOB0_1		9	87	E1	9	5
	TIOB0_2		86	64	C7	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-
	TIOA1_1		20	98	H1	15	11
	TIOA1_2		5	83	D1	5	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	23
	TIOB1_1		10	88	E2	10	6
	TIOB1_2		6	84	D2	6	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	7	K5	-	-
	TIOA2_1		21	99	H2	16	12
	TIOA2_2		96	74	C4	76	60
	TIOB2_0	Base timer ch.2 TIOB pin	42	20	K7	32	24
	TIOB2_1		11	89	E3	11	7
	TIOB2_2		95	73	B4	75	59

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 2	SIN2_2	Multifunction serial interface ch.2 input pin	59	37	G9	49	40
	SOT2_2 (SDA2_2)	Multifunction serial interface ch.2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	63	41	G8	53	44
	SCK2_2 (SCL2_2)	Multifunction serial interface ch.2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	64	42	F10	54	45
Multi Function Serial 3	SIN3_1	Multifunction serial interface ch.3 input pin	2	80	C1	2	2
	SIN3_2		39	17	K6	29	-
	SOT3_1 (SDA3_1)	Multifunction serial interface ch.3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	3	81	C2	3	3
	SOT3_2 (SDA3_2)		40	18	J6	30	-
	SCK3_1 (SCL3_1)	Multifunction serial interface ch.3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	82	B3	4	4
	SCK3_2 (SCL3_2)		41	19	L7	31	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	87	65	D7	67	54
	SIN4_1		65	43	F9	55	-
	SIN4_2		82	60	C8	-	-
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	55
	SOT4_1 (SDA4_1)		66	44	E11	56	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	90	68	C6	70	-
	RTS4_1		69	47	E9	-	-
	RTS4_2		86	64	C7	-	-
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	91	69	A5	71	-
	CTS4_1		68	46	F8	-	-
	CTS4_2		85	63	B7	-	-
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	96	74	C4	76	60
	SIN5_2		15	93	F3	-	-
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 1	DTTI1X_0	Input signal of wave form generator to control outputs RTO10 to RTO15 of multi-function timer 1	8	86	D5	8	-
	DTTI1X_1		39	17	K6	29	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	65	D7	67	-
	FRCK1_1		44	22	J7	34	-
	IC10_0	16-bit input capture input pin of multi-function timer 1 ICxx describes channel number.	88	66	A6	68	-
	IC10_1		40	18	J6	30	-
	IC11_0		89	67	B6	69	-
	IC11_1		41	19	L7	31	-
	IC12_0		90	68	C6	70	-
	IC12_1		42	20	K7	32	-
	IC13_0		91	69	A5	71	-
	IC13_1		43	21	H6	33	-
	RTO10_0 (PPG10_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG10 when it is used in PPG 1 output modes.	2	80	C1	2	-
	RTO10_1 (PPG10_1)		27	5	J4	-	-
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG10 when it is used in PPG 1 output modes.	3	81	C2	3	-
	RTO11_1 (PPG10_1)		28	6	L5	-	-
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG12 when it is used in PPG 1 output modes.	4	82	B3	4	-
	RTO12_1 (PPG12_1)		29	7	K5	-	-
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG12 when it is used in PPG 1 output modes.	5	83	D1	5	-
	RTO13_1 (PPG12_1)		30	8	J5	-	-
	RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG14 when it is used in PPG 1 output modes.	6	84	D2	6	-
	RTO14_1 (PPG14_1)		31	9	H5	21	-
	RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG14 when it is used in PPG 1 output modes.	7	85	D3	7	-
	RTO15_1 (PPG14_1)		32	10	L6	22	-

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

・ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

・ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

・ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

・ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

■ HANDLING DEVICES

- Power supply pins

  In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

  Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

- Crystal oscillator circuit

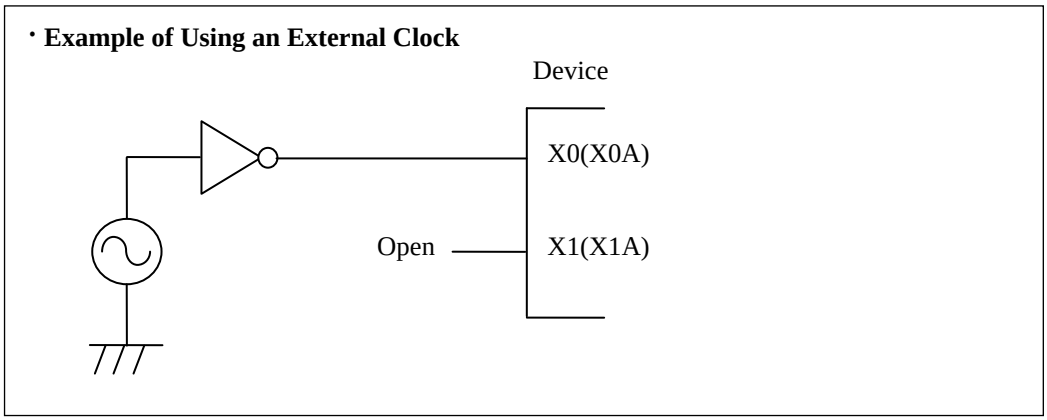
  Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

  It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

- Using an external clock

  When using an external clock, the clock signal should be driven to the X0,X0A pin only and the X1,X1A pin should be kept open.

  ・Example of Using an External Clock



- Handling when using Multi function serial pin as I^2C pin

  If it is using the multi function serial pin as I^2C pins, P-ch transistor of digital output is always disabled. However, I^2C pins need to keep the electrical characteristic like other pins and not to connect to the external I^2C bus system with power OFF.

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enabled	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Hi-Z at transmission / Input enabled/ Internal input fixed at "0" at reception	Hi-Z at transmission / Input enabled/ Internal input fixed at "0" at reception
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/Input enabled

*1 : Oscillation is stopped at sub timer mode, low speed CR timer mode, and stop mode.
*2 : Oscillation is stopped at stop mode.

・ Pin Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

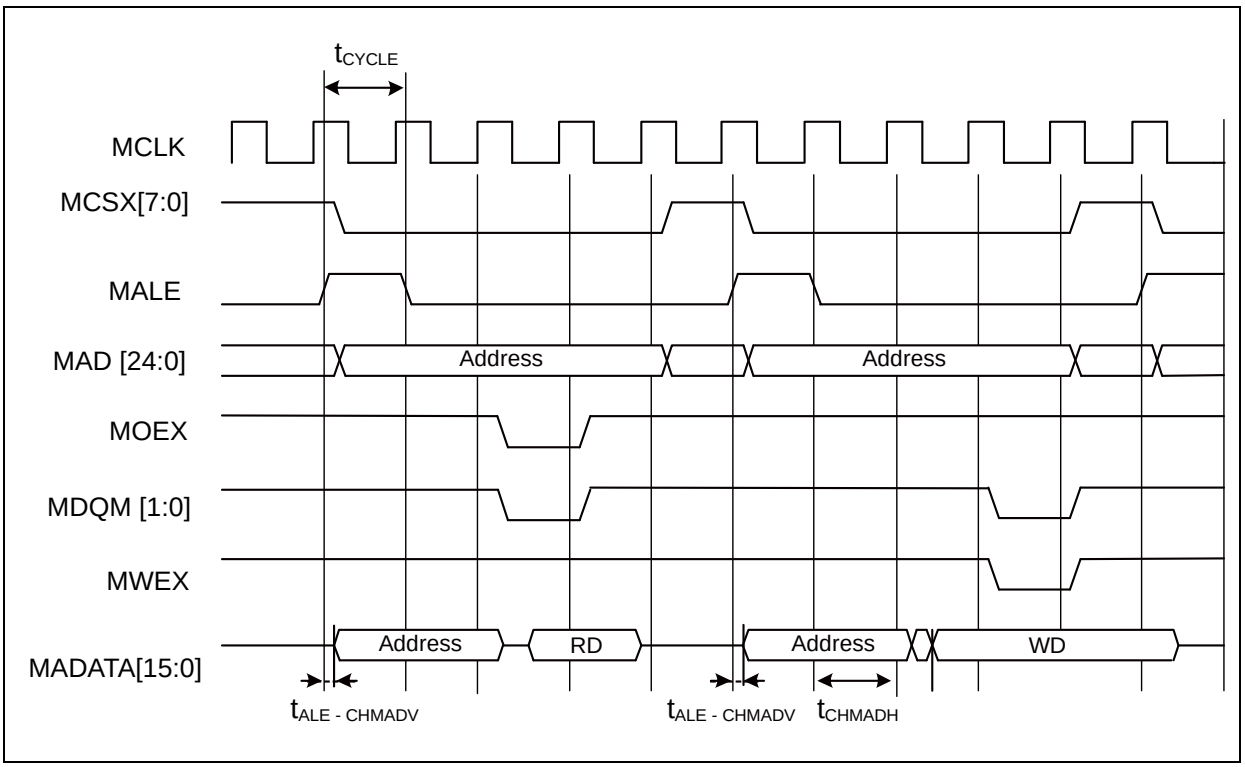
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	Vcc × 0.8	-	Vcc + 0.3	V	
		5V tolerant I/O pin	-	Vcc × 0.8	-	Vss + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	Vss - 0.3	-	Vcc × 0.2	V	
"H" level output voltage	V_{OH}	4mA type	Vcc ≥ 4.5 V I_{OH} = - 4mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 2mA					
		12mA type	Vcc ≥ 4.5 V I_{OH} = - 12mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 8mA					
		The pin doubled as USB I/O	Vcc ≥ 4.5 V I_{OH} = - 20.5mA	Vcc - 0.4	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 13.0mA					
"L" level output voltage	V_{OL}	4mA type	Vcc ≥ 4.5 V I_{OL} = 4mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 2mA					
		12mA type	Vcc ≥ 4.5 V I_{OL} = 12mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 8mA					
		The pin doubled as USB I/O	Vcc ≥ 4.5 V I_{OL} = 18.5mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 10.5mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	Vcc ≥ 4.5 V	25	50	100	kΩ	
			Vcc < 4.5 V	30	80	200		
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

・Multiplexed Bus Access Asynchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed Address delay time	$t_{ALE-CHMADV}$	MALE MADATA[15:0]	Vcc ≥ 4.5V	0	10	ns
			Vcc < 4.5V		20	
Multiplexed Address hold time	t_{CHMADH}		Vcc ≥ 4.5V	MCLK×n+0	MCLK×n+10	ns
			Vcc < 4.5V	MCLK×n+0	MCLK×n+20	

Note: When the external load capacitance C_L = 30pF (m = 0 to 15, n = 1 to 16).

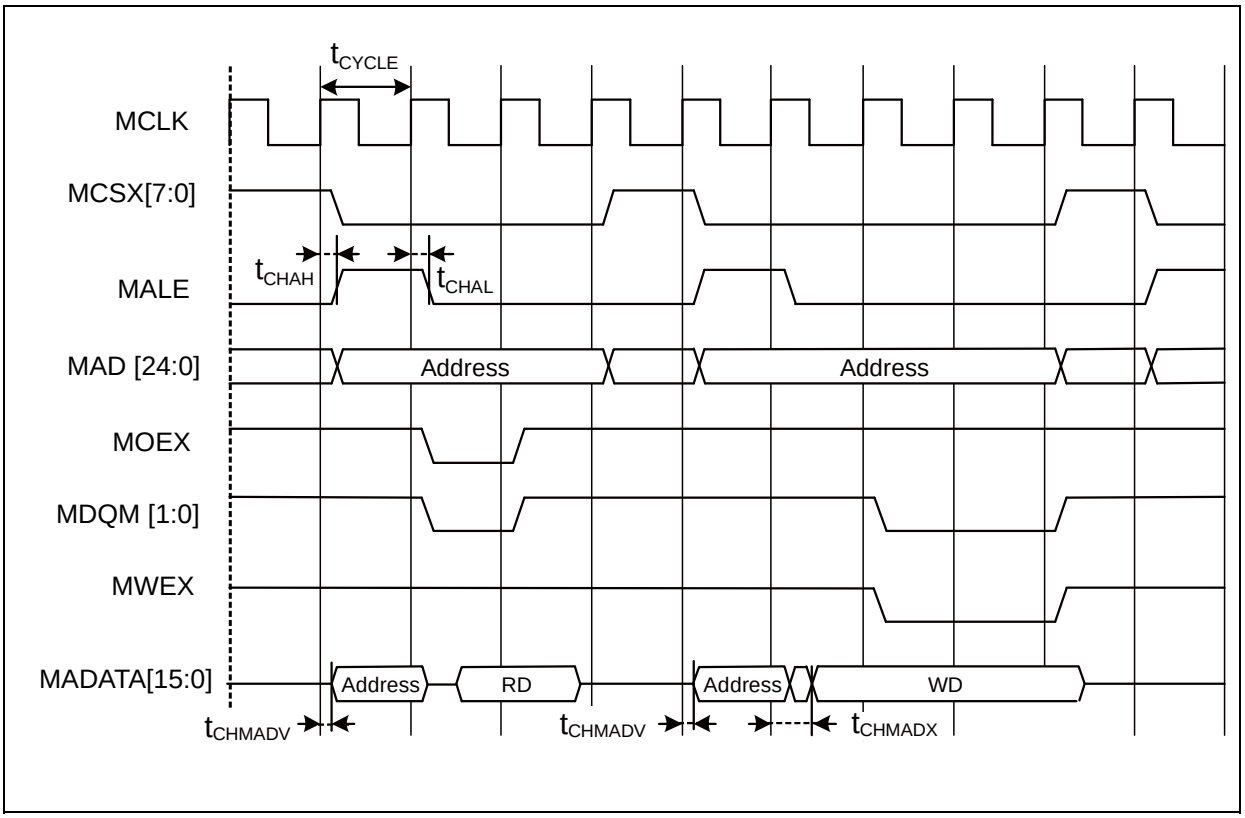


- Multiplexed Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK ALE	Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
	t_{CHAH}		Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				

Note: When the external load capacitance C_L = 30pF.

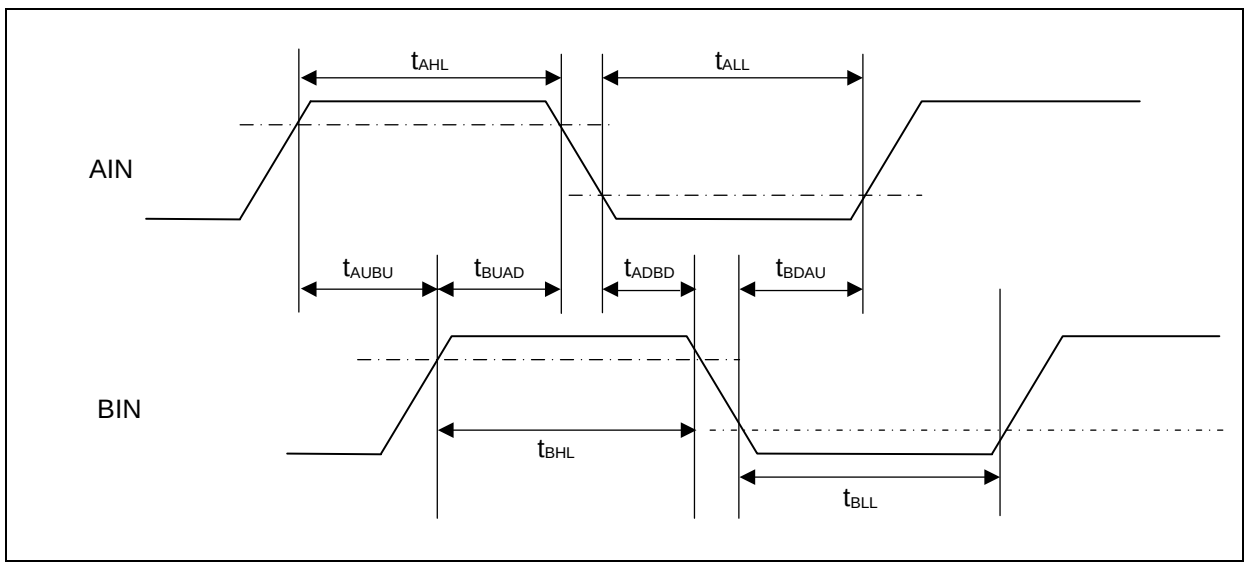


(11) Quadrature Position/Revolution Counter timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

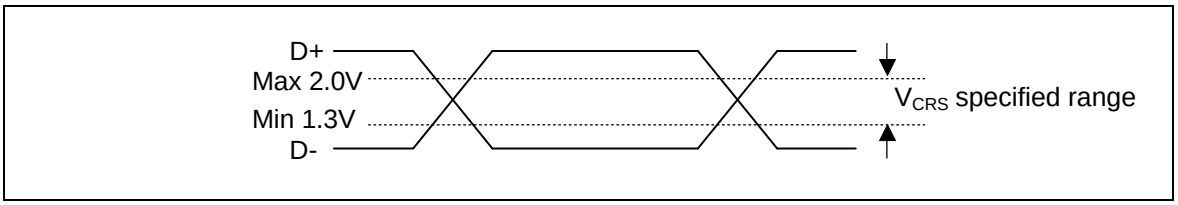
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$ *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC = "1"			

* :t_{CYCP} indicates the APB bus clock cycle time except stop.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "■BLOCK DIAGRAM" in this data sheet.

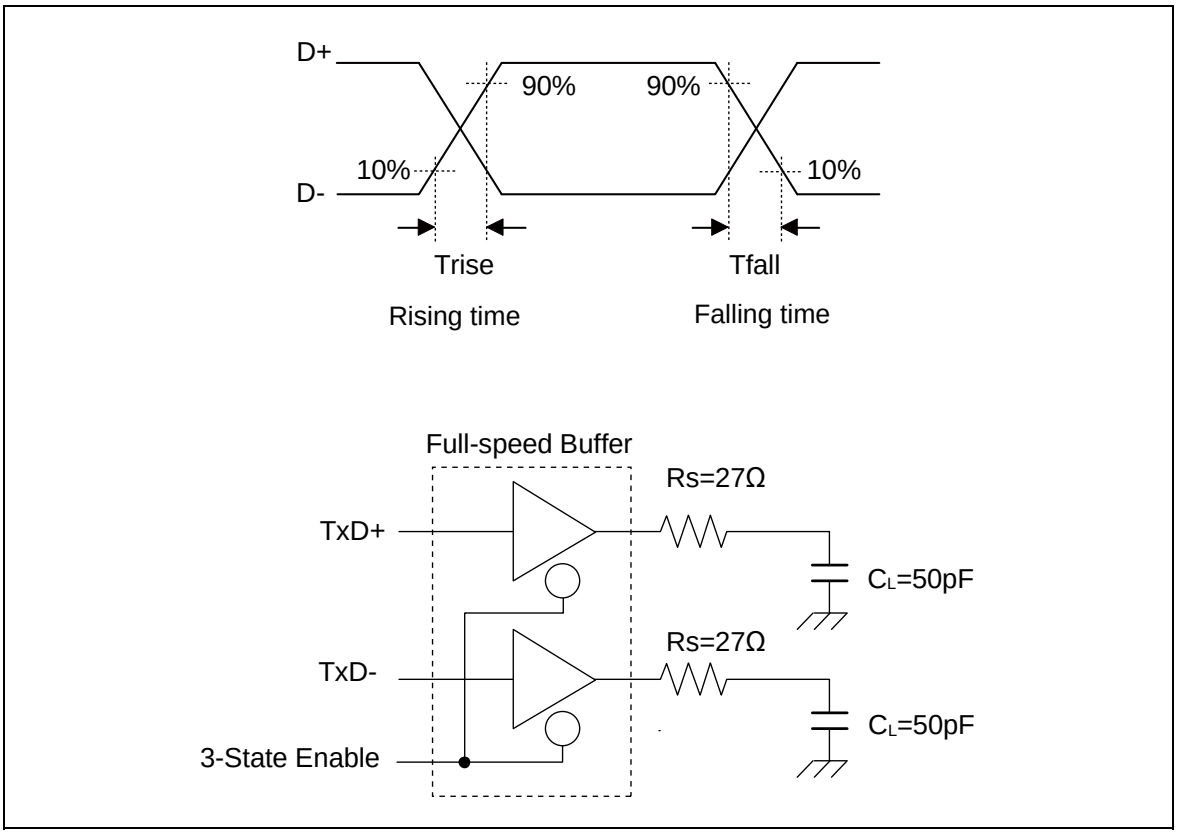


*3 : The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the ground and 1.5 kΩ load) at High-State (V_{OH}).

*4 : The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



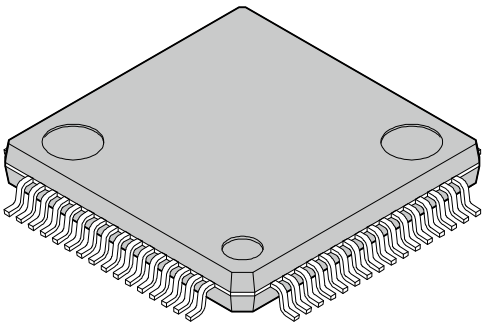
*5 : They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.



■ ORDERING INFORMATION

Part number	Package
MB9AF311LAPMC1	Plastic・LQFP(0.5mm pitch),64-pin (FPT-64P-M24/M38)
MB9AF312LAPMC1	
MB9AF314LAPMC1	
MB9AF311LAPMC	Plastic・LQFP(0.65mm pitch),64-pin (FPT-64P-M23/M39)
MB9AF312LAPMC	
MB9AF314LAPMC	
MB9AF311LAQN	Plastic・QFN(0.5mm pitch),64-pin (LCC-64P-M24)
MB9AF312LAQN	
MB9AF314LAQN	
MB9AF311MAPMC	Plastic・LQFP(0.5mm pitch),80-pin (FPT-80P-M21/M37)
MB9AF312MAPMC	
MB9AF314MAPMC	
MB9AF315MAPMC	
MB9AF316MAPMC	
MB9AF311NAPMC	Plastic・LQFP(0.5mm pitch),100-pin (FPT-100P-M20/M23)
MB9AF312NAPMC	
MB9AF314NAPMC	
MB9AF315NAPMC	
MB9AF316NAPMC	
MB9AF311NAPF	Plastic・QFP(0.65mm pitch), 100-pin (FPT-100P-M06)
MB9AF312NAPF	
MB9AF314NAPF	
MB9AF315NAPF	
MB9AF316NAPF	
MB9AF311NABGL	Plastic・PFBGA(0.8mm pitch),112-pin (BGA-112P-M04)
MB9AF312NABGL	
MB9AF314NABGL	

64-pin plastic LQFP

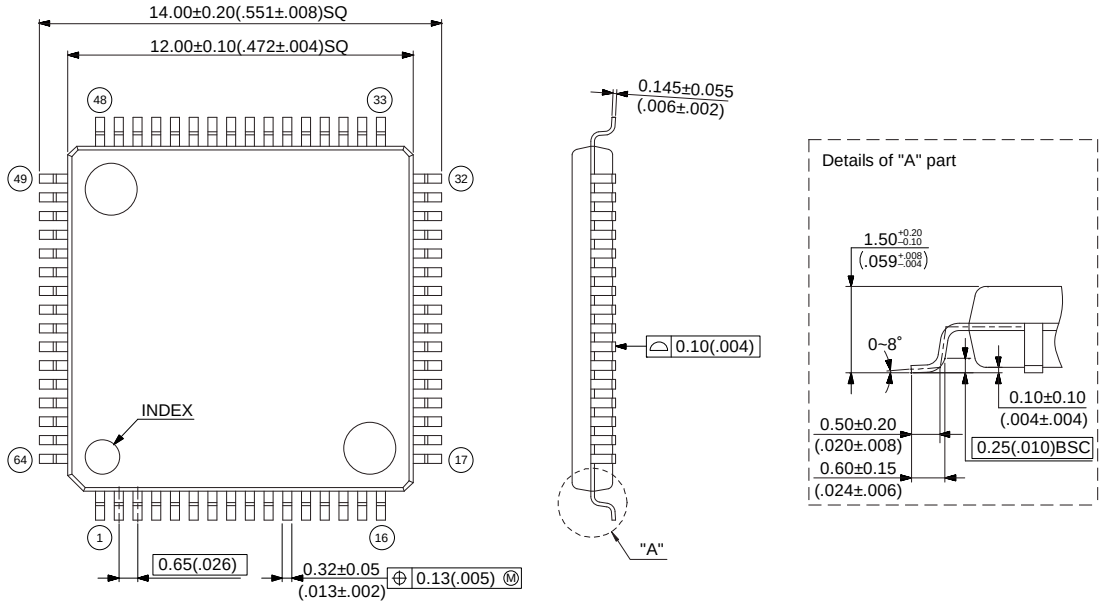


(FPT-64P-M39)

Lead pitch	0.65 mm
Package width × package length	12.00 mm × 12.00 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.47 g

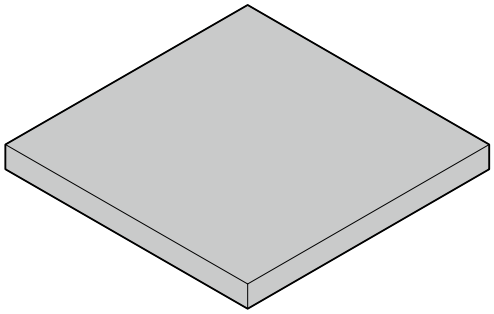
64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.

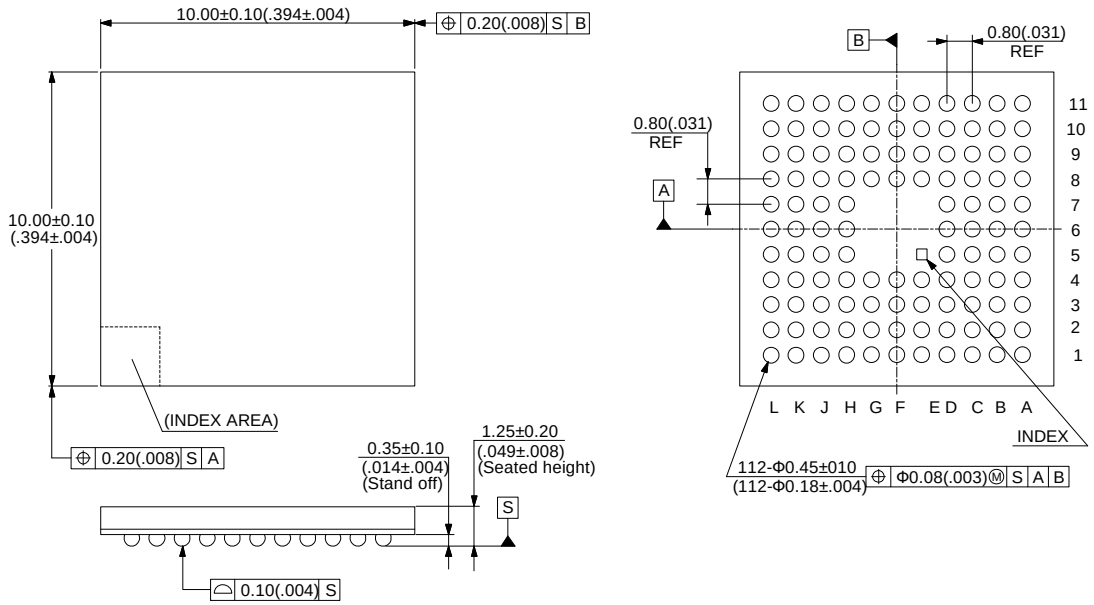


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

112-ball plastic PFBGA		
	Ball pitch	0.80 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Φ 0.45 mm
	Mounting height	1.45 mm Max.
(BGA-112P-M04)	Weight	0.22 g

112-ball plastic PFBGA
(BGA-112P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

Page	Section	Change Results
94	5. 12-bit A/D Converter (1) Electrical characteristics for the A/D converter	・Corrected the value of "Full-scale transition voltage". Min: -20 → AVRH-20 Max: +20 → AVRH+20 ・Corrected the value of "Compare clock cycle". Max: 10000 → 2000 ・Corrected the value of "Reference voltage". Min: AVSS → 2.7

MEMO