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Details

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Product Status	Obsolete
Core Processor	Н8/300Н
Core Size	16-Bit
Speed	13MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	35
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d13007vfi13v

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Preface

The H8/3006 and H8/3007 are a series of high-performance microcontrollers that integrate system supporting functions together with an H8/300H CPU core.

The H8/300H CPU has a 32-bit internal architecture with sixteen 16-bit general registers, and a concise, optimized instruction set designed for speed. It can address a 16-Mbyte linear address space.

The on-chip supporting functions include RAM, 16-bit timers, 8-bit timers, a programmable timing pattern controller (TPC), a watchdog timer (WDT), a serial communication interface (SCI), an A/D converter, a D/A converter, I/O ports, and a DMA controller (DMAC).

The address space is divided into eight areas. The data bus width and access cycle length can be selected independently in each area, simplifying the connection of different types of memory. Four MCU operating modes (modes 1 to 4) are provided, offering a choice of data bus width initial value and address space.

With these features, the H8/3006 and H8/3007 offer easy implementation of compact, high-performance systems.

This manual describes the H8/3006 and H8/3007 Group hardware. For details of the instruction set, refer to the H8/300H Series Software Manual.

Main Revisions for This Edition

All — Company name and brand names amended (Before) Hitachi, Ltd. \rightarrow (After) Renesas Technology Corp. 5.4.2 Interrupt Sequence 102 Figure amended D ₁₅ to D ₀ Figure 5.7 Interrupt Sequence 102 Description and note amended 8.7.2 Register Configuration Table 8.14 Port A Pin Functions (Modes 1 to 4) Description and note amended Bit PWM0 in TMDR, bits IOB2 to IOB0 in TIOR0, bits TPSC2 to TPSC0 in 16TCR2 to 16TCR0 of the 16-bit timer, bit NDER3 in NDERA, and bit PA_0DR select the pin function as follows. PA_JTP_JTIOCB_/TCLKD Notes: 2. TCLKD input when TPSC2 = TPSC1 = TPSC0 = 1 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR2 are as shown in (3) in the table below. PA_JTP_JTIOCA_/TCLKC 275 Table amended PM_VTP_JTIOCA_/TCLKC 275 Table amended PM_VTP_JTIOCA_/TCLKC 275 Table amended PM_VTP_JTIOCA_/TCLKC 275 Table amended Pin Pin Functions and Selection Method (2) in table below. TEGE Table amended (3) in the table below. (2) in table below. TEGE TotCA TOCA input when TPSC2 in TPSC0 in 16TCR2. (2) in table below. TEGE Table amended (1) in table below. (2) in table below. TEGE TotCA input when TPSC2 = TPSC1 = 1 and TPSC	Item	Page	Revisio	on (See Ma	nual fo	r Detai	ls)				
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Table 8.14 Port A Pin Functions (Modes 1 to 4) TPSC0 in 16TCR2 to 16TCR0 of the 16-bit timer, bit SCKS2 to CKS0 in 8TCR2 of the 8-bit timer, bit NDER3 in NDERA, and bit PA_JDDR select the pin function as follows. Notes: 2. TCLKD input when TPSC2 = TPSC1 = TPSC0 = 1 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR2 are as shown in (3) in the table below. PA_/TP_/TIOCA_/TCLKC 275 Table amended Pin Pin Functions and Selection Method PA_/TP_/TIOCA_/TCLKC 275 Table amended Pin Pin Functions and Selection Method PA_/TP_/TIOCA_/TCLKC 275 Table amended Pin Pin Functions and Selection Method PA_/TP_/TOCA_/TCLKC 275 Table amended Pin Pin Functions and Selection Method PA_/TP_/TOCA_/TCLKC 275 Totex in tMDER, and bit PA_DDR select the pin function as follows. TGLKC NDER2 in ADERA, and bit PA_DDR select the bit timer, bit NDERA, and bit PA_DDR select the pin function as follows. TCLKC NDER2 in NDERA, and bit PA_DDR select the bit timer, bit NDEA, and bit PA_DDR select the pin function as follows. TICAA input when IOA2 = 1. 2. Pin function TICCA_ioutput TOCA_ioutput Notes: 1. TICCA input when IOA2 = 1. 2. 1. 10CAC input when	Configuration		Bit PW	M0 in TMDF	R, bits I	OB2 to	IOB0 ir	n TIOR	0, bits T	PSC2 to	
PA_JTP_JTIOCB_JTCLKD Notes: 2. TCLKD input when TPSC2 = TPSC1 = TPSC0 = 1 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR2 are as shown in (3) in the table below. PA_JTP_JTIOCA_JTCLKC 275 Table amended PA_TTP_JTIOCA_JTCLKC 275 Table amended PA_TTP_TIOCA_TCLKC Table amended PA_TTP_TIOCA_TCLKC Table amended PA_TOTY Table amended PA_TOTY Table amended PA_TOTY <td< td=""><td>Table 8.14 Port A Pin Functions (Modes 1 to 4)</td><td></td><td>TPSC0 CKS0 in bit PA₃[</td><td>in 16TCR2 n 8TCR2 of DDR select</td><td>to 16T the 8-b the pin</td><td>CR0 of bit timer function</td><td>the 16- , bit NE n as fol</td><td>·bit time)ER3 in lows.</td><td>er, bits (NDER</td><td>CKS2 to A, and</td></td<>	Table 8.14 Port A Pin Functions (Modes 1 to 4)		TPSC0 CKS0 in bit PA ₃ [in 16TCR2 n 8TCR2 of DDR select	to 16T the 8-b the pin	CR0 of bit timer function	the 16- , bit NE n as fol	·bit time)ER3 in lows.	er, bits (NDER	CKS2 to A, and	
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PA_TP_TIOCA_TCLKC 275 Table amended Pin Pin Functions and Selection Method PA_TP_TIOCA/ TOCA/ TCLKC Bit PVM0 in TMDR, bits IOA2 to IOA0 in TIOR0, bits TPSC2 to TPSC0 in 16TCR2 to 16TCR0 of the 16-bit timer, bits CKS2 to CKS0 in 8TCR0 of the 8-bit timer, bit NDER2 in NDERA, and bit PA_DDR select the pin function as tollows. I6-bit timer (1) in table below (2) in table below PA_DDR - 0 1 NDER2 - - 0 1 PA_DDR - 0 1 1 NDER2 - - 0 1 1 PA_DDR - 0 1 1 1 NDER2 - - 0 1 1 PA_DDR - 0 1 1 1 NDER2 - - 0 1 1 PA_DDR - 0 1 1 1 NDER2 - - 0 1 1 1 Inforce to force to force to force to file CKS0 to file CKS0 in 81CCR0 are as shown in (3) in the ta				8TCR2	are as s	shown i	in (3) in	the tab	ole belo	w.	
Pin Pin Functions and Selection Method PA/TFP/ TIOCA/ TOCK Bit PVM0 in TMDR, bits ICA2 to IOA0 in TIOR0, bits TPSC2 to TSSC0 in BTCR0 of the 8-bit timer, bit NDER2 in NDER4, and bit PA_DDR select the pin function as follows. 16-bit timer settings (1) in table below (2) in table below PA_DDR 0 1 NDER2 0 1 0 0 Notes: 1. TIOCA0 input when IOA2 = 1. 2. CLKC input when IOA2 1 </td <td>PA2/TP2/TIOCA0/TCLKC</td> <td>275</td> <td>Table a</td> <td>mended</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	PA2/TP2/TIOCA0/TCLKC	275	Table a	mended							
PA/TP/ TOCA/ TOCK Bit PWM0 in TMDR, bits IOA2 to IOA0 in TIOR0, bits TPSC2 to TFSC0 in IBTCR2 TOCK Bit CR0 of the f-bit timer, bit NDER2 in NDERA, and bit PA_DDR select the pin function as follows. 16-bit timer NDER2 (1) in table below (2) in table below PA_DDR - 0 1 NDER2 - 0 1 Induction TIOCA, output PA, PA, TP, input output output Induction TIOCA, output PA, output output TOCKA putput output output output output TOCA, output when IOA2 = 1. 2. TOLKC input when IOA2 = 1. 2. TOLKC input when IOA2 = 1. 1. 2. TOLKO input when IOA2 = TSC0 = 0 in any of IBCR0 are as shown in (3) in the table below. 1 - - 16-bit timer channel 0 (2) (1) (2) (1) . . IOA1 0 0			Pin	Pin Functions a	and Selecti	ion Method	l				
16-bit timer channel 0 settings(1) in table below(2) in table belowPA,DDR011NDER201Pin functionTIOCA, outputPA, inputPA, inputTP, outputNotes: 1. TIOCA0 input when IOA2 = 1.2.TCLKC input*2Notes: 1. TIOCA0 input when TPSC2 = TPSC1 = 1 and TPSC0 = 0 in any of 16TCR0, or bits CKS2 to CKS0 in BTCR0 are as shown in (3) in the table below.116-bit timer channel 0(2)(1)(2)(1)PWM001IOA1001IOA101IOA101IOA001ICA1001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001IOA001 <td></td> <td></td> <td>PA_/TP_/ TIOCA_/ TCLKC</td> <td>Bit PWM0 in TM to 16TCR0 of the NDER2 in NDEF</td> <td>DR, bits IO e 16-bit tim RA, and bit</td> <td>A2 to IOA0 er, bits CKS PA₂DDR se</td> <td>in TIOR0, I S2 to CKS0 lect the pin</td> <td>oits TPSC2 in 8TCR0 of function as</td> <td>to TPSC0 i of the 8-bit t follows.</td> <td>n 16TCR2 imer, bit</td>			PA_/TP_/ TIOCA_/ TCLKC	Bit PWM0 in TM to 16TCR0 of the NDER2 in NDEF	DR, bits IO e 16-bit tim RA, and bit	A2 to IOA0 er, bits CKS PA ₂ DDR se	in TIOR0, I S2 to CKS0 lect the pin	oits TPSC2 in 8TCR0 of function as	to TPSC0 i of the 8-bit t follows.	n 16TCR2 imer, bit	
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TIOCA ₀ input ^{®1} TIOCA ₀ input ^{®1} TCLKC input when IOA2 = 1. Notes: 1. TIOCA ₀ input when TPSC2 = TPSC1 = 1 and TPSC0 = 0 in any of IBTCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR0 are as shown in (3) in the table below. 16-bit timer channel 0 (2) (1) (2) (1) PWM0 0 1 IOA2 0 1 IOA2 0 1 IOA2 0 1 IOA2 0 1 IOA3 0 1 IOA3 0 1 IOA3 0 1 IOA3 0 1 IOA3 0 1 IOA3 0 1 IOA3 0 1 -							ut	input	output	output	
FOLKO Input: Information Folkowing Weight When TORS = TPSC1 = 1 and TPSC0 = 0 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR0 are as shown in (3) in the table below. Information Folkowing Weight W								TIOCA ₀ input* ¹			
2. TCLKC input when TPSC2 = TPSC1 = 1 and TPSC0 = 0 in any of 16TCR2 to 16TCR2, or bits CKS2 to CKS0 in 8TCR0 are as shown in (3) in the table below.16-bit timer channel 0 settings(2)(1)(2)(1)PWM001IOA201IOA1001IOA001IOA001ICA1001IOA001ICA001ICA001ICKS201CKS101CKS001				Notes: 1. TIOC	A0 input wł	nen IOA2 =	1.	mput			
$ \begin{array}{ c c c c c c } 16-bit timer \\ channel 0 \\ settings \\ \hline PWM0 \\ \hline DA2 \\ IOA2 \\ IOA2 \\ O \\ I \\ IOA2 \\ O \\ I \\ IOA1 \\ O \\ O \\ I \\ I$				2. TCLK 16TC (3) in	TCLKC input when TPSC2 = TPSC1 = 1 and TPSC0 = 0 in any of 16TCR2 to 16TCR0, or bits CKS2 to CKS0 in 8TCR0 are as show (3) in the table below.			iy of hown in			
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IOA1 0 0 1 IOA0 0 1 B-bit timer channel 0 settings (4) (3) CKS2 0 1 CKS1 0 1 CKS0 0 1				IOA2	0	0	1	1	-	-	
8-bit timer channel 0 settings (4) (3) CKS2 0 1 CKS1 0 1 CKS0 0 1				IOA1 IOA0	0	1	-	_			
CKS2 0 1 CKS1 - 0 1 CKS0 - 0 1				8-bit timer channel 0	(4) (3)						
CKS1 — 0 1 CKS0 — 0 1 —				CKS2	0			1			
CKS0 — 0 1 —				CKS1	—		0		1		
				CKS0		0		1			



2.6 Instruction Set

2.6.1 Instruction Set Overview

The H8/300H CPU has 64 types of instructions, which are classified in table 2.1.

Function	Instruction	Types
Data transfer	MOV, PUSH* ¹ , POP* ¹ , MOVTPE* ² , MOVFPE* ²	5
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, MULXS, DIVXU, DIVXS, CMP, NEG, EXTS, EXTU	18
Logic operations	AND, OR, XOR, NOT	4
Shift operations	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc*3, JMP, BSR, JSR, RTS	5
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	9
Block data transfer	EEPMOV	1

Table 2.1 Instruction Classification

Total 64 types

- Notes: 1. POP.W Rn is identical to MOV.W @SP+, Rn. PUSH.W Rn is identical to MOV.W Rn, @-SP. POP.L ERn is identical to MOV.L @SP+, Rn. PUSH.L ERn is identical to MOV.L Rn, @-SP.
 - 2. Not available in the H8/3006 and H8/3007.
 - 3. Bcc is a generic branching instruction.







2.9.4 Access to External Address Space

The external address space is divided into eight areas (areas 0 to 7). Bus-controller settings determine whether each area is accessed via an 8-bit or 16-bit bus, and whether it is accessed in two or three states. For details see section 6, Bus Controller.

- Burst ROM interface
 - Burst ROM interface can be set for area 0
 - Selection of two- or three-state burst access
- Idle cycle insertion
 - An idle cycle can be inserted in case of an external read cycle between different areas
 - An idle cycle can be inserted when an external read cycle is immediately followed by an external write cycle
- Bus arbitration function
 - A built-in bus arbiter grants the bus right to the CPU, DMAC, DRAM interface, or an external bus master
- Other features
 - The refresh counter (refresh timer) can be used as an interval timer

6.1.2 Block Diagram

Figure 6.1 shows a block diagram of the bus controller.



6. Bus Controller



Figure 6.13 Bus Control Signal Timing for 16-Bit, Two-State-Access Area (2) (Byte Access to Odd Address)

Connection Examples

• Figure 6.29 shows typical interconnections when using two 2-CAS type 16-Mbit DRAMs using a × 16-bit organization, and the corresponding address map. The DRAMs used in this example are of the 10-bit row address × 10-bit column address type. Up to four DRAMs can be connected by designating areas 2 to 5 as DRAM space.



Figure 6.29 Interconnections and Address Map for 2-CAS 16-Mbit DRAMs with × 16-Bit Organization

7.4.6 Block Transfer Mode

In block transfer mode, the A and B channels are combined. One block of a specified size is transferred per request. A designated number of block transfers are executed. Addresses are specified in MARA and MARB. The block area address can be either held fixed or cycled.

Table 7.10 indicates the register functions in block transfer mode.

Table 7.10	Register Functi	ons in Block	Transfer Mode
-------------------	-----------------	--------------	----------------------

Register	Function	Initial Setting	Operation
23 0 MARA	Source address register	Transfer source start address	Incremented or decremented once per transfer, or held fixed
23 0 MARB	Destination address register	Transfer destination start address	Incremented or decremented once per transfer, or held fixed
7 0 ETCRAH	Block size counter	Block size	Decremented once per transfer until H'00 is reached, then reloaded from ETCRL
7 0 ETCRAL	Initial block size	Block size	Held fixed
15 0 ETCRB	Block transfer counter	Number of block transfers	Decremented once per block transfer until H'0000 is reached and the transfer ends

Legend:

MARA: Memory address register A

MARB: Memory address register B

ETCRA: Execute transfer count register A

ETCRB: Execute transfer count register B

The source and destination addresses are both 24-bit addresses. MARA specifies the source address. MARB specifies the destination address. MARA and MARB can be independently incremented, decremented, or held fixed as data is transferred. One of these registers operates as a block area register: even if it is incremented or decremented, it is restored to its initial value at the end of each block transfer. The TMS bit in DTCRB selects whether the block area is the source or destination.

9.2.10 Timer I/O Control Register (TIOR)

TIOR is an 8-bit register. The 16-bit timer has three TIORs, one in each channel.

Channel Abbreviation Function

1 TIOR1 ^{mode.}	0	TIOR0	TIOR controls the general registers. Some functions differ in PWM	
2 TIOR2	1	TIOR1	mode.	
2 11012	2	TIOR2		



Reserved bit

Each TIOR is an 8-bit readable/writable register that selects the output compare or input capture function for GRA and GRB, and specifies the functions of the TIORA and TIORC pins. If the output compare function is selected, TIOR also selects the type of output. If input capture is selected, TIOR also selects the edge or edges of the input capture signal.

TIOR is initialized to H'88 by a reset and in standby mode.

Bit 7—Reserved: This bit cannot be modified and is always read as 1.



16-bit timer Operating Modes

Table 9.7 (a)16-bit timer Operating Modes (Channel 0)

		Register Settings							
		TSNC		TMD	R	TIC	DR0	16TC	R0
Operating Mode		Synchro- nization	MDF	FDIR	PWM	ΙΟΑ	ЮВ	Clear Select	Clock Select
Synchro	nous preset	SYNC0 = 1	_	_	0	0	0	0	0
PWM mode		0	_		PWM0 = 1	_	0*	0	0
Output compare A		0	—	—	PWM0 = 0	IOA2 = 0 Other bits unrestricted	0	0	0
Output compare B		0	—	—	0	0	IOB2 = 0 Other bits unrestricted	0	0
Input capture A		0	_	_	PWM0 = 0	IOA2 = 1 Other bits unrestricted	0	0	0
Input capture B		0	_		PWM0 = 0	0	IOB2 = 1 Other bits unrestricted	0	0
Counter clearing	By compare match/input capture A	0	_		0	0	0	CCLR1 = 0 CCLR0 = 1	0
	By compare match/input capture B	0	_		0	0	0	CCLR1 = 1 CCLR0 = 0	0
	Syn- chronous clear	SYNC0 = 1	—	—	0	0	0	CCLR1 = 1 CCLR0 = 1	0

Legend:

• Setting available (valid)

- Setting does not affect this mode

Note: * The input capture function cannot be used in PWM mode. If compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

12.2.2 Timer Control/Status Register (TCSR)

TCSR is an 8-bit readable and writable register. Its functions include selecting the timer mode and clock source.



Status flag indicating overflow

Notes: TCSR is write-protected by a password. For details see section 12.2.4, Notes on Register Access.

* Only 0 can be written, to clear the flag.

Bits 7 to 5 are initialized to 0 by a reset and in standby mode. Bits 2 to 0 are initialized to 0 by a reset. In software standby mode bits 2 to 0 are not initialized, but retain their previous values.

Bit 7—Overflow Flag (OVF): This status flag indicates that the timer counter has overflowed from H'FF to H'00.

Bit 7 OVF	Description	
0	[Clearing condition]	(Initial value)
	Cleared by reading OVF when $OVF = 1$, then writing 0 in OVF	
1	[Setting condition]	
	Set when TCNT changes from H'FF to H'00	

Bit 5—Overrun Error (ORER): Indicates that data reception ended abnormally due to an overrun error.

Bit 5			
ORER		Description	
0		Receiving is in progress or has ended normally*1	(Initial value)
		[Clearing conditions]	
		The chip is reset or enters standby mode	
		 Read ORER when ORER = 1, then write 0 in ORER 	
1		A receive overrun error occurred* ²	
		[Setting condition]	
		Reception of the next serial data ends when RDRF = 1	
Notes:	1.	Clearing the RE bit to 0 in SCR does not affect the ORER flag, which reta previous value.	ains its
	2.	RDR continues to hold the receive data prior to the overrun error, so substreceive data is lost. Serial receiving cannot continue while the ORER flag synchronous mode, serial transmitting is also disabled.	sequent is set to 1. In

Bit 4—Framing Error (FER)/Error Signal Status (ERS): The function of this bit differs for the normal serial communication interface and for the smart card interface. Its function is switched with the SMIF bit in SCMR.

For serial communication interface (SMIF bit in SCMR cleared to 0): Indicates that data reception ended abnormally due to a framing error in asynchronous mode.

Bit 4 FER		Description	
0		Receiving is in progress or has ended normally*1	(Initial value)
		[Clearing conditions]	
		The chip is reset or enters standby mode	
		• Read FER when FER = 1, then write 0 in FER	
1		A receive framing error occurred	
		[Setting condition]	
		The stop bit at the end of the receive data is checked and fou	ind to be 0*2
Notes:	1.	Clearing the RE bit to 0 in SCR does not affect the FER flag, which re value.	tains its previous
	2.	When the stop bit length is 2 bits, only the first bit is checked. The sec checked. When a framing error occurs the SCI transfers the receive d does not set the RDRF flag. Serial receiving cannot continue while the to 1. In synchronous mode, serial transmitting is also disabled.	cond stop bit is not ata into RDR but e FER flag is set



Table 20.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 5.5 V, AVCC = 2.7 to 5.5 V, VREF = 2.7 V to AVCC*1, VSS = AVSS = $0 V^{*1}$, Ta = -20° C to +75°C (regular specifications), Ta = -40° C to +85°C (wide-range specifications)

Item		Symbol	Min	Тур	Max	Unit	Test Conditions
Schmitt	Port A,	V_	$V_{cc} imes 0.2$		_	V	
trigger input	$P8_2$ to $P8_0$	V_{T}^{+}	_		$V_{cc} imes 0.7$	V	-
voltages		$V_{_{T}}^{^{+}}-V_{_{T}}^{^{-}}$	$V_{cc} imes 0.07$	_		V	-
Input high voltage	$\frac{\overline{\text{RES}}, \overline{\text{STBY}},}{\text{NMI}, \text{MD}_2 \text{ to}}$	V _{IH}	$V_{cc} \times 0.9$	_	V _{cc} +0.3	V	
	EXTAL		$V_{cc} imes 0.7$	_	V _{cc} +0.3	V	-
	Port 7		$V_{cc} imes 0.7$		AV _{cc} +0.3	V	-
	Ports 4, 6, P8 ₃ , P8 ₄ , P9 ₅ to P9 ₀ , port B, D ₁₅ to D ₈		$V_{cc} \times 0.7$		V _{cc} +0.3	V	
Input low voltage	$\overline{\text{RES}}, \overline{\text{STBY}}, \\ \text{MD}_2 \text{ to } \text{MD}_0$	V _{IL}	-0.3		$V_{cc} imes 0.1$	V	
	NMI, EXTAL, Ports 4, 6, 7, D_{15} to D_8		-0.3		$V_{cc} \times 0.2$	V	V _{cc} < 4.0 V
	P8 ₃ , P8 ₄ , P9 ₅ to P9 ₀ , port B				0.8	V	V_{cc} = 4.0 to 5.5 V
Output high	All output pins	V _{OH}	V _{cc} –0.5		_	V	I _{OH} = -200 μA
voltage	(except RESO)		V _{cc} -1.0	_	_	V	I _{он} = —1 mA
Output low voltage	All output pins (except RESO)	$V_{\rm ol}$	_	—	0.4	V	I _{oL} = 1.6 mA
	A ₁₉ to A ₀				1.0	V	$I_{oL} = 5 \text{ mA}$ ($V_{cc} < 4.0 \text{ V}$) $I_{oL} = 10 \text{ mA}$ ($V_{cc} = 4.0 \text{ to}$ 5.5 V)
	HESU		_		0.4	v	і _{ог} = 1.6 mA



Figure 20.16 DRAM Bus Timing (Self-Refresh)

20.3.5 TPC and I/O Port Timing

Figure 20.17 shows the TPC and I/O port input/output timing.



Figure 20.17 TPC and I/O Port Input/Output Timing

20.3.6 Timer Input/Output Timing

The timings of 16-bit and 8-bit timer are shown as follows:

• Timer input/output timing

Figure 20.18 shows the timer input/output timing.

• Timer external clock input timing Figure 20.19 shows the timer external clock input timing.







Figure 20.19 Timer External Clock Input Timing

Appendix A Instruction Set

A.1 Instruction List

Operand Notation

Symbol	Description				
Rd	General destination register				
Rs	General source register				
Rn	General register				
ERd	General destination register (address register or 32-bit register)				
ERs	General source register (address register or 32-bit register)				
ERn	General register (32-bit register)				
(EAd)	Destination operand				
(EAs)	Source operand				
PC	Program counter				
SP	Stack pointer				
CCR	Condition code register				
Ν	N (negative) flag in CCR				
Z	Z (zero) flag in CCR				
V	V (overflow) flag in CCR				
С	C (carry) flag in CCR				
disp	Displacement				
\rightarrow	Transfer from the operand on the left to the operand on the right, or transition from the state on the left to the state on the right				
+	Addition of the operands on both sides				
-	Subtraction of the operand on the right from the operand on the left				
×	Multiplication of the operands on both sides				
÷	Division of the operand on the left by the operand on the right				
^	Logical AND of the operands on both sides				
V	Logical OR of the operands on both sides				
\oplus	Exclusive logical OR of the operands on both sides				
7	NOT (logical complement)				
(), <>	Contents of operand				
Note: General registers include 8-bit registers (R0H to R7H and R0L to R7L) and 16-bit registers					

(R0 to R7 and E0 to E7).

4. Shift instructions

			A Inst	ddr truc	essi tion	ng I Ler	Moc ngth	le a 1 (by	nd /tes)									No Stat	. of tes* ¹
	erand Size			ERn	d, ERn)	-ERn/@ERn+	8	d, PC)	ଥି ଗଣ					Con	diti	on C	ode	e	rmal	vanced
Mnemonic	d	¢	R	0	0	0	03	0	0		Operation		I	н	Ν	z	v	С	۶	Ad
SHAL.B Rd	В		2										_		\$	\$	¢	\$	2	2
SHAL.W Rd	W		2									0	_	_	¢	\$	¢	\$	2	2
SHAL.L ERd	L		2								MSB	LSB	—	—	¢	¢	¢	¢	2	
SHAR.B Rd	В		2										_		\$	\$	0	\$	2	2
SHAR.W Rd	W		2] [1]		_	—	\$	\$	0	\$	2	2
SHAR.L ERd	L		2								MSB	LSB	_	—	\$	\$	0	¢	2	2
SHLL.B Rd	В		2										_		≎	\$	0	\$	2	2
SHLL.W Rd	W		2									0	_		\$	\$	0	¢	2	2
SHLL.L ERd	L		2								MSB	LSB	_	—	\$	\$	0	¢	2	2
SHLR.B Rd	В		2										_	_	\$	\$	0	¢	2	2
SHLR.W Rd	W		2								0-	► C	—	—	\$	\$	0	¢	2	2
SHLR.L ERd	L		2								MSB	LSB	_	—	\$	\$	0	¢	2	2
ROTXL.B Rd	В		2										_	_	\$	\$	0	¢	2	2
ROTXL.W Rd	W		2									*	_	—	¢	¢	0	¢	2	2
ROTXL.L ERd	L		2								MSB ◄	- LSB	_	—	¢	¢	0	¢	2	2
ROTXR.B Rd	В		2										_	_	\$	\$	0	¢	2	2
ROTXR.W Rd	W		2										_		\$	\$	0	¢	2	2
ROTXR.L ERd	L		2								MSB	SB	_	—	\$	\$	0	¢	2	2
ROTL.B Rd	В		2										_		≎	\$	0	\$	2	2
ROTL.W Rd	W		2									*	_		\$	\$	0	¢	2	2
ROTL.L ERd	L		2								MSB 🔫	- LSB	—	—	\$	\$	0	¢	2	2
ROTR.B Rd	В		2										_	_	\$	\$	0	\$	2	2
ROTR.W Rd	W		2									►C	_	_	\$	\$	0	\$	2	2
ROTR.L ERd	L		2								MSB	LSB	_	_	\$	\$	0	\$	2	2

		Addressing Mode and Instruction Length (bytes)							nd /tes)								No. of States* ¹		
Mnemonic	Operand Size	#xx	Rn	@ERn	@(d, ERn)	@-ERn/@ERn+	@aa	@(d, PC)	ଡ ଡ ଅଣ		Operation	Condition Code			e	Normal	Advanced			
BLD #xx:3, @ERd	в			4							(#xx:3 of @ERd) \rightarrow C			_	_		¢	e	6	
BLD #xx:3, @aa:8	В						4				(#xx:3 of @aa:8) → C	_	_	_	_	_	\$	e	6	
BILD #xx:3, Rd	в		2								\neg (#xx:3 of Rd8) \rightarrow C			_	_		\$	2		
BILD #xx:3, @ERd	в			4							\neg (#xx:3 of @ERd) \rightarrow C	_	_	_	_	_	\$	6		
BILD #xx:3, @aa:8	в						4				\neg (#xx:3 of @aa:8) \rightarrow C	_	_	_	_	_	¢	6		
BST #xx:3, Rd	в		2								$C \rightarrow (\#xx:3 \text{ of } Rd8)$	—	_	—	—	—	—	2	2	
BST #xx:3, @ERd	в			4							$C \rightarrow (\#xx:3 \text{ of } @ERd24)$	—	—	_	—	—	—	8	3	
BST #xx:3, @aa:8	в						4				$C \rightarrow (\#xx:3 \text{ of } @aa:8)$	_	_			_		8	3	
BIST #xx:3, Rd	в		2								$\neg C \rightarrow (\#xx:3 \text{ of } Rd8)$	—	—	—	—	—	—	2	2	
BIST #xx:3, @ERd	в			4							$\neg C \rightarrow (\#xx:3 \text{ of } @ERd24)$	—	—	—	—	—	—	8	3	
BIST #xx:3, @aa:8	в						4				$\neg C \rightarrow (\#xx:3 \text{ of } @aa:8)$			—	—		—	8	3	
BAND #xx:3, Rd	В		2								$C {\wedge} (\#xx:3 \text{ of } Rd8) \to C$	—	—		—	—	\$	2		
BAND #xx:3, @ERd	В			4							$C {\wedge} (\#xx:3 \text{ of } @ERd24) \rightarrow C$	—	—	—	—	—	\$	e	5	
BAND #xx:3, @aa:8	В						4				$C {\wedge} (\#xx:3 \text{ of } @aa:8) \rightarrow C$						\$	6	5	
BIAND #xx:3, Rd	В		2								$C {\wedge} \neg (\#xx:3 \text{ of } Rd8) \rightarrow C$	—	—		—	—	\$	2		
BIAND #xx:3, @ERd	В			4							$C \land \neg$ (#xx:3 of @ERd24) \rightarrow C	—	—	—	—	—	\$	6	3	
BIAND #xx:3, @aa:8	В						4				$C {\wedge} \neg (\#xx:3 \text{ of } @ aa:8) \rightarrow C$	_	_	_	_	_	€	e	5	
BOR #xx:3, Rd	в		2								$C{\scriptstyle\lor}(\texttt{\#xx:3 of Rd8})\rightarrow C$	—	—	—	—	—	¢	2	2	
BOR #xx:3, @ERd	В			4							$C{\scriptstyle\vee}(\texttt{\#xx:3 of @ERd24})\rightarrowC$	—	—	—	—	—	\$	6	3	
BOR #xx:3, @aa:8	в						4				$C \lor (\#xx:3 \text{ of } @aa:8) \rightarrow C$	—	—	_	—	—	¢	e	3	
BIOR #xx:3, Rd	в		2								$C \lor \neg$ (#xx:3 of Rd8) \rightarrow C	—	—	_	_	—	¢	2	2	
BIOR #xx:3, @ERd	в			4							$C \lor \neg$ (#xx:3 of @ERd24) \rightarrow C	—	—		—	—	¢	6	3	
BIOR #xx:3, @aa:8	в						4				$C \lor \neg$ (#xx:3 of @aa:8) $\rightarrow C$	—	—	—	—	—	\$	6	3	
BXOR #xx:3, Rd	В		2								$C {\oplus} (\#xx:3 \text{ of } Rd8) \to C$	_	_	_	_	_	\$	2	2	
BXOR #xx:3, @ERd	В			4							C⊕(#xx:3 of @ERd24) → C	_	_	-	_	_	\$	6		
BXOR #xx:3, @aa:8	в						4				C⊕(#xx:3 of @aa:8) → C	_	_	_	_	_	\$	6		
BIXOR #xx:3, Rd	В		2								C⊕¬(#xx:3 of Rd8) → C	—	—	-	-	—	\$	2		
BIXOR #xx:3, @ERd	В			4							C⊕¬(#xx:3 of @ERd24) → C	_	_	_	_	_	\$	6	3	
BIXOR #xx:3, @aa:8	В						4				$C \oplus \neg (\#xx:3 \text{ of } @aa:8) \rightarrow C$	—	—			—	\$	6	3	



0	Normal operation selected for channel 2 (Initial value)
1	Phase counting mode selected for channel 2

