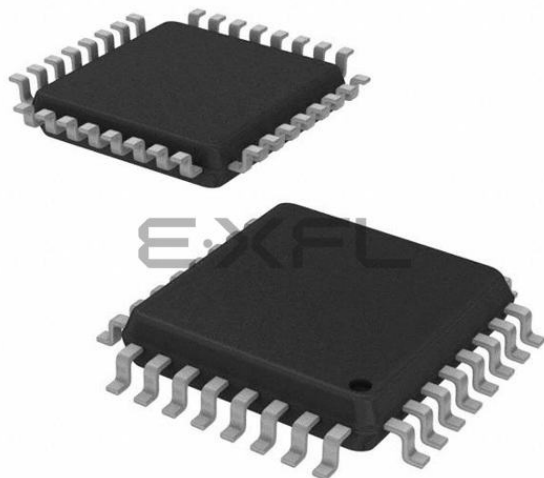




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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa8avlc

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PA16 and PA8.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA (V) B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	MC = fully qualified, general market flow
9	Memory	9 = flash based
S08	Core	S08 = 8-bit CPU
PA	Device family	PA
AA	Approximate flash size in KB	16 = 16 KB 8 = 8 KB
(V)	Mask set version	(blank) = Any version - A = Rev. 2 or later version, this is recommended for new design

Table continues on the next page...

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, XTAL, or true open drain pin PTA2 and PTA3)	-0.3	$V_{DD} + 0.3$	V
	Digital input voltage (true open drain pin PTA2 and PTA3)	-0.3	6	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. All digital I/O pins, except open-drain pin PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} . PTA2 and PTA3 is only clamped to V_{SS} .

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	—	V
	C		High current drive pins, high-drive strength ²	5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	—	V

Table continues on the next page...

6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V _{POR}	D	POR re-arm voltage ^{1, 2}		1.5	1.75	2.0	V
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

- Maximum is highest voltage that POR is guaranteed.
- POR ramp time must be longer than 20us/V to get a stable startup.
- Rising thresholds are falling threshold + hysteresis.
- Voltage factory trimmed at $V_{DD} = 5.0$ V, Temp = 25 °C

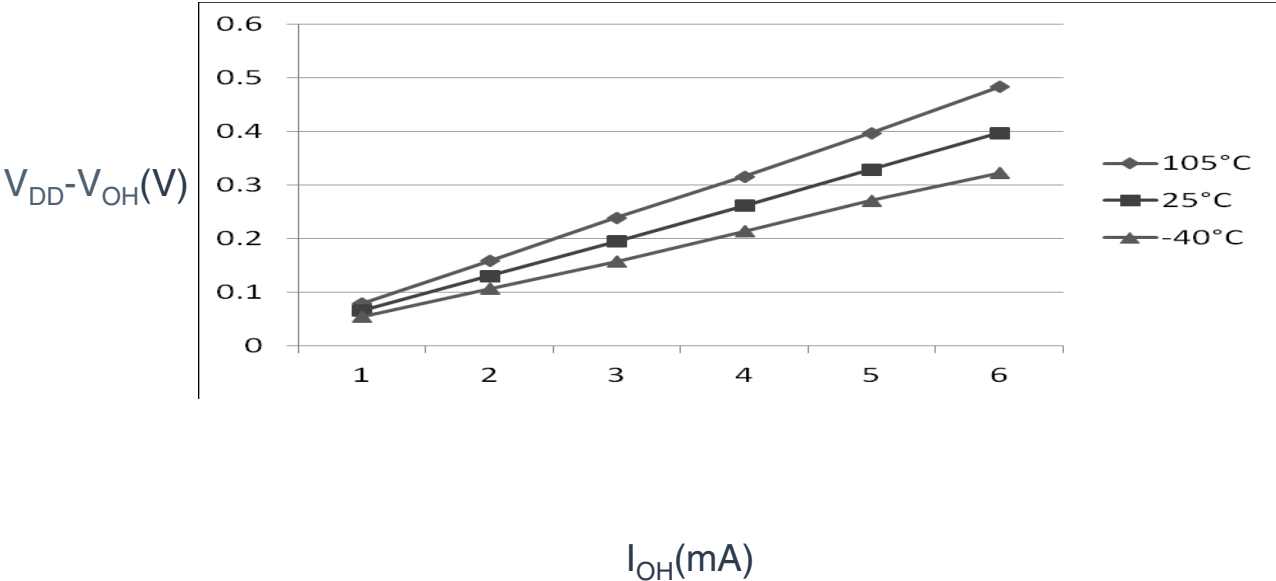


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

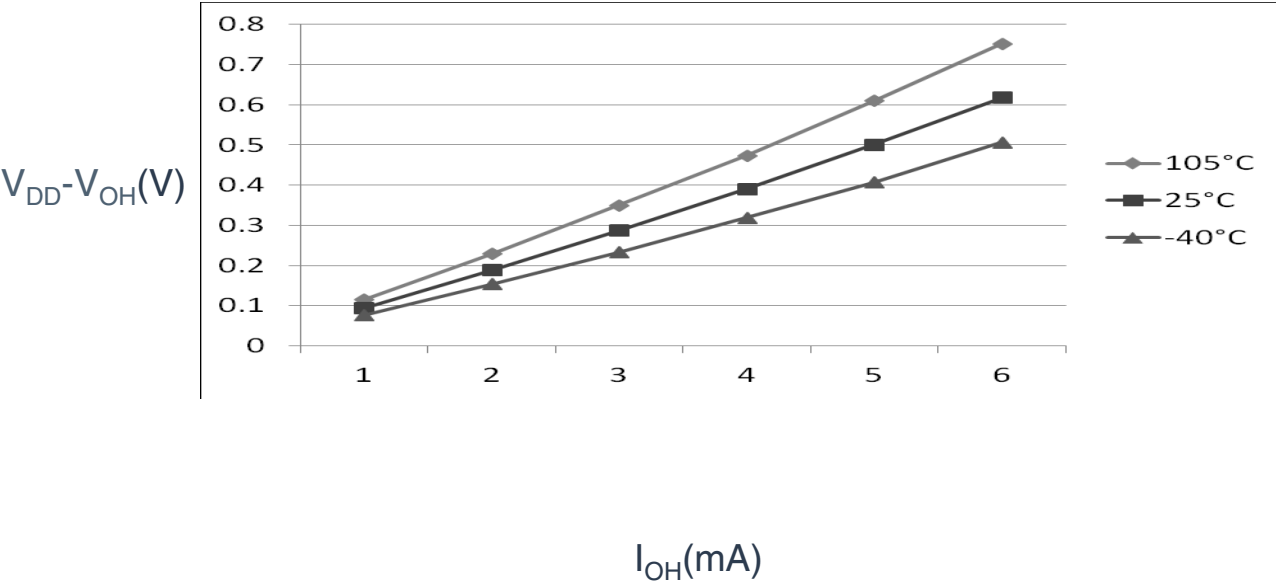


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

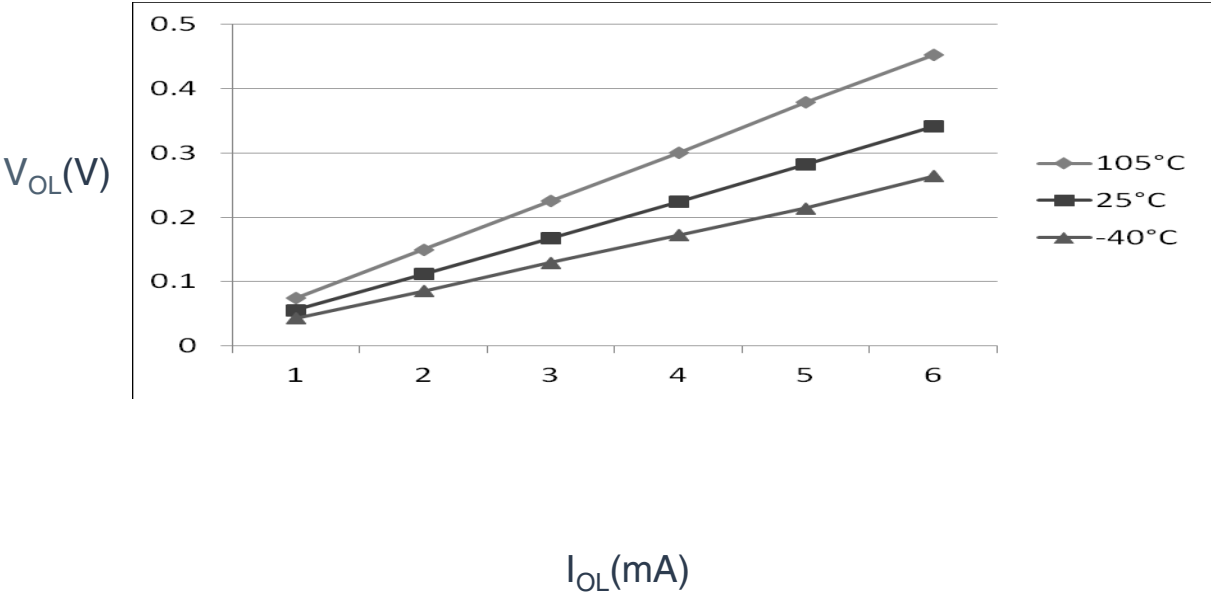


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5$ V)

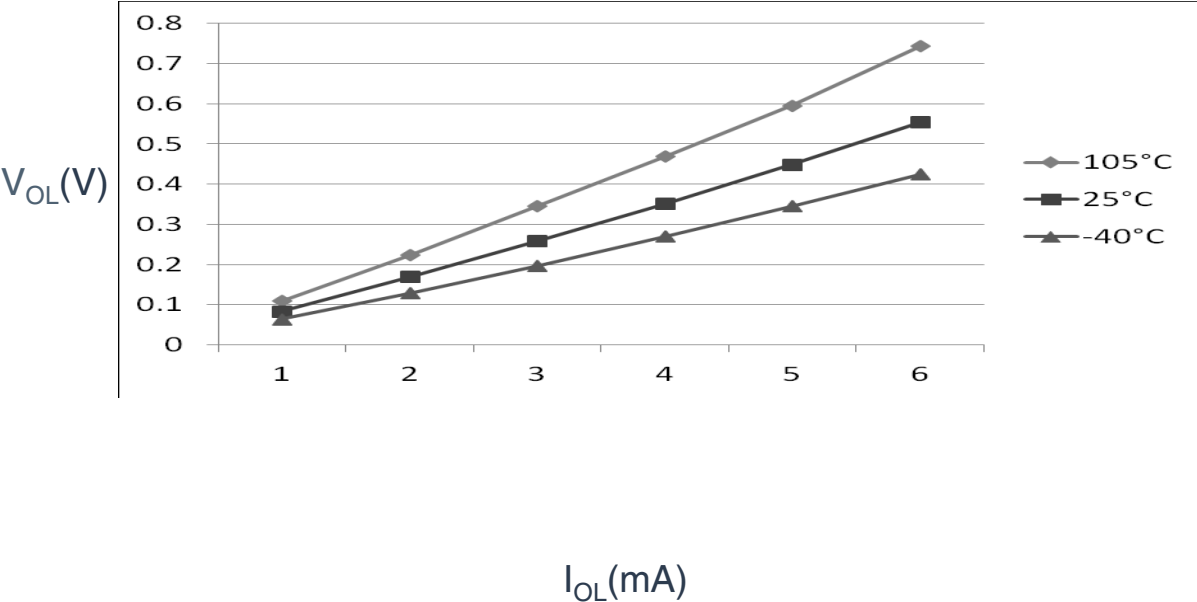


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3$ V)

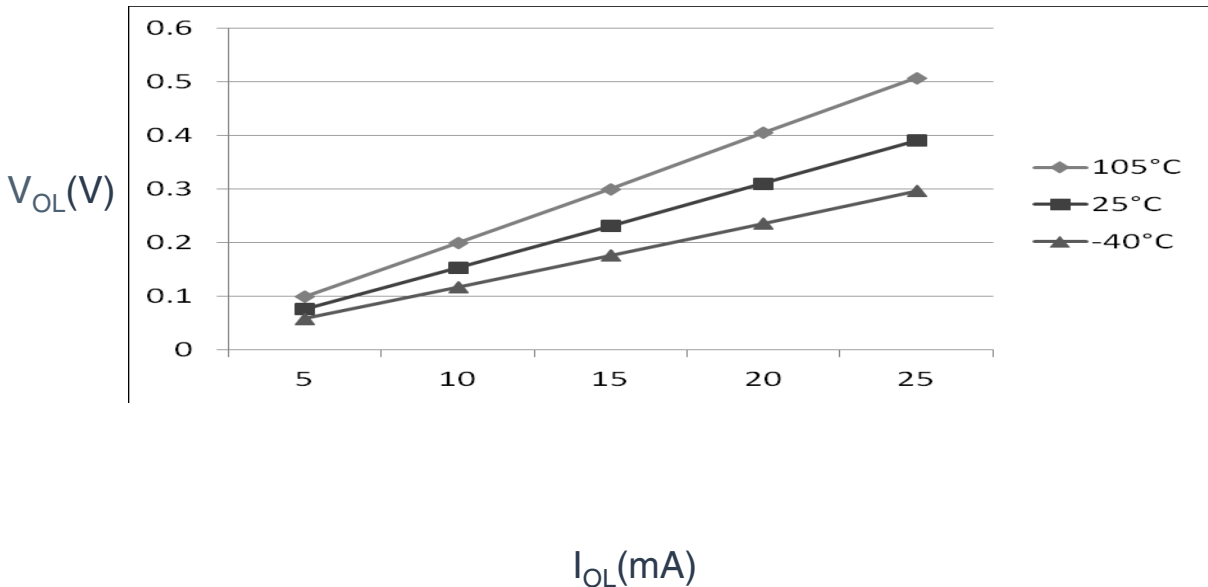


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

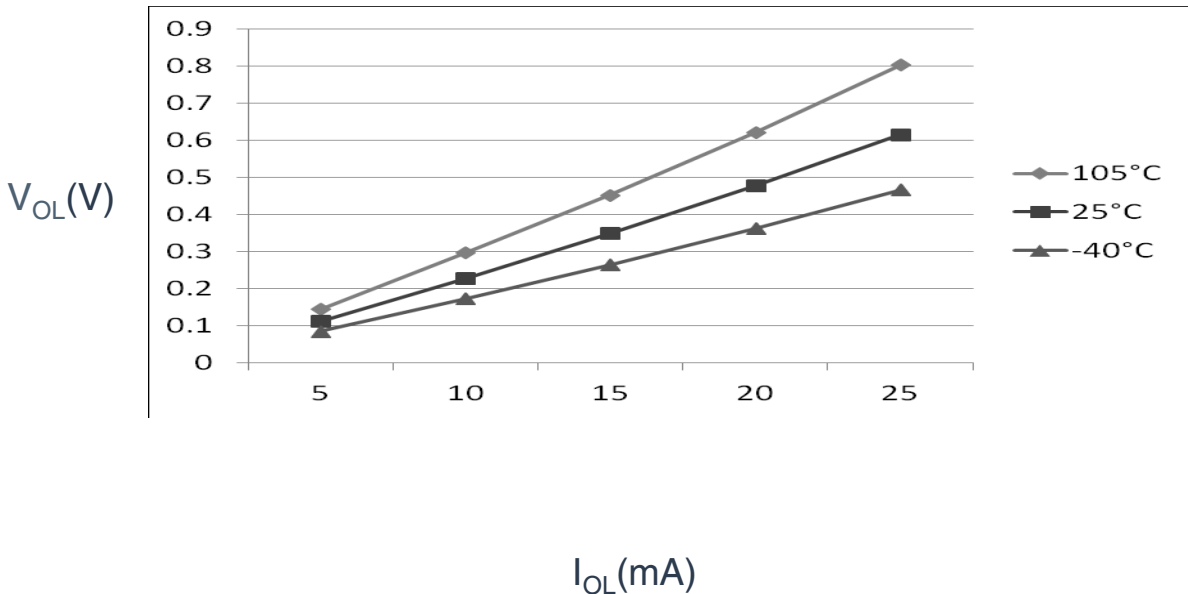


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	7.60	—	mA	-40 to 105 °C
	C			10 MHz		4.65	—		
	C			1 MHz		1.90	—		
	C			20 MHz	3	7.05	—		
	C			10 MHz		4.40	—		
	C			1 MHz		1.85	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	5.88	—	mA	-40 to 105 °C
	C			10 MHz		3.70	—		
	C			1 MHz		1.85	—		
	C			20 MHz	3	5.35	—		
	C			10 MHz		3.42	—		
	C			1 MHz		1.80	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	10.9	14.0	mA	-40 to 105 °C
	C			10 MHz		6.10	—		
	C			1 MHz		1.69	—		
	P			20 MHz	3	8.18	—		
	C			10 MHz		5.14	—		
	C			1 MHz		1.44	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	8.50	13.0	mA	-40 to 105 °C
	C			10 MHz		5.07	—		
	C			1 MHz		1.59	—		
	P			20 MHz	3	6.11	—		
	C			10 MHz		4.10	—		
	C			1 MHz		1.34	—		
5	P	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	5.95	—	mA	-40 to 105 °C
	C			10 MHz		3.50	—		
	C			1 MHz		1.24	—		
	C			20 MHz	3	5.45	—		
	C			10 MHz		3.25	—		
	C			1 MHz		1.20	—		
6	C	Stop3 mode supply current no clocks active (except 1kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	4.6	—	μA	-40 to 105 °C
	C			—	3	4.5	—		-40 to 105 °C
7	C	ADC adder to stop3	—	—	5	40	—	μA	-40 to 105 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	LVD adder to stop3 ⁴	—	—	5	128	—	μA	-40 to 105 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

Table 5. EMC radiated emissions operating behaviors for 44-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	8	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	8	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	8	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 20 MHz, f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

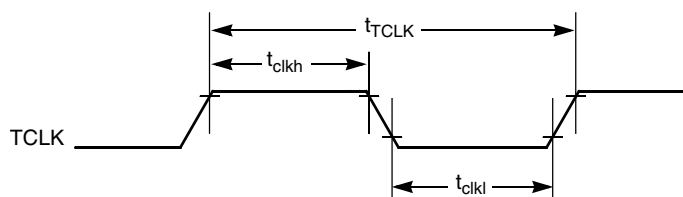


Figure 13. Timer external clock

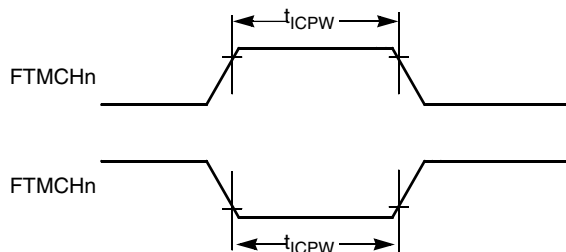


Figure 14. Timer input capture pulse

6.3 Analog

6.3.1 ADC characteristics

Table 12. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
ADC conversion clock frequency	8-bit mode (all valid f_{ADCK})		—	—	10		
	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

6.3.2 Analog comparator (ACMP) electricals

Table 14. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted, and 100 pF load on all SPI pins. All timing assumes high drive strength is enabled for SPI output pins.

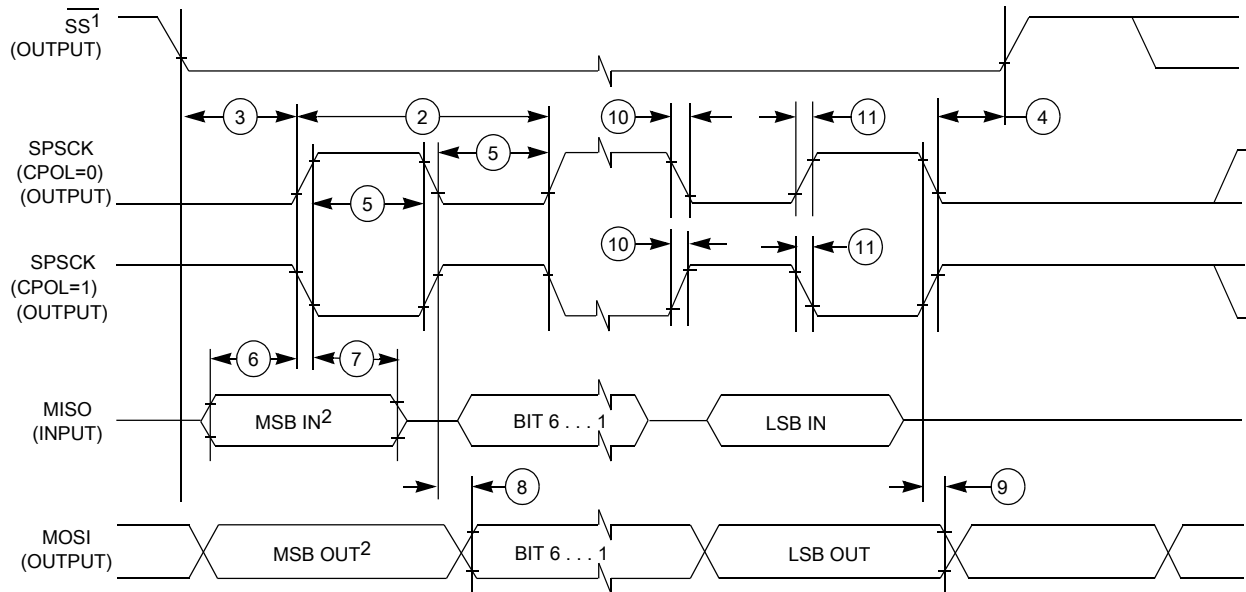
Table 15. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—

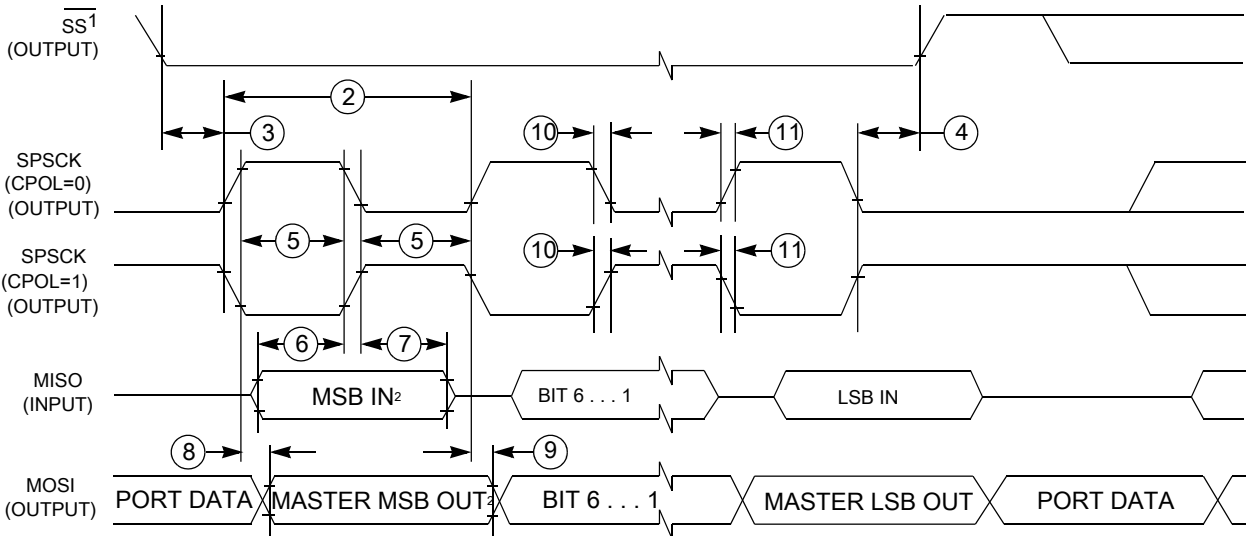
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Table 15. SPI master mode timing (continued)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)


1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 16. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{Bus} - 25$	ns	—
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output	—	25	ns	—

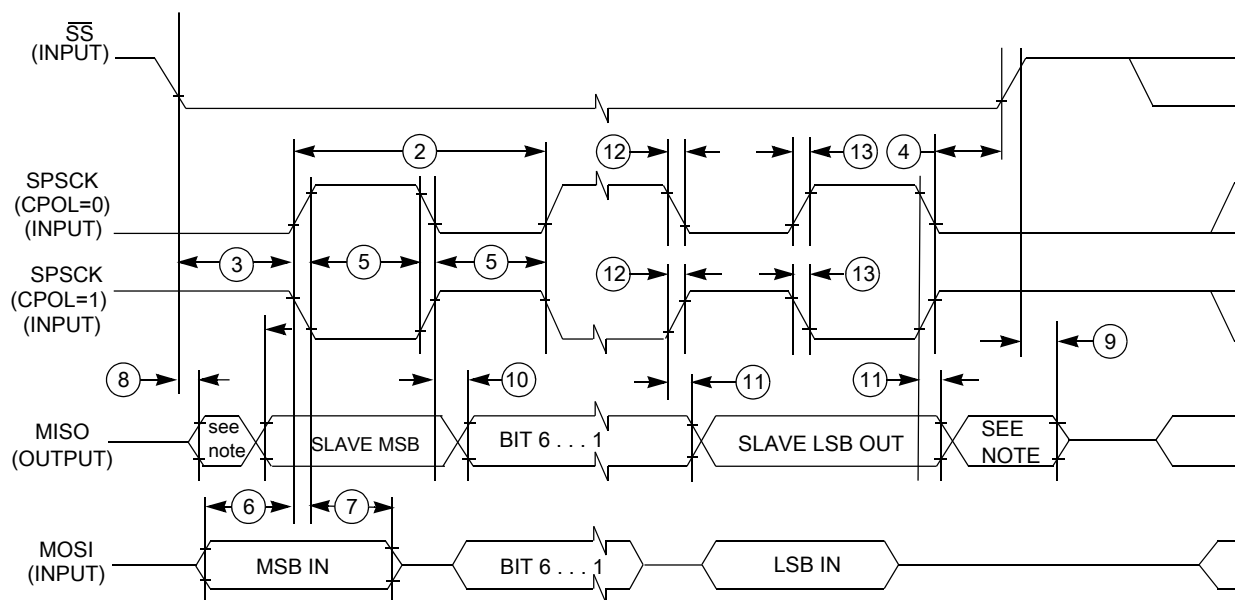


Figure 19. SPI slave mode timing (CPHA = 0)

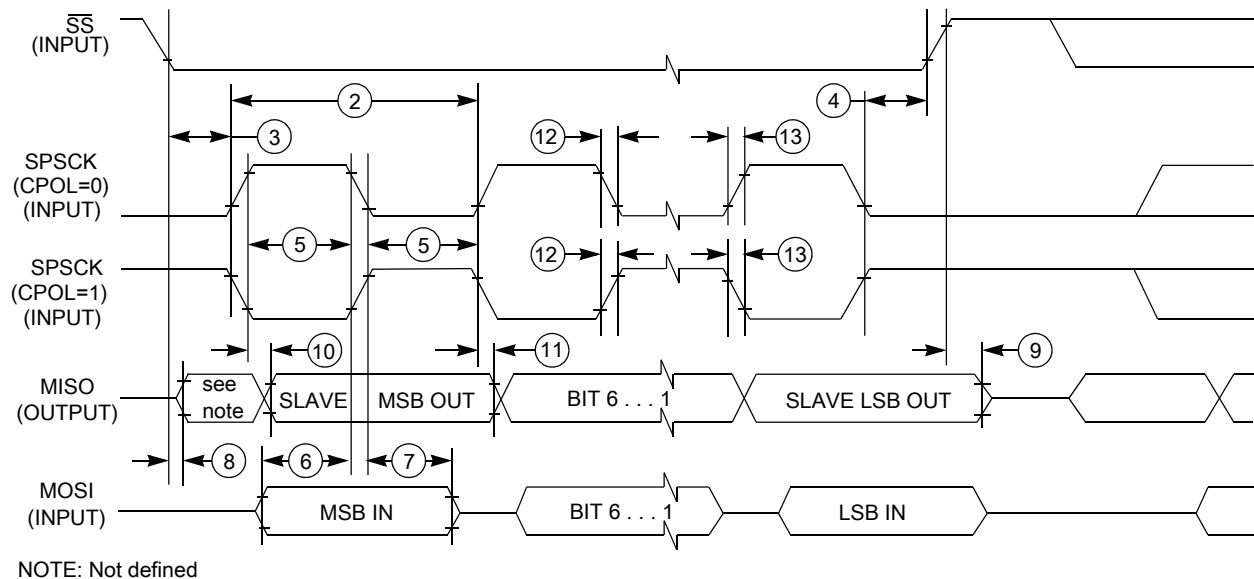


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
20-pin SOIC	98ASB42343B
20-pin TSSOP	98ASH70169A
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 17. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
44-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	—	—	PTD1 ¹	—	FTM2CH3	—	—
2	2	—	—	PTD0 ¹	—	FTM2CH2	—	—
3	—	—	—	PTE4	—	TCLK2	—	—
4	—	—	—	PTE3	—	BUSOUT	—	—
5	3	3	3	—	—	—	—	V _{DD}
6	4	—	—	—	—	—	V _{DDA}	V _{REFH}
7	5	—	—	—	—	—	V _{SSA}	V _{REFL}
8	6	4	4	—	—	—	—	V _{SS}
9	7	5	5	PTB7	—	—	SCL	EXTAL
10	8	6	6	PTB6	—	—	SDA	XTAL
11	—	—	—	—	—	—	—	V _{ss}
12	9	7	7	PTB5 ¹	—	FTM2CH5	SS0	—
13	10	8	8	PTB4 ¹	—	FTM2CH4	MISO0	—
14	11	9	—	PTC3	—	FTM2CH3	ADP11	—
15	12	10	—	PTC2	—	FTM2CH2	ADP10	—
16	—	—	—	PTD7	—	—	—	—
17	—	—	—	PTD6	—	—	—	—
18	—	—	—	PTD5	—	—	—	—
19	13	11	—	PTC1	—	FTM2CH1	ADP9	—
20	14	12	—	PTC0	—	FTM2CH0	ADP8	—
21	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	—
22	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	—
23	17	15	11	PTB1	KBI0P5	TXD0	ADP5	—
24	18	16	12	PTB0	KBI0P4	RXD0	ADP4	—
25	19	—	—	PTA7	—	FTM2FAULT2	ADP3	—
26	20	—	—	PTA6	—	FTM2FAULT1	ADP2	—
27	—	—	—	—	—	—	—	V _{ss}
28	—	—	—	—	—	—	—	V _{DD}

Table continues on the next page...

Table 17. Pin availability by package pin-count (continued)

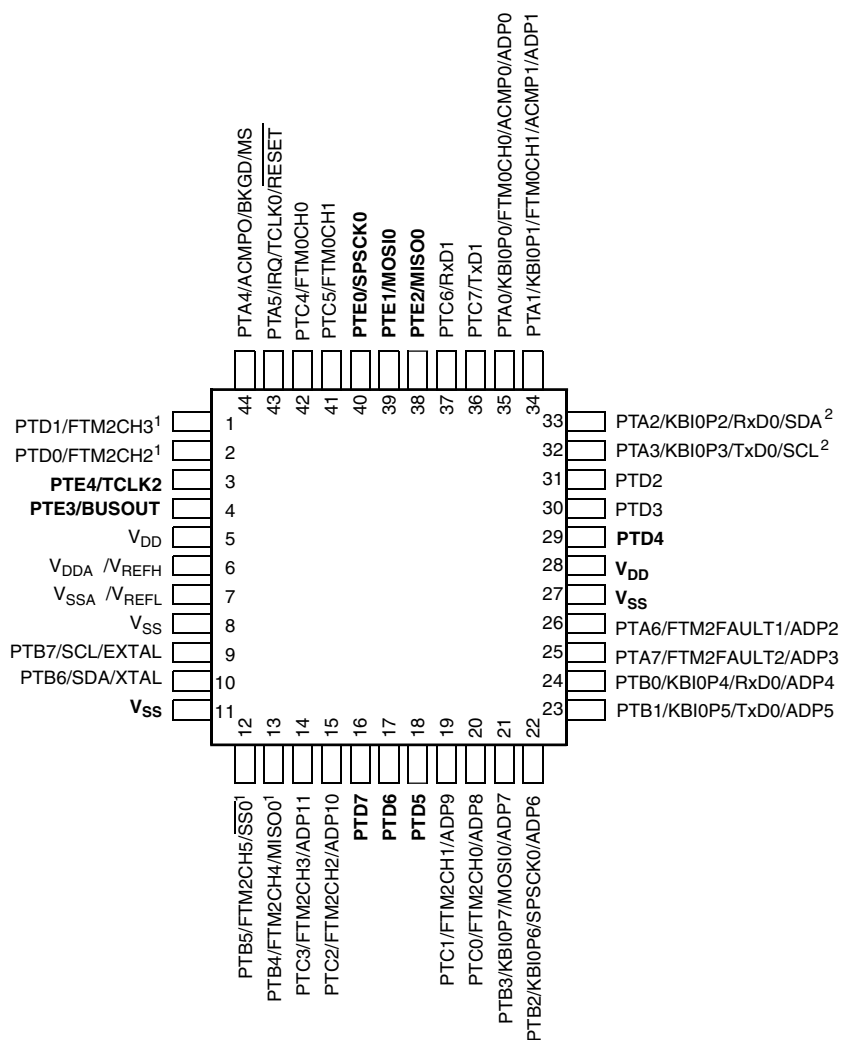
Pin Number				Lowest Priority <-- --> Highest				
44-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
29	—	—	—	PTD4	—	—	—	—
30	21	—	—	PTD3	—	—	—	—
31	22	—	—	PTD2	—	—	—	—
32	23	17	13	PTA3 ²	KBI0P3	TXD0	SCL	—
33	24	18	14	PTA2 ²	KBI0P2	RXD0	SDA	—
34	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
35	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
36	27	—	—	PTC7	—	TxD1	—	—
37	28	—	—	PTC6	—	RxD1	—	—
38	—	—	—	PTE2	—	MISO0	—	—
39	—	—	—	PTE1	—	MOSI0	—	—
40	—	—	—	PTE0	—	SPSCK0	—	—
41	29	—	—	PTC5	—	FTM0CH1	—	—
42	30	—	—	PTC4	—	FTM0CH0	—	—
43	31	1	1	PTA5	IRQ	TCLK0	—	RESET
44	32	2	2	PTA4	—	ACMPO	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment

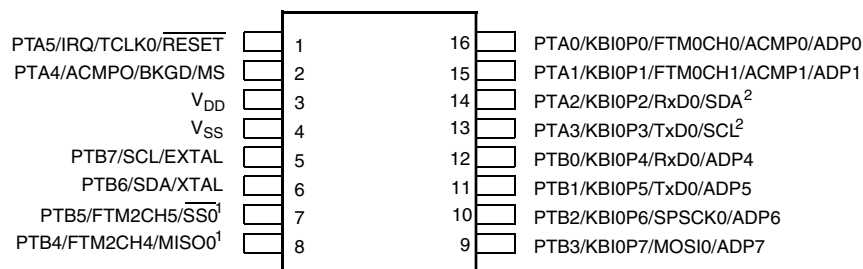


Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 21. MC9S08PA16 44-pin LQFP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 24. MC9S08PA16 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
1	10/2012	Initial public release
2	09/2014	- Updated V_{OH} and V_{OL} in DC characteristics - Updated footnote on the $S3I_{DD}$ in Supply current characteristics - Added EMC radiated emissions operating behaviors - Updated the typical of f_{int_t} to 31.25 kHz and updated footnote to $t_{Acquire}$ in External oscillator (XOSC) and ICS characteristics - Updated the assumption for all the timing values in SPI switching specifications - Updated the rating descriptions for t_{Rise} and t_{Fall} in Control timing - Updated the part number format to add new field for new part numbers in Fields
3	06/2015	- Corrected the Min. of the t_{extrst} in Control timing - Updated Thermal characteristics to add footnote to the T_A and removed redundant information. Updated the symbol of θ_{JA} to $R_{\theta JA}$.