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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa8avtgr

- Input/Output
 - Up to 37 GPIOs including one output-only pin
 - One 8-bit keyboard interrupt module (KBI)
 - Two true open-drain output pins
 - Four, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 44-pin LQFP
 - 32-pin LQFP
 - 20-pin SOIC; 20-pin TSSOP
 - 16-pin TSSOP

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PA16 and PA8.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA (V) B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	<ul style="list-style-type: none"> MC = fully qualified, general market flow
9	Memory	<ul style="list-style-type: none"> 9 = flash based
S08	Core	<ul style="list-style-type: none"> S08 = 8-bit CPU
PA	Device family	<ul style="list-style-type: none"> PA
AA	Approximate flash size in KB	<ul style="list-style-type: none"> 16 = 16 KB 8 = 8 KB
(V)	Mask set version	<ul style="list-style-type: none"> (blank) = Any version A = Rev. 2 or later version, this is recommended for new design

Table continues on the next page...

Field	Description	Values
B	Operating temperature range (°C)	<ul style="list-style-type: none"> • V = –40 to 105
CC	Package designator	<ul style="list-style-type: none"> • LD = 44-LQFP • LC = 32-LQFP • TJ = 20-TSSOP • WJ = 20-SOIC • TG = 16-TSSOP

2.4 Example

This is an example part number:

MC9S08PA16VLD

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, XTAL, or true open drain pin PTA2 and PTA3)	-0.3	$V_{DD} + 0.3$	V
	Digital input voltage (true open drain pin PTA2 and PTA3)	-0.3	6	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. All digital I/O pins, except open-drain pin PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} . PTA2 and PTA3 is only clamped to V_{SS} .

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	—	V
	C		High current drive pins, high-drive strength ²	5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	—	V

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I _{OHT}	D	Output high current	Max total I _{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V _{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, I _{load} = 5 mA	—	—	0.8	V
	C			3 V, I _{load} = 2.5 mA	—	—	0.8	V
	C	High current drive pins, high-drive strength ²		5 V, I _{load} = 20 mA	—	—	0.8	V
	C			3 V, I _{load} = 10 mA	—	—	0.8	V
I _{OLT}	D	Output low current	Max total I _{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V _{IH}	P	Input high voltage	All digital inputs	V _{DD} > 4.5V	0.70 × V _{DD}	—	—	V
	C			V _{DD} > 2.7V	0.75 × V _{DD}	—	—	
V _{IL}	P	Input low voltage	All digital inputs	V _{DD} > 4.5V	—	—	0.30 × V _{DD}	V
	C			V _{DD} > 2.7V	—	—	0.35 × V _{DD}	
V _{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V _{DD}	—	—	mV
I _{IN}	P	Input leakage current	All input only pins (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZ}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZTOT}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V _{IN} = V _{DD} or V _{SS}	—	—	2	μA
R _{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R _{PU} ³	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I _{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	V _{IN} < V _{SS} , V _{IN} > V _{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C _{in}	C	Input capacitance, all pins		—	—	—	7	pF
V _{RAM}	C	RAM retention voltage		—	2.0	—	—	V

- Typical values are measured at 25 °C. Characterized, not tested.
- Only PTB4, PTB5, PTD0, PTD1 support ultra high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for , are internally clamped to V_{SS} and V_{DD}.
- Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.

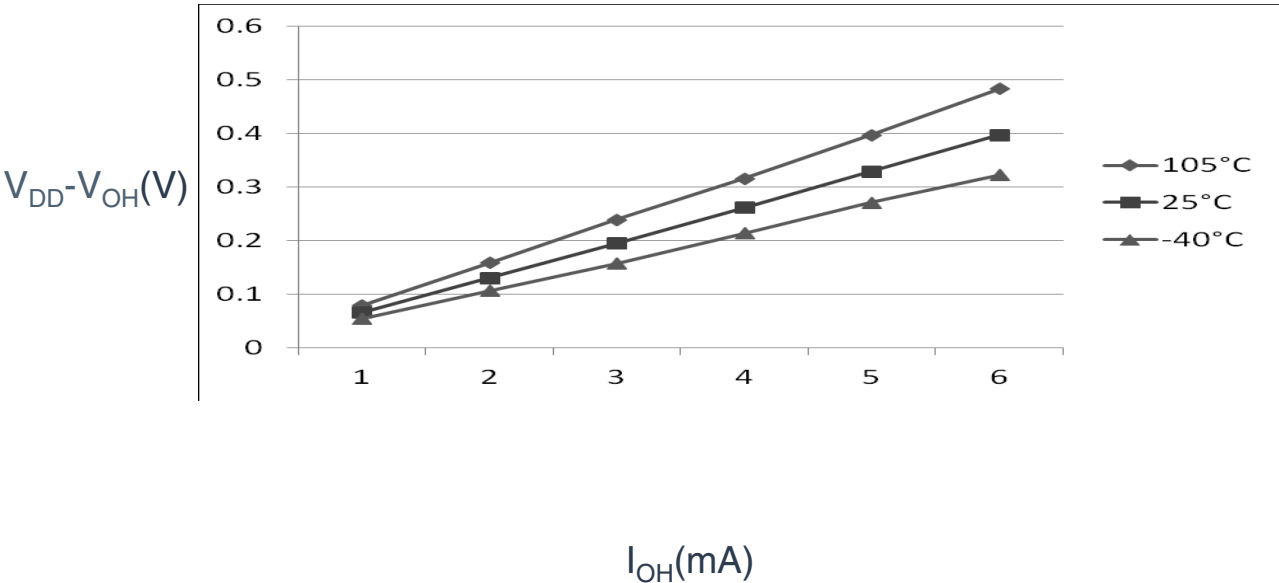


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

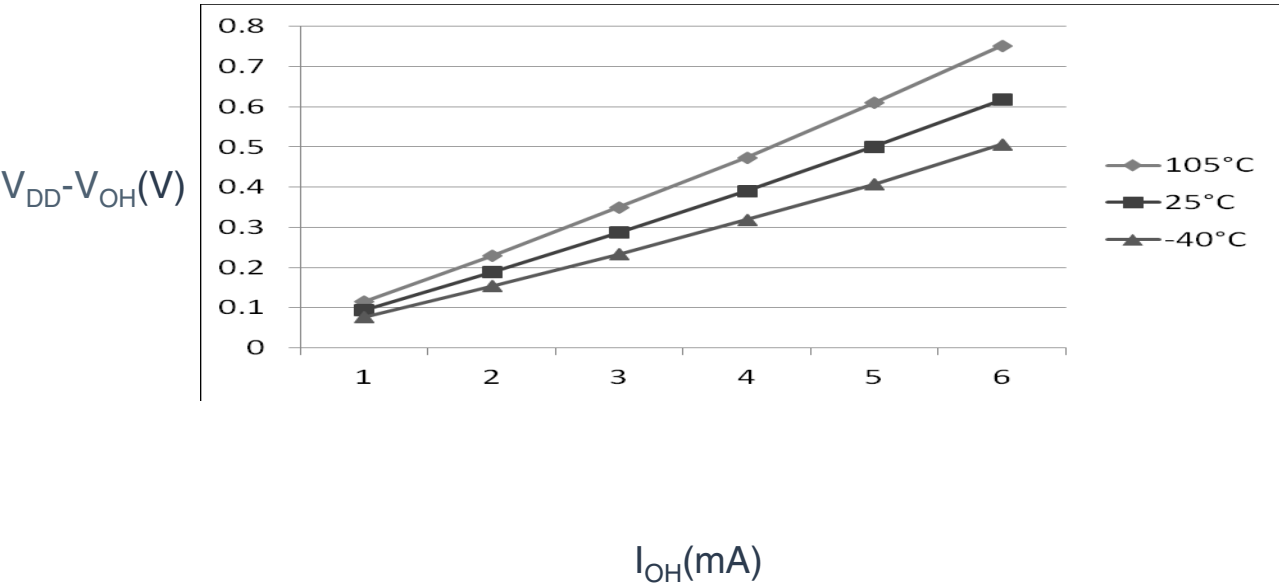


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

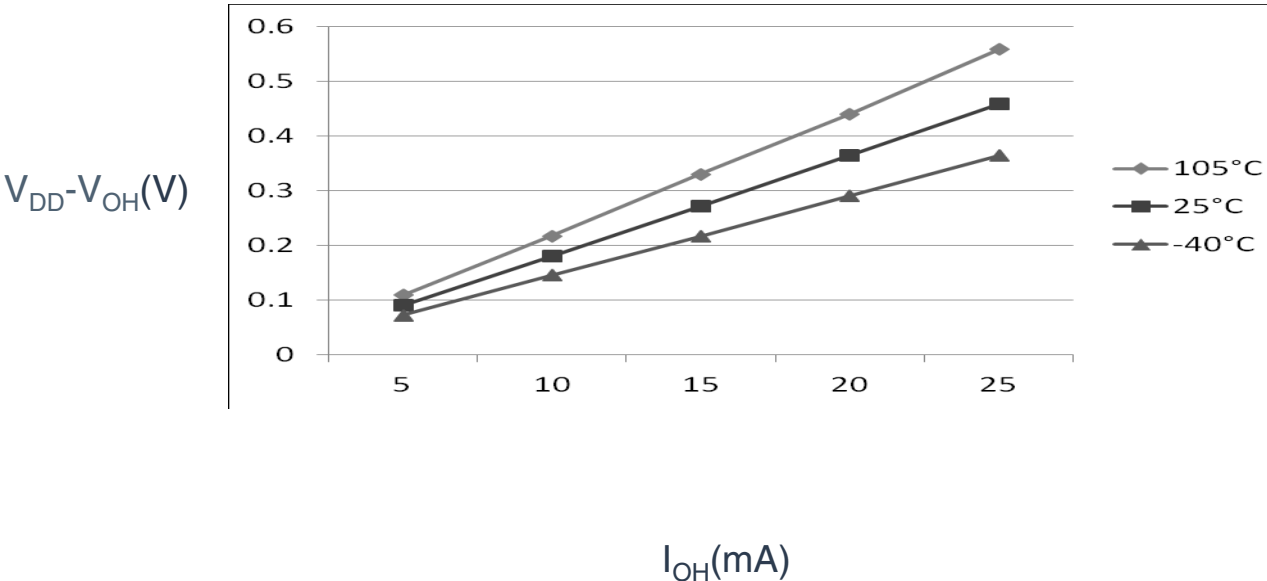


Figure 3. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 5 V)

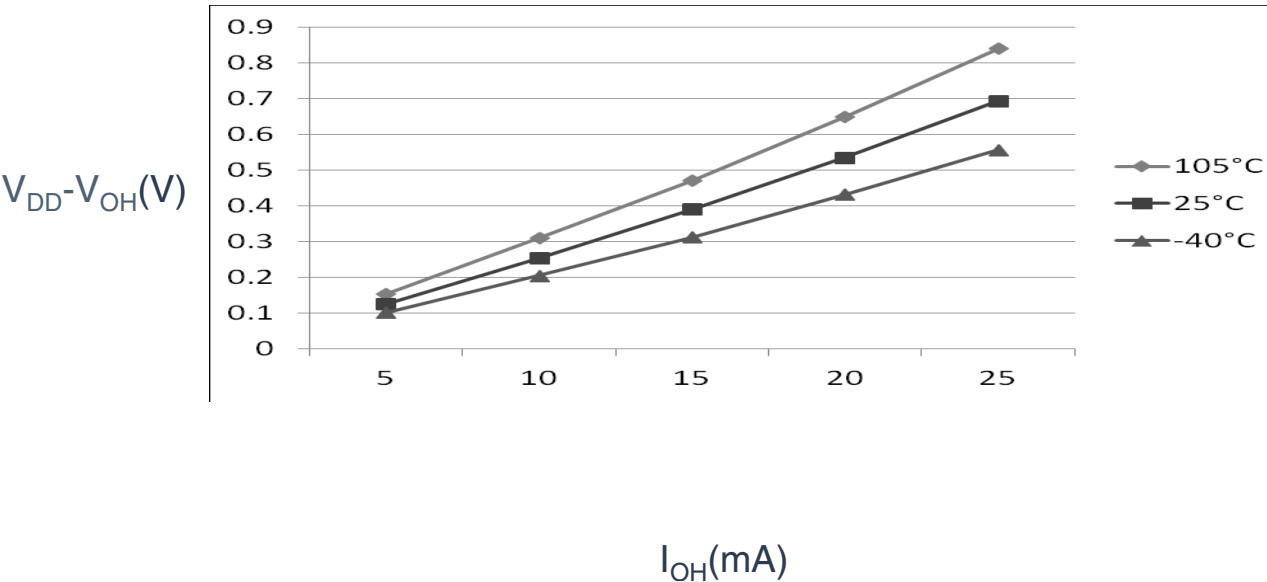


Figure 4. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 3 V)

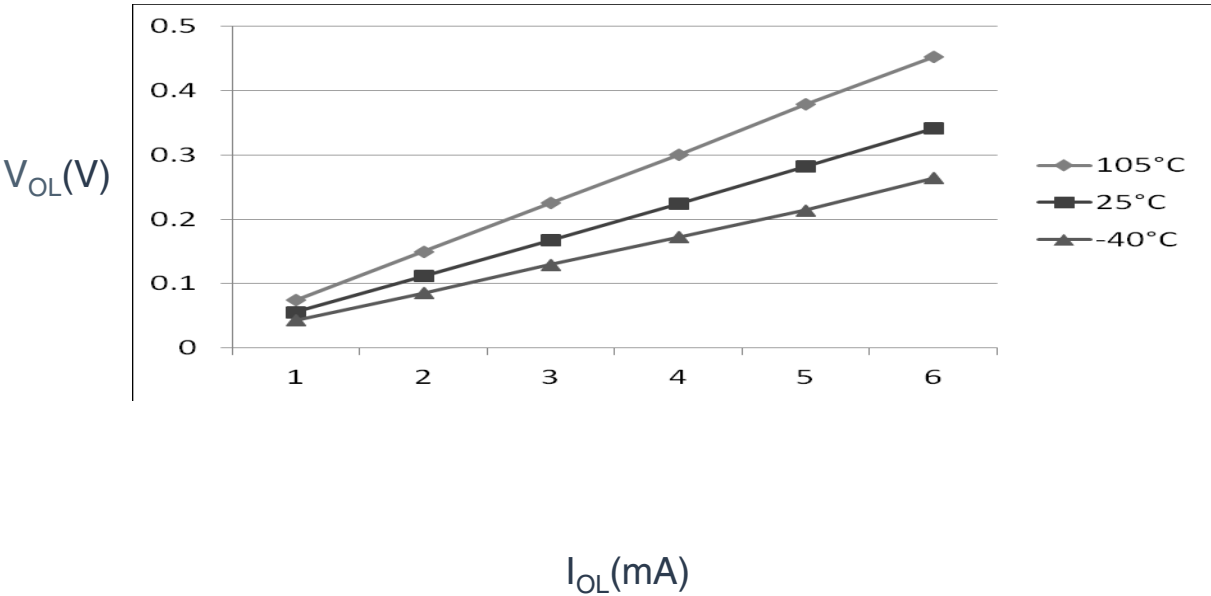


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5$ V)

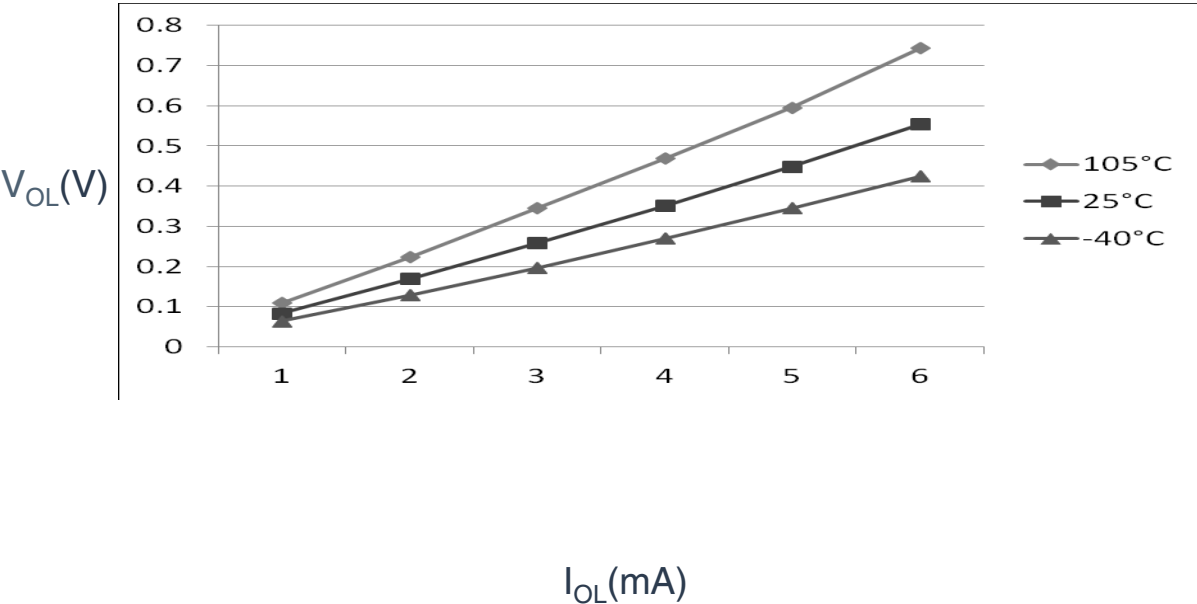


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3$ V)

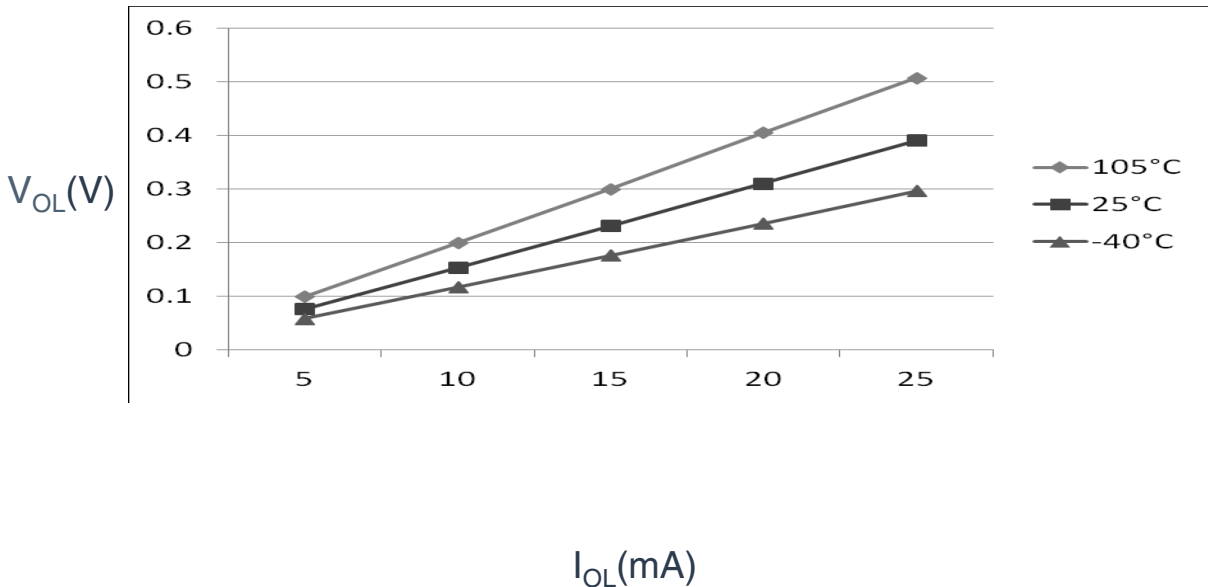


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

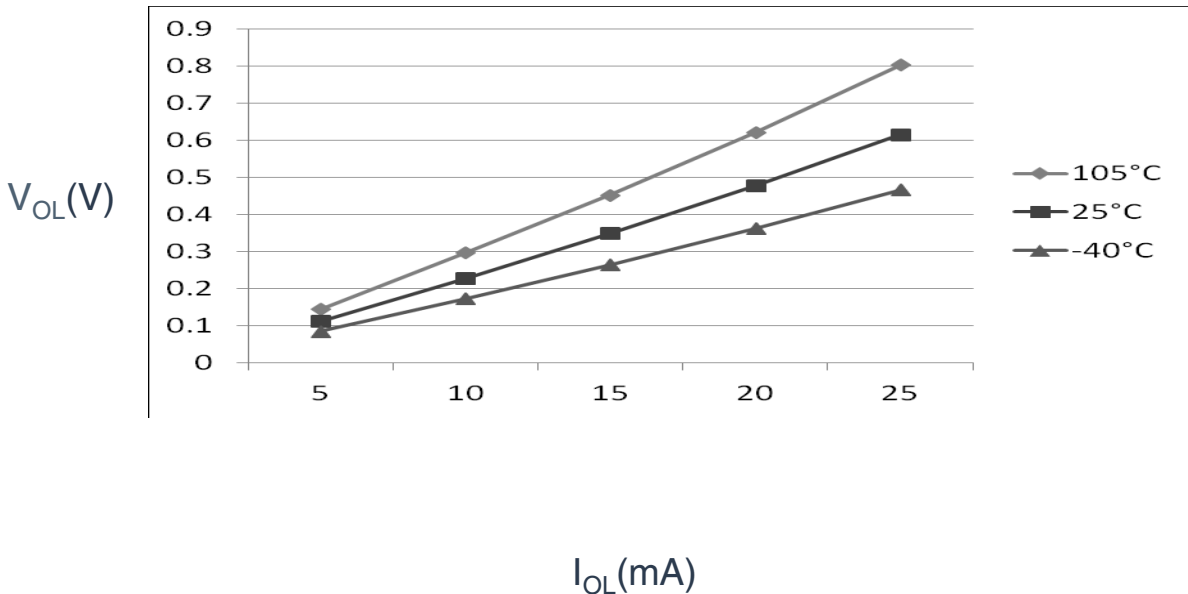


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	LVD adder to stop3 ⁴	—	—	5	128	—	μA	-40 to 105 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

Table 5. EMC radiated emissions operating behaviors for 44-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	8	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	8	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	8	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 20 MHz, f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 9. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A ¹	T_L to T_H -40 to 105	°C
Junction temperature range	T_J	-40 to 150	°C
Thermal resistance single-layer board			
44-pin LQFP	$R_{\theta JA}$	76	°C/W
32-pin LQFP	$R_{\theta JA}$	88	°C/W
20-pin SOIC	$R_{\theta JA}$	82	°C/W
20-pin TSSOP	$R_{\theta JA}$	116	°C/W
16-pin TSSOP	$R_{\theta JA}$	130	°C/W
Thermal resistance four-layer board			
44-pin LQFP	$R_{\theta JA}$	54	°C/W
32-pin LQFP	$R_{\theta JA}$	59	°C/W
20-pin SOIC	$R_{\theta JA}$	54	°C/W
20-pin TSSOP	$R_{\theta JA}$	76	°C/W
16-pin TSSOP	$R_{\theta JA}$	87	°C/W

- Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

6 Peripheral operating requirements and behaviors

Table 11. Flash characteristics (continued)

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	t_{DRD1SEC}	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t_{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to $T_H = -40^\circ\text{C}$ to 105°C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T_L to $T_H = -40^\circ\text{C}$ to 105°C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of $T_{\text{Javg}} = 85^\circ\text{C}$ after up to 10,000 program/erase cycles	$t_{\text{D_ret}}$	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{\text{cyc}} = 1 / f_{\text{NVMBUS}}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ²	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB ³
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB ³
	10-bit mode ⁴	P		—	±0.25	±0.5	
	8-bit mode ⁴	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB ³
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error ⁵	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB ³
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	±2.5	—	LSB ³
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB ³
Input leakage error ⁷	all modes	D	E_{IL}	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{in} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

Table 14. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted, and 100 pF load on all SPI pins. All timing assumes high drive strength is enabled for SPI output pins.

Table 15. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—

Table continues on the next page...

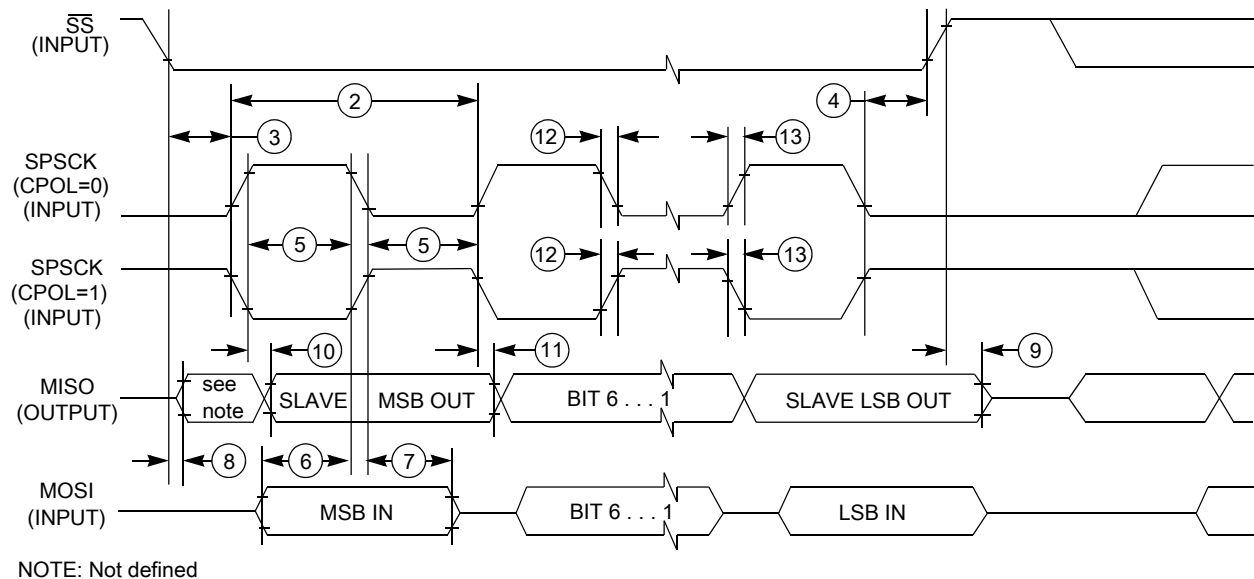


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
20-pin SOIC	98ASB42343B
20-pin TSSOP	98ASH70169A
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 17. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
44-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	—	—	PTD1 ¹	—	FTM2CH3	—	—
2	2	—	—	PTD0 ¹	—	FTM2CH2	—	—
3	—	—	—	PTE4	—	TCLK2	—	—
4	—	—	—	PTE3	—	BUSOUT	—	—
5	3	3	3	—	—	—	—	V _{DD}
6	4	—	—	—	—	—	V _{DDA}	V _{REFH}
7	5	—	—	—	—	—	V _{SSA}	V _{REFL}
8	6	4	4	—	—	—	—	V _{SS}
9	7	5	5	PTB7	—	—	SCL	EXTAL
10	8	6	6	PTB6	—	—	SDA	XTAL
11	—	—	—	—	—	—	—	V _{ss}
12	9	7	7	PTB5 ¹	—	FTM2CH5	SS0	—
13	10	8	8	PTB4 ¹	—	FTM2CH4	MISO0	—
14	11	9	—	PTC3	—	FTM2CH3	ADP11	—
15	12	10	—	PTC2	—	FTM2CH2	ADP10	—
16	—	—	—	PTD7	—	—	—	—
17	—	—	—	PTD6	—	—	—	—
18	—	—	—	PTD5	—	—	—	—
19	13	11	—	PTC1	—	FTM2CH1	ADP9	—
20	14	12	—	PTC0	—	FTM2CH0	ADP8	—
21	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	—
22	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	—
23	17	15	11	PTB1	KBI0P5	TXD0	ADP5	—
24	18	16	12	PTB0	KBI0P4	RXD0	ADP4	—
25	19	—	—	PTA7	—	FTM2FAULT2	ADP3	—
26	20	—	—	PTA6	—	FTM2FAULT1	ADP2	—
27	—	—	—	—	—	—	—	V _{ss}
28	—	—	—	—	—	—	—	V _{DD}

Table continues on the next page...

Table 17. Pin availability by package pin-count (continued)

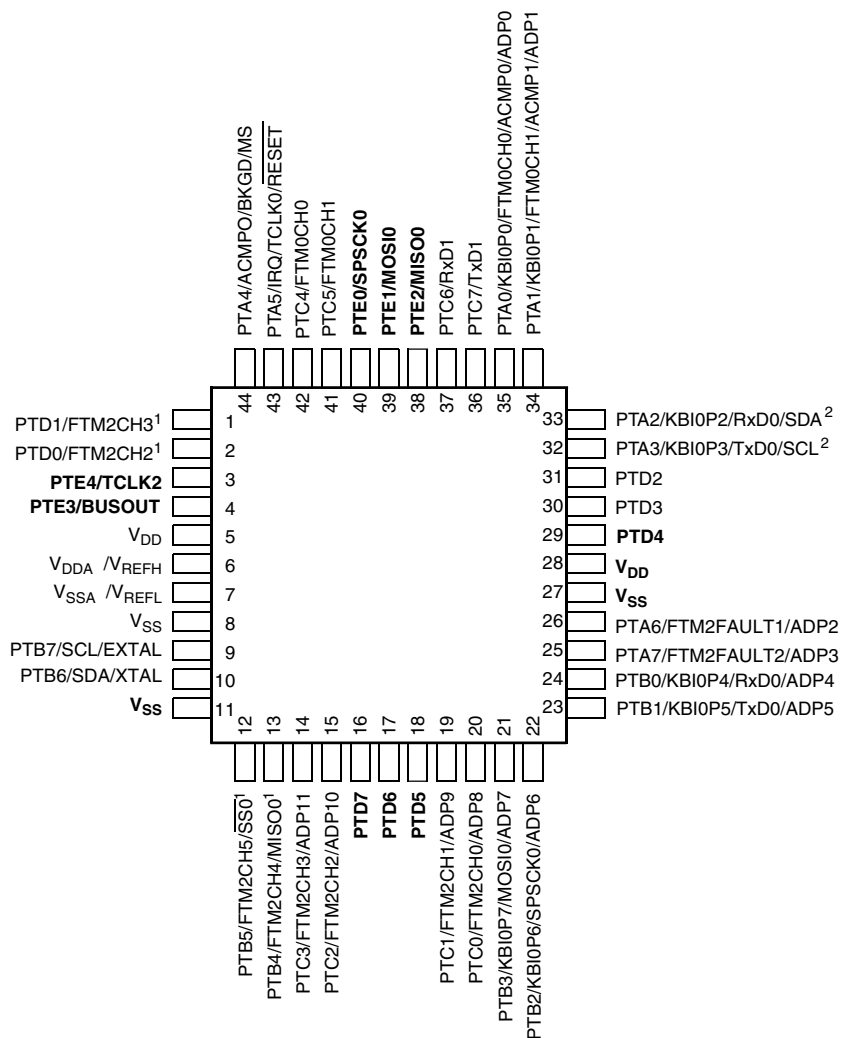
Pin Number				Lowest Priority <-- --> Highest				
44-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
29	—	—	—	PTD4	—	—	—	—
30	21	—	—	PTD3	—	—	—	—
31	22	—	—	PTD2	—	—	—	—
32	23	17	13	PTA3 ²	KBI0P3	TXD0	SCL	—
33	24	18	14	PTA2 ²	KBI0P2	RXD0	SDA	—
34	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
35	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
36	27	—	—	PTC7	—	TxD1	—	—
37	28	—	—	PTC6	—	RxD1	—	—
38	—	—	—	PTE2	—	MISO0	—	—
39	—	—	—	PTE1	—	MOSI0	—	—
40	—	—	—	PTE0	—	SPSCK0	—	—
41	29	—	—	PTC5	—	FTM0CH1	—	—
42	30	—	—	PTC4	—	FTM0CH0	—	—
43	31	1	1	PTA5	IRQ	TCLK0	—	RESET
44	32	2	2	PTA4	—	ACMPO	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment

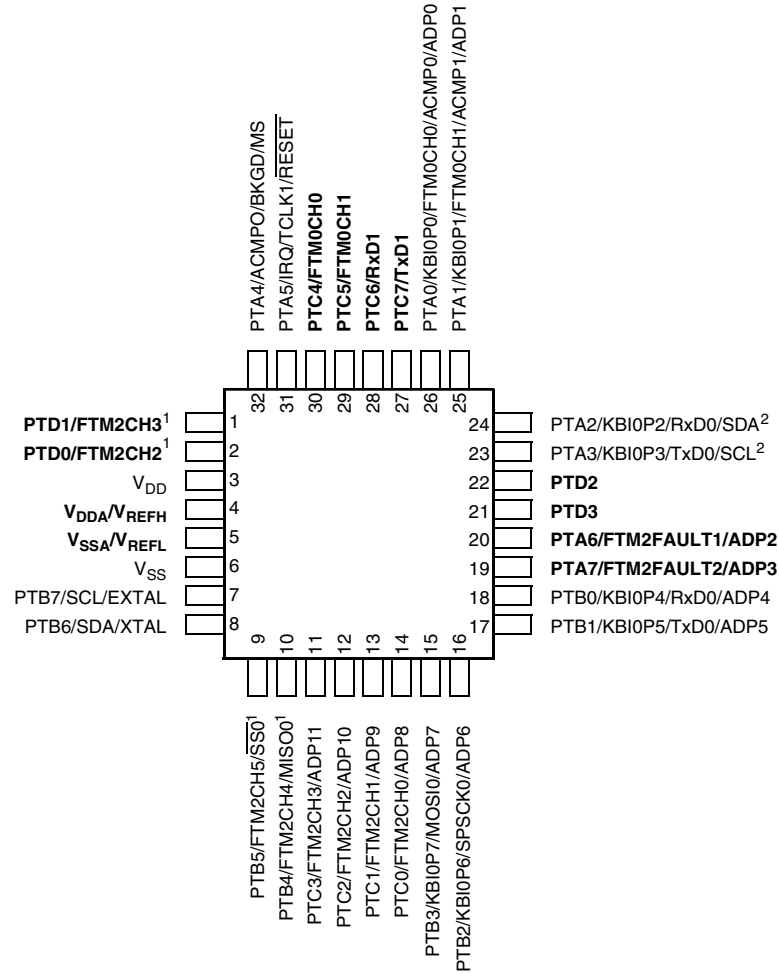


Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 21. MC9S08PA16 44-pin LQFP package

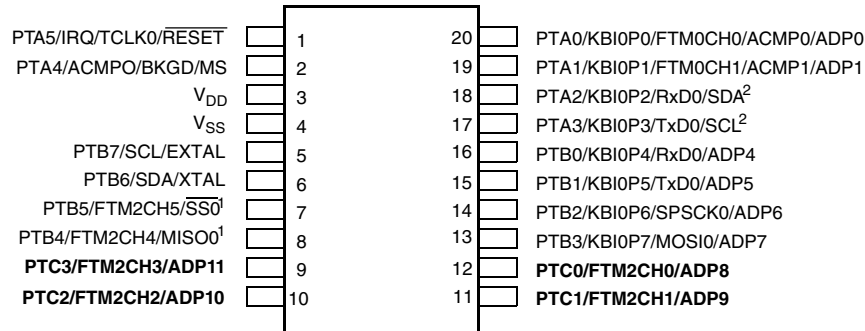


Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 22. MC9S08PA16 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 23. MC9S08PA16 20-pin SOIC and TSSOP package