Renesas Electronics America Inc - R5F2136CCNFP#V0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136ccnfp-v0

5. Block diagram

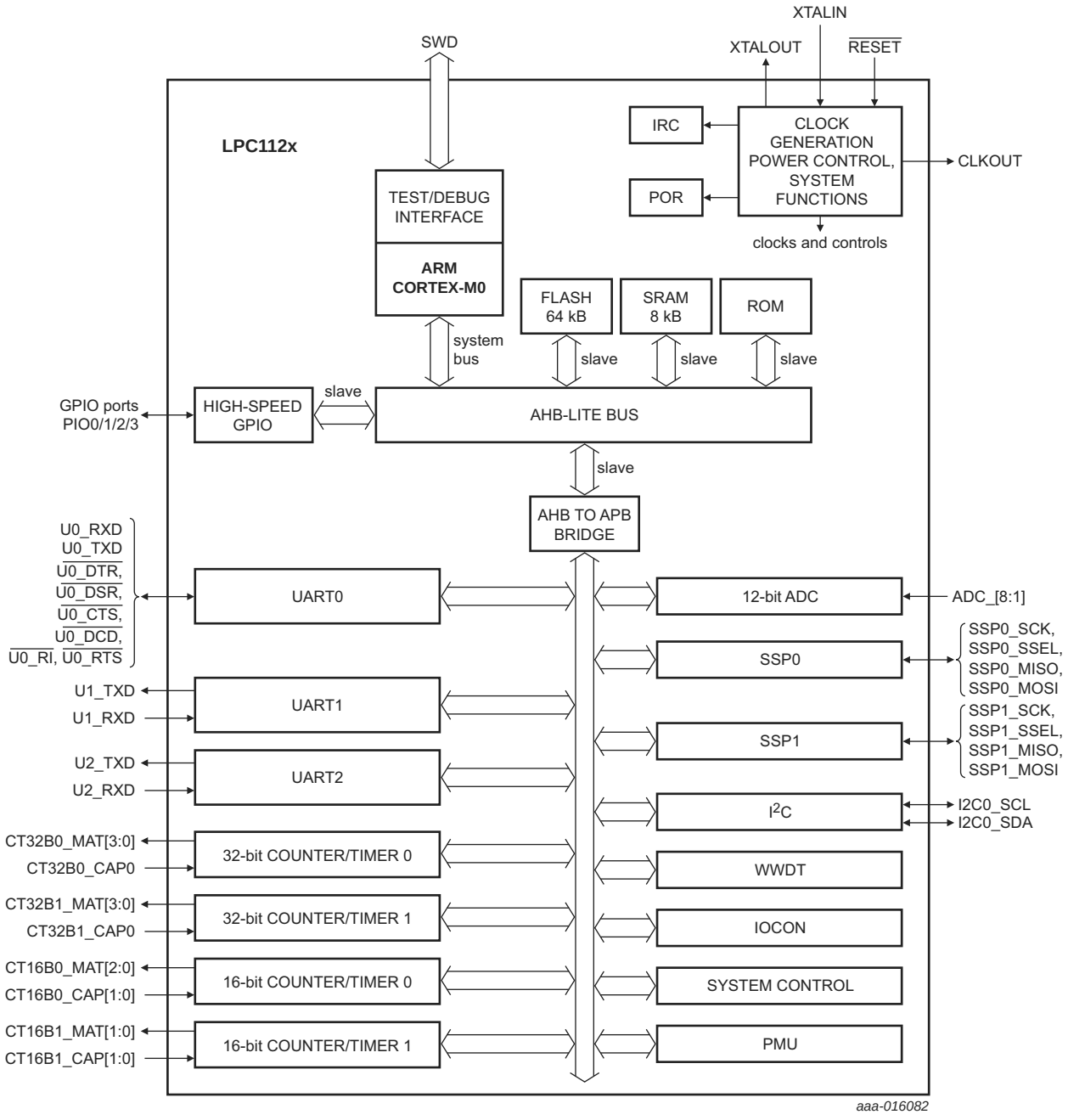


Fig 1. LPC112x block diagram

6. Pinning information

6.1 Pinning

Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
P0_9	27	[5]	inactive; pull-up enabled	I/O		PIO0_9 — General purpose digital input/output pin.
				I/O	SSP0_MOSI — Master Out Slave In for SSP0.
				O	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
				-	Reserved.
				I	ADC_PIN_TRIG3 — ADC trigger input 3.
SWCLK/PIO0_10	28		[5]	inactive; pull-up enabled	I/O	SWCLK — Serial wire clock.
					I/O	PIO0_10 — General purpose digital input/output pin.
					I/O	SSP0_SCK — Serial clock for SSP0.
					O	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11	6		[6]	inactive; pull-up enabled	I	R — Reserved configurable as GPIO pin. Do not configure this pin as GPIO.
					I/O	PIO0_11 — General purpose digital input/output pin.
					A	ADC_7 — ADC input 7.
					O	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
R/PIO1_0	13		[6]	inactive; pull-up enabled	I	R — Reserved configurable as GPIO pin. Do not configure this pin as GPIO.
					I/O	PIO1_0 — General purpose digital input/output pin.
					A	ADC_6 — ADC input 6.
					I	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1	23		[6]	inactive; pull-down	O	R — Reserved configurable as GPIO pin. Do not configure this pin as GPIO.
					I/O	PIO1_1 — General purpose digital input/output pin.
					A	ADC_5 — ADC input 5.
					O	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2	5		[6]	inactive; pull-up enabled	I	R — Reserved configurable as GPIO pin. Do not configure this pin as GPIO.
					I/O	PIO1_2 — General purpose digital input/output pin.
					A	ADC_4 — ADC input 4.
					O	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3	8		[6]	inactive; pull-up enabled	I/O	SWDIO — Serial wire debug input/output. Used for serial wire debugging.
					I/O	PIO1_3 — General purpose digital input/output pin.
					A	ADC_3 — ADC input 3.
					O	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.

Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	I	U0_DCD — [illegible]
					I/O	SSP1_MISO — [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	I	U0_RI — [illegible]
					I/O	SSP1_MOSI — [illegible]
[illegible]	19	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					O	CT16B1_MAT1 — [illegible]
					I/O	SSP1_SSEL — [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					O	CT32B0_MAT0 — [illegible]
[illegible]	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					O	CT32B0_MAT1 — [illegible]
[illegible]	11	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					O	CT32B0_MAT2 — [illegible]
					I	U0_RXD — [illegible]
[illegible]	12	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	CT32B0_MAT3 — [illegible]
					O	U0_TXD — [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	CT32B0_CAP0 — [illegible]
[illegible]	-	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					O	U0_DTR — [illegible]
					O	CT16B0_MAT0 — [illegible]
					O	U0_TXD — [illegible]
[illegible]	-	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	U0_DCD — [illegible]
					O	CT16B0_MAT2 — [illegible]
					I/O	SSP1_SCK — [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	U0_RI — [illegible]
					I	CT16B0_CAP0 — [illegible]
[illegible]	18	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	CT16B0_CAP1 — [illegible]
					I	U0_RXD — [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
					I	CT16B1_CAP1 — [illegible]
					O	U0_TXD — [illegible]

Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
[illegible]	6	[illegible]	-	-	-	[illegible] 1.8 V
[illegible]	7	[illegible]	-	-	-	[illegible]
[illegible]	3	-	-	-	[illegible]	
[illegible]	[illegible]	-	-	-	[illegible]	
V_D	8, 4		-	-	-	[illegible]
$V_{[illegible]}$	[illegible]	-	-	-	[illegible]	
$V_{[illegible]}$	[illegible]	-	-	-	[illegible]	
V_S	5, [illegible]		-	-	-	[illegible]

[1] [illegible] V D [illegible] (V D = 3 V); [illegible]

[2] [illegible]

[3] 5 V [illegible]).

[4] [illegible] . [illegible]). [illegible]

[5] [illegible] ([illegible]).

[6] [illegible] ([illegible]).

[7] I^2C [illegible] I^2C [illegible]

[8] 5 V [illegible]

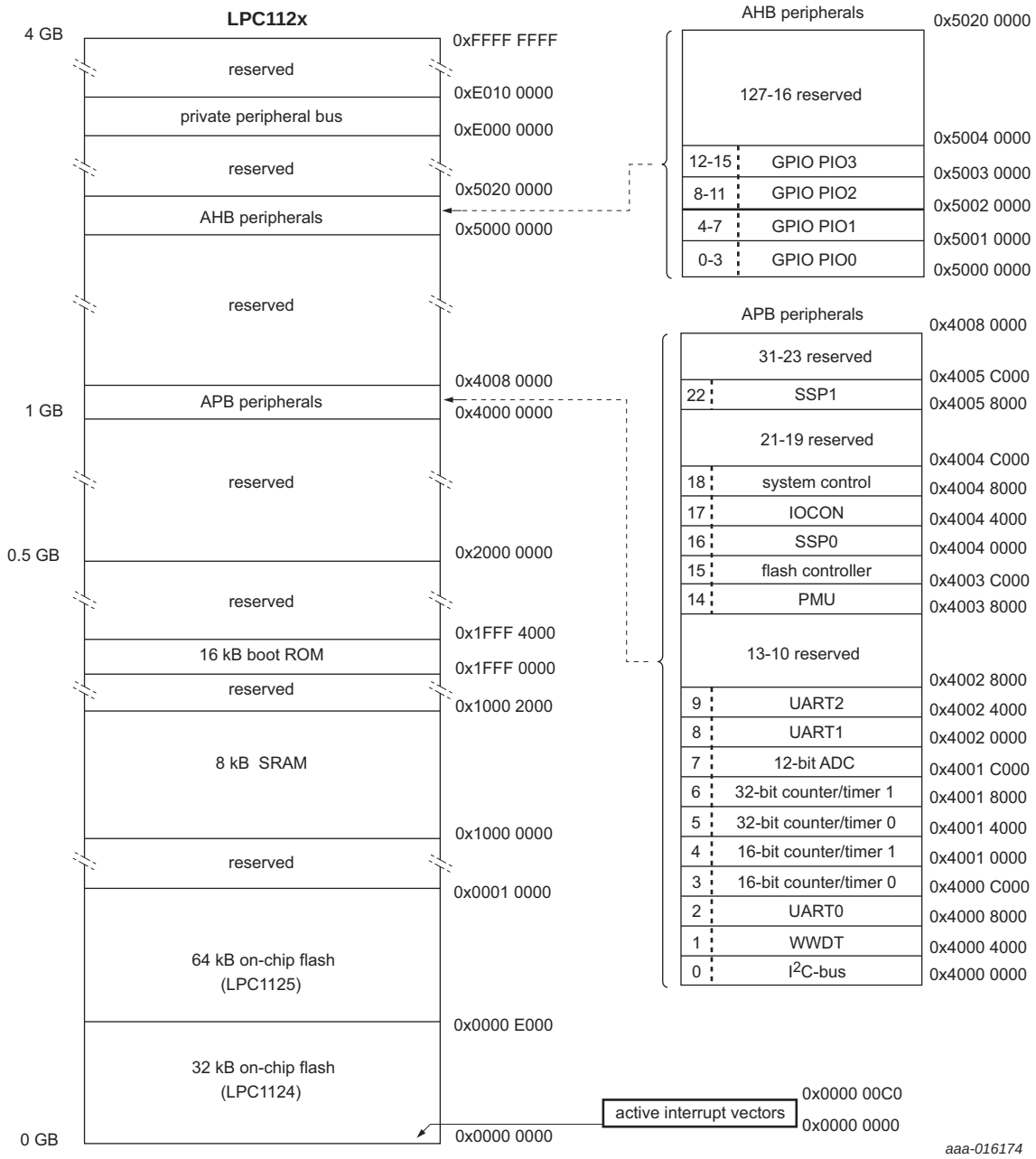


Fig 3. LPC112x memory map

7.5 Nested Vectored Inte rrupt Controller (NVIC)

7.5.1 Features

- [illegible]

7.10.1 Features

- I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode
- Easy to configure as master, slave, or master/slave
- Programmable clocks allow versatile rate control
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock stretching and pulse skipping of data bits to slow down bit rate
- Wake-up from power-down mode on address recognition
- I²C-bus can be used for test and diagnostic purposes
- I²C-bus controller supports multiple address recognition and a bus monitor mode

7.11 Analog-to-Digital Converter (ADC)

One 12-bit successive approximation analog-to-digital converter with eight channels and conversion times as low as 2.44 µs per channel.

Hardware-triggered conversion.

7.11.1 Features

- 12-bit successive approximation analog-to-digital converter
- 12-bit conversion rate of 400 ksamples/s
- Eight channels
- Burst conversion mode for single or multiple inputs
- Optional conversion on transition on input pin or timer match signal
- Individual result registers for each ADC channel to reduce interrupt overhead
- Overrun status flag
- Single-power and dedicated analog supply pins for noise reduction
- Power-down mode

7.12 General purpose externa l event counter/timers

7.12.1 Features

- A
- C
- I
- T
  - I
- E
  - C
  - C
  - E
- I
  - C
  - C
  - C
  - C

7.13 System tick timer

7.14 Windowed WatchDog Timer

7.14.1 Features

- T
- T
- T
- T

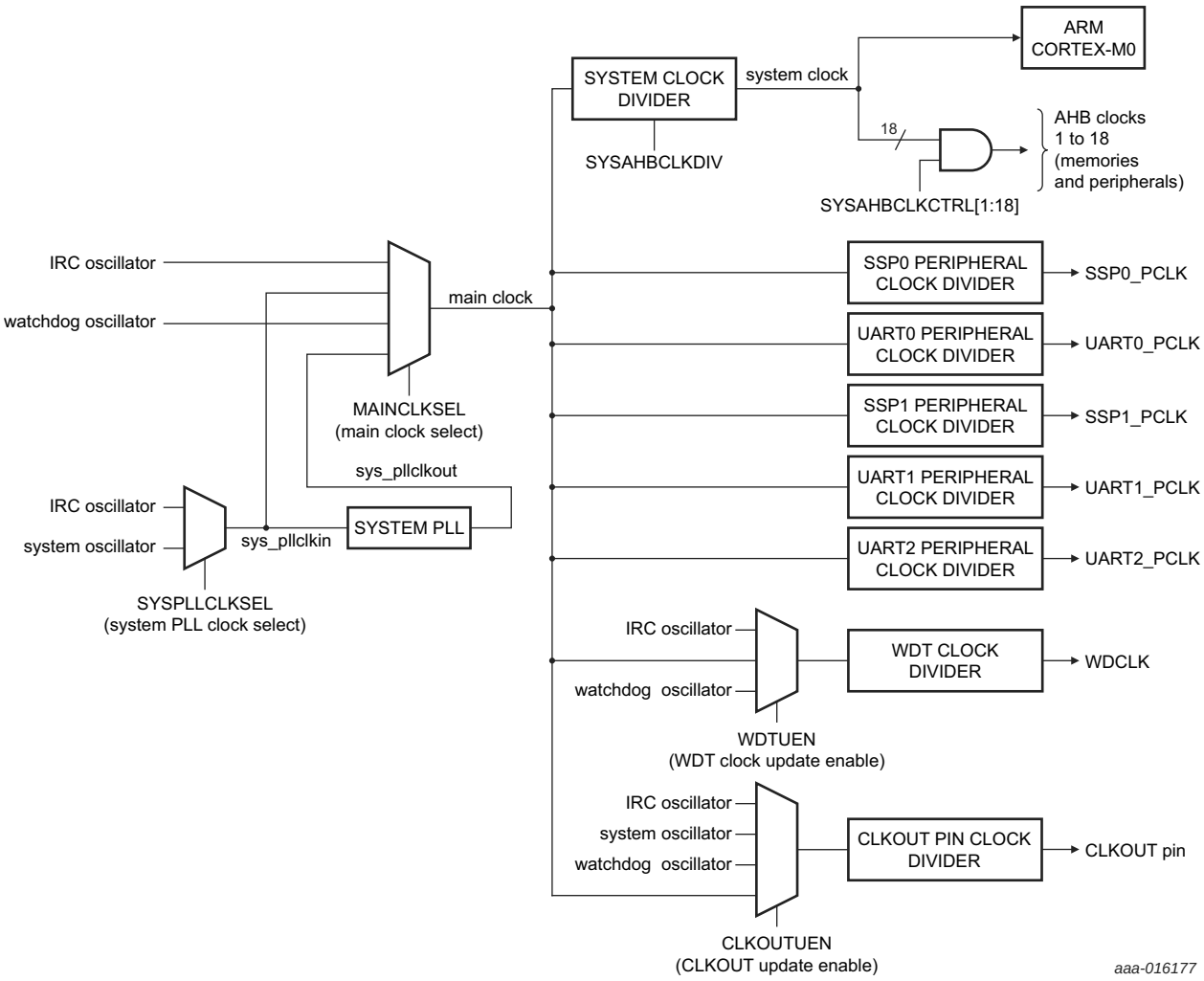


Fig 4. LPC112x clock generation block diagram

7.15.1.1 Internal RC oscillator

7.15.1.2 System oscillator

7.15.1.3 Watchdog oscillator

[illegible]

7.15.2 System PLL

[illegible]

7.15.3 Clock output

[illegible]

7.15.4 Wake-up process

[illegible]

7.15.5 Power control

[illegible]

7.15.5.1 Power profiles

[illegible]

- [illegible]
- [illegible]

CAUTION

LPC112x user manual.

7.16.5 APB interface

7.16.6 AHBLite

7.16.7 External interrupt inputs

7.17 Emulation and debugging

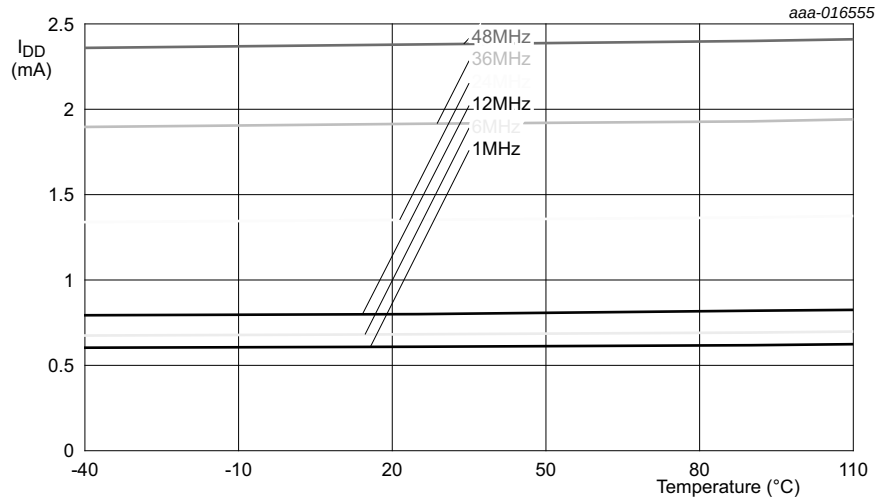
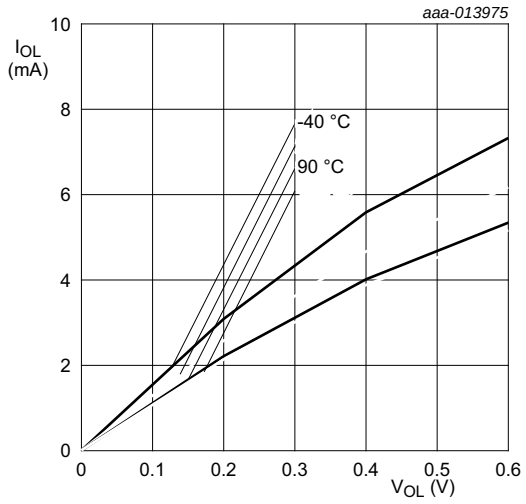


Fig 6. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



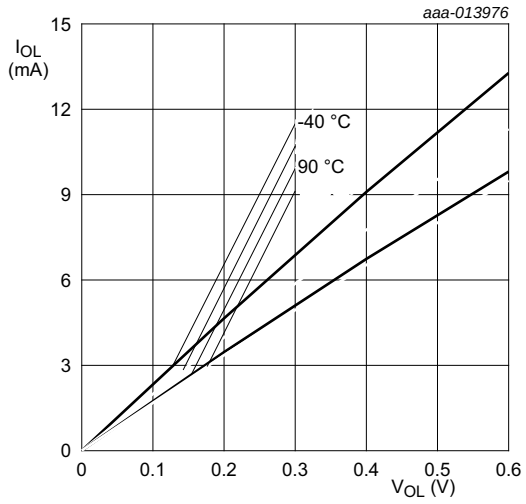
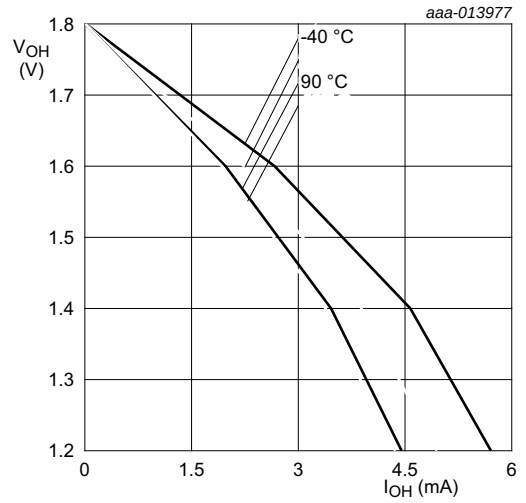


Fig 13. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



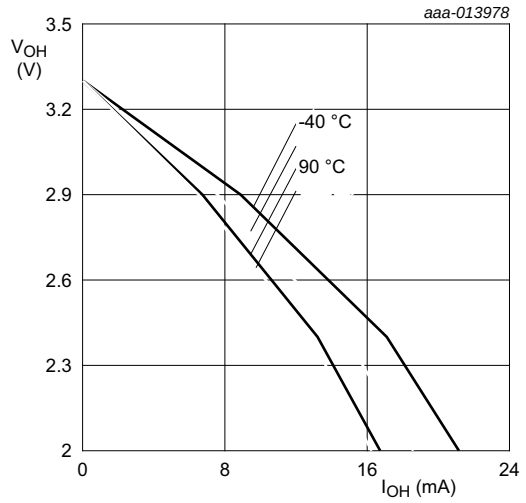


Fig 14. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

11.5 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins [1]
T_{amb} = 40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL	[3][4][5][6][7]	Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Fast-mode	$20 + 0.1 C_b$	300	ns
			Fast-mode Plus	-	120	ns
$t_{HD;DAT}$	data hold time		Standard-mode	47	-	ns
			Fast-mode	1.3	-	ns
			Fast-mode Plus	0.5	-	ns
$t_{SU;DAT}$	data set-up time		Standard-mode	40	-	ns
			Fast-mode	0.6	-	ns
			Fast-mode Plus	0.2	-	ns
t_{SP}	pulse width of spikes	[8][9][10]	Standard-mode	0	-	ns
			Fast-mode	0	-	ns
			Fast-mode Plus	0	-	ns
t_{SP}	pulse width of spikes	[9][10]	Standard-mode	2	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Operating temperature is dependent on power dissipation.

[3] t_r rise time

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters and pull-up resistors are implemented in accordance with the I²C-bus specification and support Fast-mode Plus.

[7] Fast-mode Plus is supported on pins PIO0_4 and PIO0_5 only.

[8] Minimum pulse width of spikes that must be suppressed by the input filter. The spikes suppression can be disabled by the I²C configuration registers.

[9] Pulse width of spikes that must be suppressed by the input filter.

[10] Accepted by the I²C-bus interface. The I²C-bus interface will not lengthen the LOW period of the SCL signal. Slave devices connected to the I²C-bus may add a clock stretch period to the LOW period of the SCL signal (see *UM10204*). Bus speeds of 1 Mbit/s may not be achieved if clock stretching is used.

[11] t_{SP} pulse width of spikes

[12] Accepted by the I²C-bus interface. Only if the I²C-bus interface is configured as a master or a slave with clock stretching enabled. In slave mode with clock stretching disabled, the I²C-bus interface will not lengthen the LOW period of the SCL signal. Bus speeds of 1 Mbit/s may not be achieved if clock stretching is used.

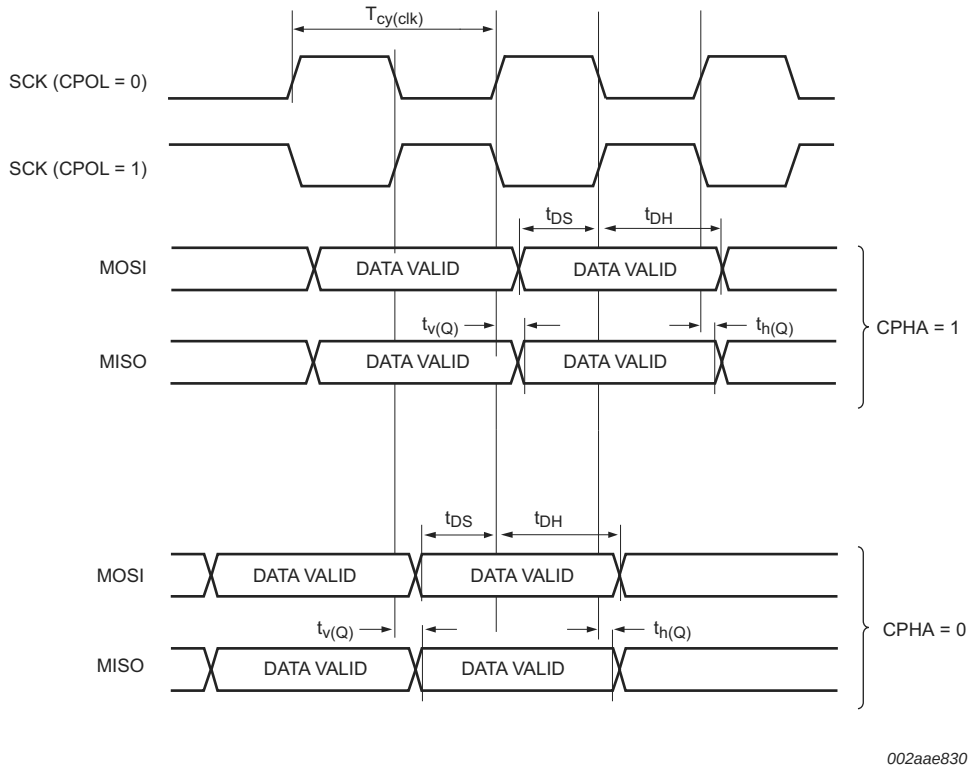


Fig 21. SSP slave timing in SPI mode

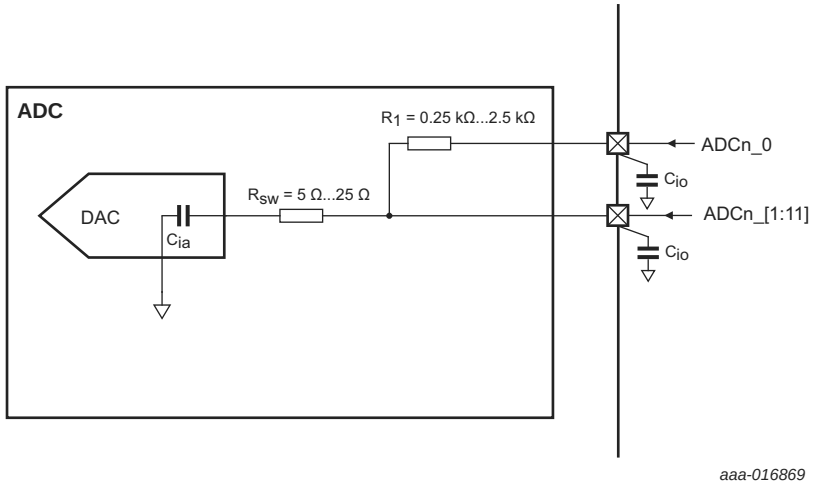


Fig 23. ADC input impedance

13. Application information

13.1 ADC usage notes

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]

13.2 XTAL input

[illegible] 1.8 V [illegible]

C_i = 100 pF [illegible]

[illegible] C_g [illegible] $C_i/(C_i + C_g)$. [illegible]

200 mV (RMS) [illegible]

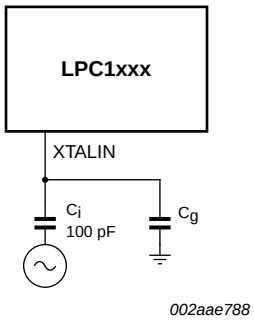


Fig 24. Slave mode operation of the on-chip oscillator

[illegible] 100 pF

([illegible]), [illegible] 200 mV (RMS) 1000 mV (RMS) [illegible]

[illegible] 1.4 V

[illegible]

[illegible] [illegible] [illegible]

[illegible] [illegible] and [illegible]. [illegible]

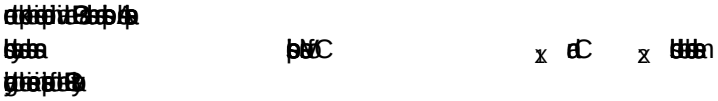
[illegible] x and x [illegible]

([illegible] [illegible] [illegible]

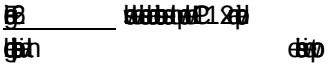
R_S). [illegible] P in [illegible] [illegible]

[illegible] , C_L, R_S and P [illegible]

[illegible]).



13.4 Connecting power, clo cks, and debug functions



13.5 Termination of unused pins

not

Table 19. Termination of unused pins

Pin	Default state [1]	Recommended termination of unused pins
		•
	-	
	-	

[1]

13.6 Pin states in different power modes

Table 20. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
		[1]		
		[1]		
		[1]		

[1]

13.7 Standard I/O pad configuration

- [illegible]

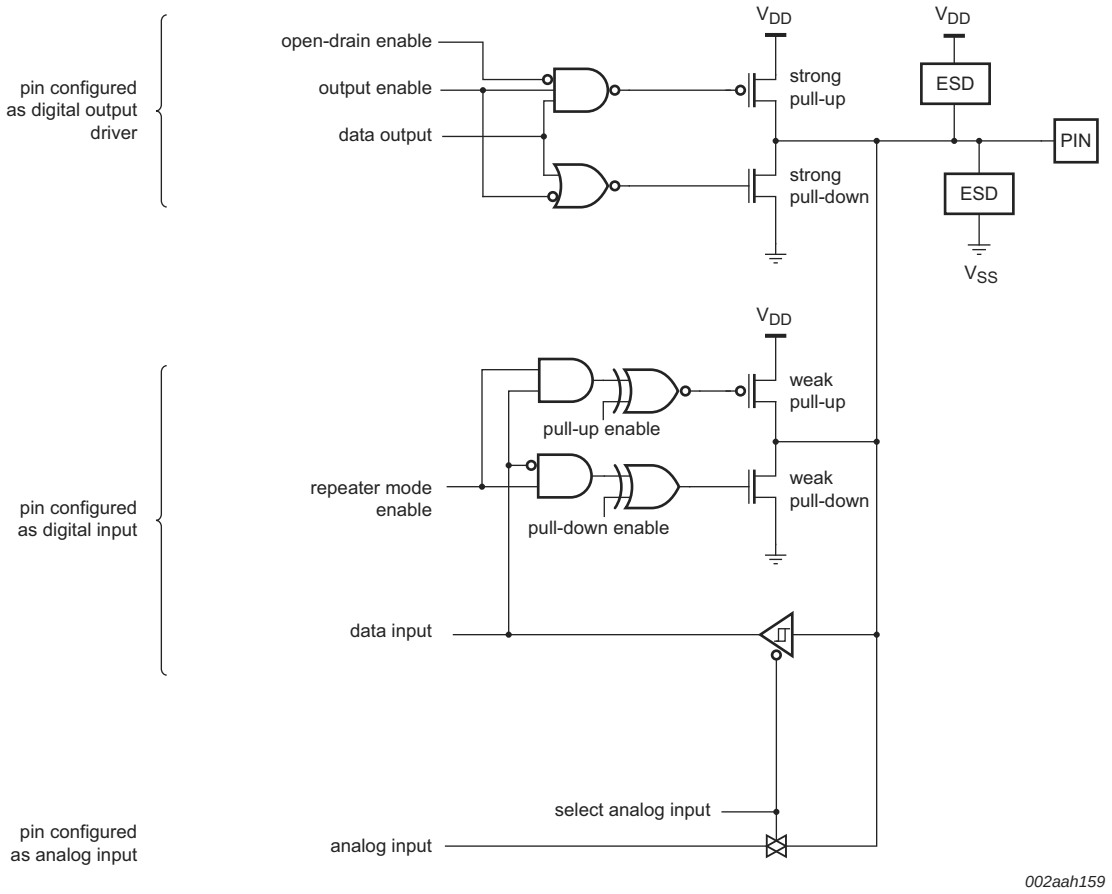


Fig 27. Standard I/O pad configuration

16. Abbreviations

Table 21. Abbreviations

Acronym	Description
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	
[illegible]	

17. References

[illegible]

[illegible]

[illegible] *UM10204*.

[illegible]